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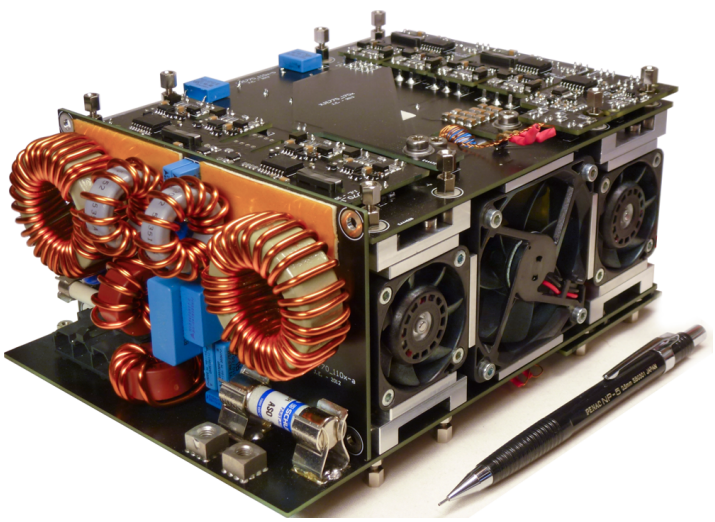
Modeling and Optimization of Bidirectional Dual Active Bridge AC–DC Converter Topologies



Jordi Everts

Dissertation presented in partial
fulfillment of the requirements for the
degree of Doctor in Engineering Science

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Jordi EVERTS

Examination Committee:
Prof. dr. ir. J. Vandewalle, chair
Prof. dr. ir. J. Driesen, supervisor
Prof. dr. ir. G. Deconinck
Prof. dr. ir. D. Schreurs
Prof. dr. ir. J. Poortmans
Prof. dr. ir. J. Genoe
Prof. dr. ir. J.W. Kolar
(ETH Zürich, Switzerland)
Dr. ir. J. Van den Keybus
(Triphase NV, Belgium)

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v.u. Leen Cuypers, Arenberg Doctoral School, W. de Croylaan 6, 3001 Heverlee

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Abstract

Single-phase, utility interfaced, isolated AC–DC converters with power factor correction cover a wide range of applications such as chargers for plug-in hybrid electric vehicles and battery electric vehicles, inverters for multiple renewable energy sources (e.g. photovoltaic modules), as well as interfaces for residential DC distribution systems and energy storage systems. Moreover, bidirectional conversion capability enables the development of smart interactive power networks in which the energy systems play an active role in providing different types of support to the grid. Examples are vehicle-to-grid concepts, 'smart home' concepts, AC microgrids, and residential DC distribution systems (DC nanogrids).

In the presented work, the main objective is to investigate the feasibility and suitability of a single-stage (1-S) dual active bridge (DAB) AC–DC converter for the realization of the above mentioned bidirectional energy conversions. Compared to the commonly used dual-stage (2-S) systems, the 1-S architecture has the potential to benefit the system performance with regard to efficiency, volume (power density), number of components (reliability), weight, and costs, due to the effective omission of a complete energy conversion stage. In order to validate the presented analyses, a second objective is to realize a state-of-the-art (i.e. regarding efficiency and power density) converter prototype system that is designed in order to meet the requirements for future, mode 1 compatible, on-board electric vehicle battery chargers, interfacing a 400 V_{nom} DC-bus with the single-phase 230 V_{AC} / 50 Hz mains. Compliance with domestic power sockets results in a nominal (active) AC charging current of $I_{AC,P} = 16$ A_{rms} and a nominal power of $P_{nom} = 3.7$ kW.

The main challenge to achieve the above objectives lies in addressing the fundamental limitations of the existing analyses and circuit implementations of DAB converters. These limitations mainly relate to the soft-switching (i.e. by virtue of zero voltage switching, ZVS) modulation schemes available in literature, being especially problematic for DAB converters with large input and/or output voltage variations and large power variations, such as is the case for the 1-S DAB AC–DC architecture at hand. By means of an introductory Chapter (i.e. Chapter 2), the shortcomings in the existing analyses of DAB converters are highlighted, and the selection of the full bridge - full bridge (FBFB) DAB implementation as the most

suitable candidate for the considered AC–DC converter topology is motivated. The subsequent chapters discuss the 1-S DAB AC–DC converter in detail:

- Chapter 3 outlines the operating principle of the DAB AC–DC converter. The exact operating range of the DAB DC–DC converter, as the main building block of the 1-S AC–DC architecture, is derived, and a control equation for the DAB input current is obtained. Furthermore, the steady-state analysis of the DAB is presented and 'commutation inductance(s)' are introduced as an essential HF AC-link modification in order to achieve full-operating-range ZVS. Lastly, a novel 'current-dependent charge-based' (CDCB) ZVS verification method is proposed in order to deal with the deficiencies of the existing current-based (CB) and energy-based (EB) ZVS analyses;
- Chapter 4 is devoted to the derivation of full-operating-range ZVS modulation schemes for the DAB converter. Three different approaches are presented, being a numerical approach, an analytical approach, and a semi-analytical approach, all relying on the CDCB ZVS verification method proposed in Chapter 3 in order to assure that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions;
- In Chapter 5, the main functional elements of the DAB AC–DC prototype converter are designed, employing the values for the circuit level variables and the ZVS modulation schemes derived in Chapter 4. State-of-the-art design methods/procedures, models for the component losses, and volume models are combined with custom developed (local) optimization algorithms in order to obtain a high-efficiency and high-power-density converter design that is in compliance with the specified system requirements;
- In Chapter 6, first a DC–DC system characterization of the prototype system is presented in order to validate the theoretical analyses, i.e. the steady-state converter model and the ZVS analysis outlined in Chapter 3, as well as the CDCB ZVS modulation schemes proposed in Chapter 4. Thereafter, the results of an AC–DC system characterization are given, allowing to evaluate the performance of the prototype converter with regard to the reached efficiency and with regard to the quality of the AC input power. Conversion efficiencies higher than 95 % within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency, are reported. The peak efficiency is around 96 % and the efficiency at nominal power approximately 95.6 %. Moreover, a high power density of 2 kW/liter is obtained. From a brief comparison with several (similar) dual-stage prototype systems found in literature, it is clear that the achieved performance is close to the absolute state-of-the-art;
- Chapter 7 concludes the presented work and provides an outlook regarding future research in the field of DAB AC–DC converters.

Samenvatting

Enkelfasige, netgekoppelde, geïsoleerde AC–DC omvormers met vermogensfactor correctie hebben een breed toepassingsgebied, zoals laders voor plug-in hybride-elektrische voertuigen en batterij-elektrische voertuigen, invertoren voor hernieuwbare energiebronnen (bv. fotovoltaïsche modules), alsook interfaces voor residentiële DC distributiesystemen en energieopslagsystemen. Bovendien laat de mogelijkheid tot bidirectionele vermogensoverdracht toe om slimme interactieve elektriciteitsnetten te ontwikkelen waarin de energiesystemen een actieve rol spelen in het aanbieden van verschillende netondersteunende diensten. Voorbeelden zijn 'voertuig-naar-net' concepten, 'slimme-huis' concepten, AC micronetten, en residentiële DC distributiesystemen (DC nanonetten).

Het voorgestelde werk onderzoekt de geschiktheid van een eentraps 'dual active bridge' (DAB) AC–DC omvormer voor de realisatie van de bovengenoemde bidirectionele energieconversies. In vergelijking met de traditionele tweetraps aanpak kan een eentraps systeem voordelig zijn op het gebied van efficiëntie, volume (vermogensdichtheid), aantal componenten (betrouwbaarheid), gewicht, en kost. Ter validatie van de theoretische analyses is een tweede doelstelling om een 'state-of-the-art' (d.w.z. met betrekking tot efficiëntie en vermogensdichtheid) prototype omvormer te realiseren die ontworpen is om te voldoen aan de vereisten voor toekomstige mode 1 batterijladers voor elektrische voertuigen. De beschouwde lader is aan boord van het voertuig opgesteld en koppelt een 400 V_{nom} DC-bus met het enkelfasige 230 V_{AC} / 50 Hz elektriciteitsnet. Compatibiliteit met huishoudelijke stopcontacten resulteert in een nominale (actieve) AC laadstroom van $I_{AC,P} = 16$ A_{rms} en een nominaal laadvermogen van $P_{nom} = 3.7$ kW.

De grootste moeilijkheid die gepaard gaat met het behalen van bovengenoemde doelstellingen ligt in het aanpakken van de fundamentele beperkingen van de bestaande analyses en circuitimplementaties van DAB omvormers. Deze beperkingen zijn vooral gerelateerd aan de modulatiestrategieën die voorhanden zijn om de DAB geheel zacht-schakelend (d.w.z. bij wijze van 'zero voltage switching, ZVS') te laten werken, en zijn vooral problematisch voor DAB omvormers die onderworpen zijn aan grote in- en/of uitgangsspanningsvariaties, zoals het geval is voor de beschouwde eentraps AC–DC architectuur. In een inleidend hoofdstuk (d.w.z. Hoofdstuk 2) worden de tekortkomingen van de bestaande analyses nader

toegelicht en wordt de keuze voor de volle brug - volle brug DAB als meest geschikte kandidaat gemotiveerd. In de daaropvolgende hoofdstukken wordt de eentraps DAB AC–DC omvormer uitvoerig besproken:

- In hoofdstuk 3 wordt het werkingsprincipe van de DAB AC–DC omvormer uitgelegd. Eerst wordt het exacte werkingsgebied van de DAB DC–DC omvormer, als hoofdbouwsteen van de eentraps AC–DC architectuur, bepaald. Hieruit wordt een vergelijking voor het berekenen van de DAB ingangsstroom verkregen. Daarna volgt de steady-state analyse van de DAB en worden 'commutatie inductantie(s)' geïntroduceerd als een essentiële AC-link modificatie voor het verkrijgen van ZVS in het volledige werkingsgebied. Tenslotte wordt een ladingsgebaseerde ZVS verificatie methode voorgesteld die veel nauwkeuriger is dan de stroom- en energiegebaseerde tegenhangers;
- Hoofdstuk 4 is toegewijd aan het afleiden van modulatieschema's die ZVS toelaten in het volledige werkingsgebied van de DAB omvormer. Drie verschillende aanpakken worden voorgesteld, zijnde een numerieke, een analytische, en een semi-analytische aanpak. Deze maken alle drie gebruik van de ZVS verificatie methode uit Hoofdstuk 3, waardoor een zacht-schakelende werking met quasi geen schakelverliezen verzekerd is in de berekende ZVS werkingsgebieden;
- In Hoofdstuk 5 worden, gebruik makend van de waardes voor de circuit variabelen en de ZVS modulatieschema's die bekomen werden in Hoofdstuk 4, de functionele elementen van het DAB AC–DC omvormer prototype ontworpen. State-of-the-art ontwerpmethodes en ontwerpprocedures, modellen voor de verliezen in de componenten, en modellen voor het berekenen van de ingenomen volumes worden gecombineerd met (lokale) optimalisatiealgoritmes ten einde een omvormer ontwerp met hoge efficiëntie en hoge vermogensdichtheid, en dat voldoet aan de gespecificeerde systeemvereisten, te bekomen;
- In Hoofdstuk 6 wordt eerst een DC–DC systeem karakterisatie van het omvormer prototype getoond met als doel de theoretische analyses te valideren, d.w.z. zowel het steady-state omvormer model en de ZVS analyse gepresenteerd in Hoofdstuk 3, als de ZVS modulatieschema's voorgesteld in Hoofdstuk 4. Daarna wordt een AC–DC systeem karakterisatie gegeven die toelaat om de performantie van het omvormer prototype te evalueren met betrekking tot de gehaalde efficiëntie en de kwaliteit van het AC ingangsvermogen. Efficiënties hoger dan 95 % in het grootste gedeelde van het uitgangsvermogensbereik, met een zeer vlakke efficiëntiecurve en dus een hoge efficiëntie in deellast, zijn gehaald. De piek efficiëntie is ongeveer 96 % en de efficiëntie bij nominaal vermogen ongeveer 95.6 %. Bovendien is een vermogensdichtheid van 2 kW/liter bereikt. Een vergelijking met enkele tweetraps prototype systemen gerapporteerd in de literatuur toont dat de bekomen performantie zeer dicht aanleunt bij de absolute state-of-the-art;
- Hoofdstuk 7 besluit het voorgestelde werk en biedt een kijk op het toekomstige onderzoek in het domein van DAB AC–DC omvormers.

Voorwoord

In januari 2009 begon ik aan mijn doctoraatsonderzoek bij ELECTA. Als, tot dan toe, één van de enige industrieel ingenieurs binnen de groep voelde ik mij de eerste dagen en weken een beetje onwennig tussen al die 'burgies'. Ik had het gevoel dat ik, vooral op theoretisch vlak, een achterstand moest goedmaken en stortte mij dan ook met volle overgave op mijn werk. In het prille begin ervaarde ik dit als een opgave maar gaandeweg evolueerde dit gevoel naar een echte passie voor vermogenelektronica, en al snel werden de elektronische componenten en circuits, die eerst zo onvertrouwd leken, een deel van mijn leven. Met veel plezier spendeerde ik vele uren, dagen, weekends, en feestdagen op mijn bureau en in het labo, hetgeen uiteindelijk resulteerde in deze doctoraatstekst. Uiteraard ging dit niet altijd over een leien dakje en daarom wil ik graag een dankwoordje richten aan de mensen die me gedurende de afgelopen jaren hebben bijgestaan.

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Jordi Everts
Maart, 2014

List of Designators and Abbreviations

List of Designators

Commonly Used Designators

Symbol	Description
Att	Attenuation (general)
$Att_{\mathrm{Filt}}(j\omega)$	Attenuation characteristic/spectrum of the (DM) EMC input filter
A_{c}	Effective core cross section
B	Flux density (general)
B_{sat}	Saturation flux density
B_w	Control bandwidth
C	Capacitance (general)
C_1	HF filter capacitance (input side of the DAB)
C_2	HF filter capacitance (output side of the DAB)
$C_{2,\mathrm{st}}$	LF filter capacitance (output side of the DAB)
C_{GD}	Gate to drain capacitance of a MOSFET
C_{GS}	Gate to source capacitance of a MOSFET
C_{DS}	Drain to source capacitance of a MOSFET
C_{oss}	Output capacitance of a MOSFET ($= C_{\mathrm{GD}} + C_{\mathrm{DS}}$)
C_{leg}	Total parasitic capacitance of a bridge leg
D_{ctr}	Duty-cycle counter
d	Primary side referred voltage conversion ratio
dir	Power flow direction
f	Frequency (general)
f_{L}	Line frequency

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Symbol	Description
f_s	Switching frequency
f_ctr	Frequency counter
f_cutoff	Cut-off frequency
f_pack	Packing factor
H	Magnetic field (general)
i	Instantaneous current (general)
i_AC	Instantaneous grid current
I_AC	RMS value of the grid current
$I_\mathrm{AC,P}$	RMS value of the active component of the grid current
$\hat{I}_\mathrm{AC,P}$	Amplitude value of the active component of the grid current
i_1	Instantaneous DAB input current (non-filtered)
i_2	Instantaneous DAB output current (non-filtered)
I_DAB1	DAB input current (averaged over T_s and quasi constant)
I_DAB2	DAB output current (averaged over T_s and quasi constant)
i_DAB1	DAB input current (averaged over T_s and highly variable)
i_DAB2	DAB output current (averaged over T_s and highly variable)
i_{C_1}	Instantaneous current in HF filter capacitance C_1
i_{C_2}	Instantaneous current in HF filter capacitance C_2
$i_\mathrm{R,o}$	Instantaneous output current of the synchronous rectifier or the PFC rectifier, i.e. the input port current of the DAB ($= i_\mathrm{DAB1} + i_{\mathrm{C}_1}$)
$i_\mathrm{R,i}$	Instantaneous input current of the synchronous rectifier or the PFC rectifier
i_DC2	Instantaneous output port current of the DAB ($= i_\mathrm{DAB2} - i_{\mathrm{C}_2}$)
i_HF1	Instantaneous primary side HF AC-link current (bridge current)
I_HF1	Local (i.e. regarding a switching period T_s) RMS value of the primary side HF AC-link current (bridge current)
i_HF2	Instantaneous secondary side HF AC-link current (bridge current)
I_HF2	Local (i.e. regarding a switching period T_s) RMS value of the secondary side HF AC-link current (bridge current)
i_L	Instantaneous current in an inductance (general) / Instantaneous current in the equivalent HF AC-link inductance L
I_L	Local (i.e. regarding a switching period T_s) RMS value of the current in the equivalent HF AC-link inductance L
$i_{\mathrm{L}_\mathrm{c}}$	Instantaneous current in a commutation inductance
i_leg	Instantaneous leg current

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Symbol	Description
i_{C}	Instantaneous current in a capacitance (general)
i_{D}	Instantaneous current in a diode (general)
i_{T}	Instantaneous current in a transistor (general)
i_{S}	Instantaneous current in a switch (general)
I_{S}	Local (i.e. regarding a switching period T_{s}) RMS value of the current in a switch
i_{DS}	Instantaneous drain to source current of a MOSFET
I_{D}	Continuous drain to source current of a MOSFET
$I_{\mathrm{p,comm}}$	Primary side commutation current
$I_{\mathrm{s,comm}}$	Secondary side commutation current
L	Inductance (general) / Equivalent HF AC-link inductance
L_{ext}	Inductance value of the external series inductor
L_{c}	Commutation inductance
L_{M}	Magnetizing inductance of a transformer
L_{tr}	Leakage inductance of a transformer
L_{mains}	Mains inductance
l_{g}	Air gap length
$Lim_{\mathrm{B}}(j\omega)$	Spectrum of the CISPR 22 Class B limit for conducted emission
n_1	Number of turns of the primary side winding of a transformer
n_2	Number of turns of the secondary side winding of a transformer
n_1/n_2	Turns ratio of a transformer
n_{ind}	Number of turns of an inductor (general)
PF	(True) power factor
P	Average AC port power (> 0 for power transfer from the AC port to the DC port)
p	Instantaneous power (general)
P_1	DAB input power (averaged over T_{s} and quasi constant)
P_2	DAB output power (averaged over T_{s} and quasi constant)
p_1	DAB input power (averaged over T_{s} and highly variable)
p_2	DAB output power (averaged over T_{s} and highly variable)
p_{X}	Instantaneous power losses in a component 'X'
P_{X}	Average (i.e. averaged over a line cycle T_{L}) power losses in a component 'X'
P_{cond}	Average (i.e. averaged over a line cycle T_{L}) conduction losses
P_{g}	Average (i.e. averaged over a line cycle T_{L}) gate drive losses

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Symbol	Description
$P_{\mathrm{S,cond}}$	Average (i.e. averaged over a line cycle T_{L}) conduction losses of a single MOSFET
$P_{\mathrm{S,g}}$	Average (i.e. averaged over a line cycle T_{L}) gate drive losses of a single MOSFET
P_{S}	Average (i.e. averaged over a line cycle T_{L}) total losses of a single MOSFET
Q_{g}	Total (typical) gate charge of a single MOSFET
Q_{comm}	Commutation charge (related to the complete commutation of a bridge leg)
Q_{A}	Commutation charge (related to the first half of the commutation of a bridge leg)
Q_{B}	Commutation charge (related to the second half of the commutation of a bridge leg)
R	Resistance (general)
$R_{\mathrm{DS(on)}}$	Drain to source on-resistance of a MOSFET
R_{th}	Thermal resistance (general)
R_{m}	Reluctance (general)
$R_{\mathrm{m,core}}$	Core reluctance
$R_{\mathrm{m,air}}$	Air gap reluctance
st_{leg}	State of a bridge leg
st_{SR}	State of the synchronous rectifier
$s^{\pm}$	Multiplier
T_{L}	Line period, $T_{\mathrm{L}} = 1/f_{\mathrm{L}}$
T_{s}	Switching period, $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$
T_{ctr}	Timing counter
v	Instantaneous voltage (general)
v_{AC}	Instantaneous grid voltage
V_{AC}	RMS value of the grid voltage
$\hat{V}_{\mathrm{AC}}$	Amplitude value of the grid voltage
V_{DC1}	DAB input voltage (quasi constant)
V_{DC2}	DAB output voltage (quasi constant)
v_{DC1}	DAB input voltage (highly variable)
v_{DC2}	DAB output voltage (highly variable)
v_{HF1}	Instantaneous primary side HF AC-link terminal voltage
v_{HF2}	Instantaneous secondary side HF AC-link terminal voltage

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Symbol	Description
v_{L}	Instantaneous voltage across equivalent HF AC-link inductance L
v_{DS}	Instantaneous drain to source voltage of a MOSFET
v_{GS}	Instantaneous gate to source voltage of a MOSFET
V_{GS}	Gate to source voltage during the on-state or during the off-state of a MOSFET
v_{C}	Instantaneous voltage across a capacitance (general)
V	Component volume (general)
$V_{\mathrm{F}}(j\omega)$	Spectrum of the video-filtered quasi-peak values at the output of the EMC test receiver
v_{meas}	Voltage at the LISN output
ω	Angular frequency (general), $\omega = 2\,\pi\,f$
ω_{L}	Angular line frequency, $\omega_{\mathrm{L}} = 2\,\pi\,f_{\mathrm{L}}$
ω_{s}	Angular switching frequency, $\omega_{\mathrm{s}} = 2\,\pi\,f_{\mathrm{s}}$
ϕ	Phase-shift angle
τ_1	Pulse-width modulation angle of the primary side HF AC-link terminal voltage v_{HF1}
τ_2	Pulse-width modulation angle of the secondary side HF AC-link terminal voltage v_{HF2}
t_{dead}	Dead time
$t_{\mathrm{sw,del}}$	Switching delay
T_{J}	Junction temperature
T_{Am}	Ambient temperature
η	Efficiency (general)
η_{gd}	Efficiency of the gate drive units
ρ	Power density (general)

Subscripts

x_{av}	Available value of x
$x_{\mathrm{av,p}}$	Available value of x, regarding the DAB's primary side active bridge
$x_{\mathrm{av,s}}$	Available value of x, regarding the DAB's secondary side active bridge
x_{crit}	Critical value of x
x_{eq}	Equivalent value of x

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Symbol	Description
x_{init}	Initial value of x
x_{l}	Lower value of x
x_{m}	Measured value of x
x_{max}	Maximum value of x
x_{min}	Minimum value of x
x_{nom}	Nominal value of x
x_{norm}	Normalized value of x
x_{opt}	Optimal value of x
x_{pre}	Predefined value of x
x_{ref}	Reference value of x
x_{req}	Required value of x
$x_{\mathrm{req,p}}$	Required value of x, regarding the DAB's primary side active bridge
$x_{\mathrm{req,s}}$	Required value of x, regarding the DAB's secondary side active bridge
x_{set}	Set value of x
x_{u}	Upper value of x
$\mathbf{x}$	Vector of variables x
	Principle Notation
$\hat{x}$	Amplitude value or peak value of x
$\tilde{x}$	LF AC ripple component of x
X	RMS value of x
x'	Quantity x referred to the primary side of a transformer
x^*	Set value of x

Chapter/Section Specific Designators

Symbol	Description
	Chapter 1: Introduction
	Section 1.1.4: The Necessity of Multi-Objective Optimization (MOO)
p	Performance Index
$\mathbf{p}$	Vector of Performance Indices p
x	Design variable
$\mathbf{x}$	Vector of design variables x
k	Design constant (e.g. the saturation flux density)
$\mathbf{k}$	Vector of design constants k
r	System specification and/or operating requirement
$\mathbf{r}$	Vector of system specifications and/or operating requirements r
g	Side condition: inner converter function
h	Side condition: minimum requirement function
a	Probability density
w	Weighting factor
	Chapter 4: ZVS Modulation Schemes
	Section 4.1.1: Constrained Nonlinear Optimization Procedure
$\mathbf{h}$	Vector of circuit level variables (L, L_{c1}, L_{c2}, and n_1/n_2)
$\mathbf{x}$	Vector of independent variables (ϕ, τ_1, τ_2, and f_{s})
$c_{\mathrm{eq}}(\mathbf{x})$	Nonlinear function of $\mathbf{x}$, describing the dependency of i_{DAB1} on $\mathbf{x}$
$c(\mathbf{x})$	Nonlinear function of $\mathbf{x}$, describing the ZVS conditions
$\mathbf{l_b}$	Vector of lower bounds, describing the physical limitations on $\mathbf{x}$
$\mathbf{u_b}$	Vector of upper bounds, describing the physical limitations on $\mathbf{x}$
A	Matrix of mode boundary coefficients
$\mathbf{b}$	Vector of mode boundary constants
$f_{\mathrm{cost}}(\mathbf{x})$	Cost/objective function (to be minimized)
EF	Exit flag

List of Abbreviations

Abbreviation	Description
1-S	Single-Stage
2-S	Dual-Stage
AC	Alternating Current
BCM	Boundary Conduction Mode
BEV	Battery Electric Vehicle
CB	Current-Based
CCM	Continuous Conduction Mode
CDCB	Current-Dependent Charge-Based
CE	Conducted Emission
CHP	Combined Heat and Power
CM	Common Mode
CSPI	Cooling System Performance Index
DAB	Dual Active Bridge
DC	Direct Current
DES	Distributed Energy Source
DG	Distributed Generator (Generation)
DM	Differential Mode
DR	Demand Response
EB	Energy-Based
EGCI	European Green Cars Initiative
ELCO	Electrolytic Capacitor
EM	Electric Machine (motor/generator)
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EU	European Union
EV	Electric Vehicle
EVSE	Electric Vehicle Supply Equipment
FB	Full Bridge
FC	Fuel Cell
FCV	Fuel Cell Vehicle
GHG	Greenhouse Gas

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Abbreviation	Description
GWP	Global Warming Potential
HB	Half Bridge
HDAB	Hybrid Dual Active Bridge
HEV	Hybrid Electric Vehicle
HF	High Frequency
HV	High Voltage
ICE	Internal Combustion Engine
ICEV	Internal Combustion Engine Vehicle
IEC	International Electrotechnical Commission
iGSE	improved Generalized Steinmetz Equation
i^2GSE	improved improved Generalized Steinmetz Equation
IGBT	Insulated Gate Bipolar Transistor
LF	Low Frequency
LISN	Line Impedance Stabilization Network
LV	Low Voltage
MOO	Multi-Objective Optimization
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PCC	Point of Common Coupling
PE	Protective Earth
PEMFC	Proton Exchange Membrane Fuel Cell
PEV	Plug-in Electric Vehicle
PF	Power Factor
PFC	Power Factor Correction
PFCV	Plug-in Fuel Cell Vehicle
PHEV	Plug-in Hybrid Electric Vehicle
PV	Photovoltaic
PWM	Pulse-Width Modulation
QP	Quasi-Peak
RES	Renewable Energy Source
RTT	Real-Time Target
RBW	Resolution Bandwidth
SAE	Society of Automotive Engineers
SOFC	Solid Oxide Fuel Cell

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Abbreviation	**Description**
SR	Synchronous Rectifier
STS	Static Transfer Switch
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
UNFCCC	United Nations Framework Convention on Climate Change
UPF	Unity Power Factor
V2G	Vehicle-to-Grid
ZEV	Zero Emission Vehicle
ZVS	Zero Voltage Switching

Contents

1

Introduction

First, the evolution of the electricity grid toward a 'smart grid' and the increasing need for higher energy efficiency in the conservation of resources is summarized, supported with facts and figures. Thereafter, a general impression of the role that power electronics will play in future electricity grids and the technological developments that are feasible to meet the requirements of future power electronic systems is given. In this context, the essence of mathematical modeling and subsequent multi-objective optimization of converter systems is emphasized. As this work investigates a particular single-phase, bidirectional, and isolated AC–DC converter that is interfaced with the low voltage (230 V_{AC} – 50 Hz) utility grid, the focus is on power electronic systems that are connected with the electricity grid on the distribution/residential level. There, bidirectional conversion capability is a key feature in the development of a smart interactive power network ('smart grid'). Subsequently, an overview of the main application areas and the corresponding system level requirements for these types of grid-tied converters is provided from which the specifications for the investigated AC–DC converter are derived. Lastly, the selection of the (single-stage, 1-S) dual active bridge (DAB) AC–DC converter topology for the realization of the above AC–DC conversions is motivated and the objectives as well as the new contributions of the work are highlighted.

1.1 General Trends

Worldwide, energy policies are more than ever looking in the same direction, heading for a common goal: offer a secure supply of energy at affordable prices to the citizens and companies and in the meanwhile reduce the negative environmental effects of energy use [1, 2]. Energy remains a major component of the economic growth, and thus of the growth, the stability and the well-being of citizens. Therefore, energy research within the context of sustainable development is mainly driven by these three elements, linking economic development, protection of the environment and social justice [3]. Providing the essential energy services to meet the human needs while understanding and addressing the environmental consequences associated with the use of energy is perhaps the biggest challenge ever faced by mankind. This challenge will become even more prominent in the coming decades as the world energy consumption is expected to grow by 53% from 505 quadrillion[1] Btu[2] in 2008 to 770 quadrillion Btu in 2035 (see Figure 1.1) [4]. This strong increase is mainly the result of robust economic growth and expanding world populations.

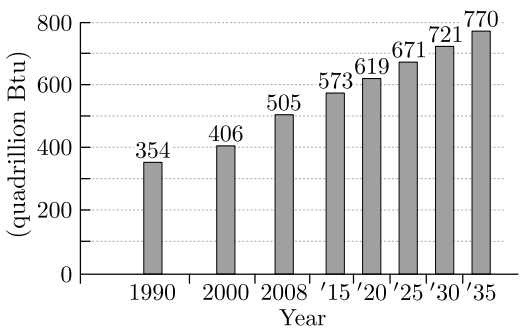


Figure 1.1: World energy consumption, 1990–2035. Source: [4]

One of the most prominent illustrations of the worldwide commitment for addressing the negative environmental effects of energy use is the Kyoto Protocol [5] which is an international agreement linked to the United Nations Framework Convention on Climate Change (UNFCCC) that sets mandatory targets on anthropogenic greenhouse gas[3] (GHG) emissions for the world's leading economies. The Kyoto Protocol is adopted in Kyoto, Japan, on 11 December 1997 and entered into force on

[1] One quadrillion: $1,000,000,000,000,000$; one thousand million million; 10^{15}; SI prefix: peta (P).

[2] The British thermal unit (symbol Btu or sometimes BTU) is a traditional unit of energy and is equal to about 1055 joules. It is the amount of energy needed to heat one pound of water by one degree Fahrenheit.

[3] Greenhouse gases (GHGs) are gases in the atmosphere (water vapor, carbon dioxide, nitrous oxide, ozone, methane,...) that trap heat energy – most of this heat energy directly comes from

16 February 2005. For the first commitment period (2008-2012), 37 industrialized countries and the European Community agreed on a reduction of GHG emissions to an average of five percent against 1990 levels. For the second commitment period (2013-2020), involving a different composition of parties, the goal is to reduce GHG emissions by at least 18 percent below 1990 levels. The 20-20-20 targets set by the European Union (EU) are one of the noticeable policies that indicate the EU's determination to meet these ambitious climate objectives. The targets aim at a 20 % reduction in EU greenhouse gas emissions compared to 1990 levels, a 20 % increase of the share of the EU's energy consumption produced from renewable resources, and a 20 % improvement in the EU's energy efficiency. In the coming decades even more stringent reductions on GHG emissions are to be expected, heading towards a decarbonization of the energy system. A number of scenarios investigated in the EU Energy Roadmap 2050 indicate an 85 % decline of energy-related CO_2 (carbon dioxide) emissions by the year 2050 [7, 8].

1.1.1 Sustainable Electric Energy Production and Consumption

As it has for the past several decades, electricity is the world's fastest growing form of end use energy consumption. Worldwide, electricity generation is expected to increase by 84 % from 19.1 trillion[4] kWh in 2008 to 35.2 trillion kWh in 2035 (see Figure 1.2) [4]. This means a rise by 2.3 % per year on average, while the total energy demand grows by an annual average of 1.6 % (see Figure 1.3). The rising need for reducing the negative environmental effects of energy use implies in the first place that more effort must be put in reducing energy consumption and wastage, for example by setting minimum energy efficiency standards and rules

the sun – in the Earth's atmosphere [6]. The atmospheric concentration of GHGs affects the temperature of the Earth and has an impact on global warming.

[4]One trillion: $1,000,000,000,000$; one million million; 10^{12}; SI prefix: tera (T).

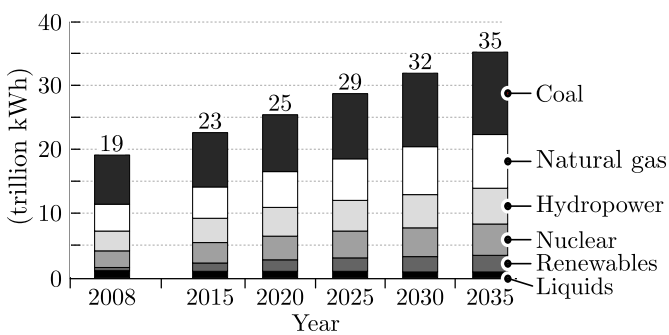


Figure 1.2: World net electricity generation by fuel type, 2008–2035. Source: [4]

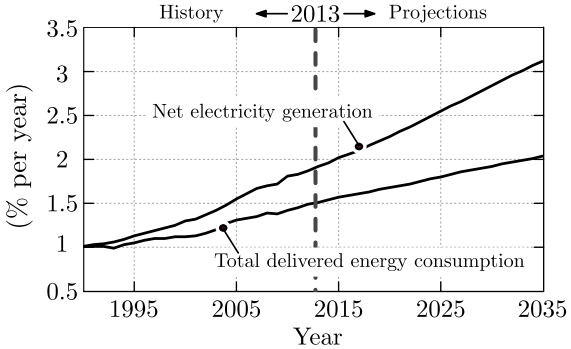


Figure 1.3: Growth in world electricity generation and total delivered energy consumption, 1990–2035 (index, 1990 = 1). Source: [4]

on labeling for products, services and infrastructure [3]. Contrary to the electric power systems developed in the last century, providing carbon and nuclear-based electricity, new energy systems that effectively reduce or completely eliminate emissions and nuclear waste are needed to make clean and sustainable power available. In the meanwhile the reliability, quality and security of the electricity supply need to be assured while the efficiency of the energy conversion (both at the load and generation side) needs to be increased, resulting in a more sustainable electric power system. These goals can be achieved by reducing the dependence on imported fuels (mostly fossil and nuclear) and exploiting renewable energy sources, resulting in a decentralization of the energy conversion and electricity production [3, 9]. Today, government policies and incentives throughout the world support the rapid construction of renewable electricity generation facilities (e.g. hydro, wind, solar, ... - power). As a result, renewable generation is the world's fastest growing source of electric power, rising at an average annual rate of 3 % and outpacing the average annual increases for natural gas (2.6 %), nuclear power (2.4 %), and coal (1.9 %) [4]. The renewable share of global electricity generation is expected to increases from 19 % in 2008 to 23 % in 2035. However, reaching the EU 20-20-20 targets implies a share of approximately 34 % of renewables in the overall European electricity generation [10].

1.1.2 Evolution of the Electricity Grid: Smart Grids

The aim toward a low-carbon economy and complete carbon-neutrality for the power sector has an impact on the way the electric power system will be redesigned and reinforced in the coming decades [11]. The traditional model with large centrally dispatched remote power stations, long transmission lines, and a distribution system primarily designed to deliver power from transmission substations to load centers

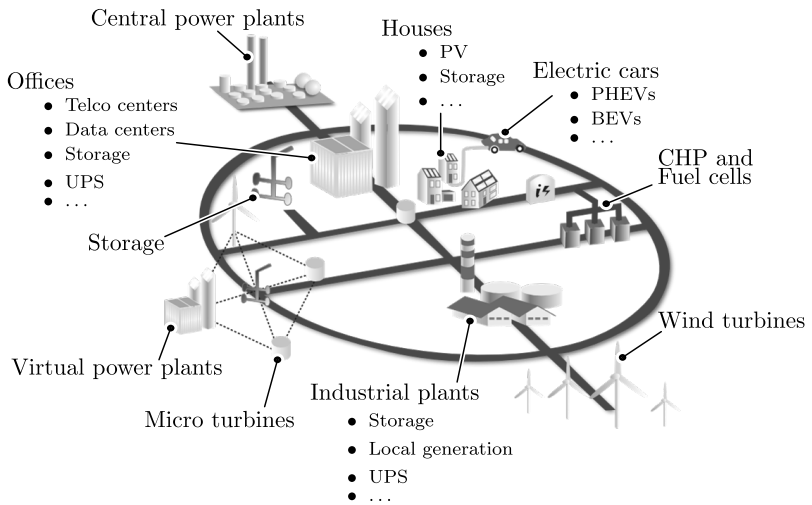


Figure 1.4: Future electricity grid ('smart grid'), an interactive service network with large-scale deployment and effective integration of distributed and renewable energy sources.

is evolving towards a 'smart' energy network, an interactive service network (with customers and operators) where large-scale deployment and effective integration of distributed and renewable energy sources is possible (see Figure 1.4). Along the way, major technical challenges will have to be faced in order to assure environmental compliance, energy conservation, grid reliability, improved operational efficiencies and customer services [1, 3, 9].

On the distribution and residential level, the transformation of the electric power system will accommodate generation closer to the loads, storage facilities, plug-in hybrid electric vehicles (PHEVs), battery electric vehicles (BEVs), and greater levels of demand side management (e.g. demand response (DR)) [9]. Today, the main contributors to the decentralized electricity production are wind power and hydroelectricity [4]. They reach a competitive level with traditional forms of energy generation. The contribution of photovoltaics (PV) and micro-turbines is still low but increasing. Similarly the amount of (electric) energy storage systems and (hybrid) electric vehicles ((H)EVs) is still limited. However, in the near future, a massive integration into the low voltage distribution grid of small scale distributed generators (DGs) is forecasted [12], with storage systems, PHEVs, and BEVs complementing these energy generation units. In order to maintain and further enable this increasing penetration into the electricity grid, system costs need to be further reduced while the efficiency and reliability of the systems need to be improved.

1.1.3 The Role of Power Electronics in Future Energy Networks (Smart Grids)

As explained in the previous sections, the current electricity grid is evolving from a rather passive to a interactive energy network. Power electronics can be seen as key enabling technologies for the realization of these 'smart grids' where high power quality and security of supply/service are one of the main objectives [12, 13]. Most of the distributed energy sources (DESs) use a power electronic converter to interconnect to the grid. Moreover, almost every electric load comprises a power electronic circuit/converter. This means that a large fraction of the total generated electric energy (see section 1.1.1) is converted and conditioned by power electronic systems (on the generation as well as on the load side). For economic and environmental reasons it is very important that these energy conversions take place at the highest possible efficiency. The decentralized energy sources (wind, sun, water, ...) do not have the high energy densities of the ones in central production units (e.g. uranium in a nuclear plant). Also, their availability is variable in time, often resulting in a partial load condition for the energy conversion systems. Thus, considering the low generation efficiency, the energy efficiency of power electronic converters will gain eminent importance in the conservation of resources. Besides efficiency, other important improvements can still be made to address the requested demands on reliability, cost, power quality, controllability, power density, ... The focus of this work is on power electronic systems that are connected with the electricity grid on the distribution/residential level where a large penetration of power electronics is expected to happen within the next 25-30 years [13, 14]. The main transmission grid will be affected to a lesser extent [9, 14] and the power electronics development will primarily be in the distributed generation units and in the loads [14].

In addition to their interfacing function, power electronics allow the implementation of decentralized control schemes for the DESs and can add several possibilities to improve the overall power quality of the electric energy supply system [12, 15]. Voltage support, active filtering, harmonic suppression, phase balancing and frequency support are some important examples. Thereby it is desirable to strive for a modular structure in which expansion is possible without additional system adaptations, resulting in a universal connectivity and operability. Below, the general system-level features and requirements for power electronics in future energy networks (smart grids) are summarized [3].

Distributed Intelligent Control— The traditional central control philosophy will shift to a more distributed control paradigm where DESs become active elements of the energy system. The emphasis is now on integrating instead of connecting DESs into the overall system. Distributed intelligent control is necessary to make this shift possible and power electronics can be the key enablers of this new control strategy [12, 15].

Efficiency and System Cost— To maintain and increase the further spread of DESs into the utility grid, it is important to decrease the cost and at the same time improve the efficiency and reliability of these systems. Power electronic converters play a key role in this process as they account for a significant portion of the total system efficiency and cost (photovoltaic converters for example account for approximately 15-25 % of the system cost). In addition they are still a bottleneck for system reliability. Hence it is important to have a close look at the power electronic side of the distributed generation, where valuable improvements can be made. Energy losses do not only account for economic losses, but also aggravate the problem of heat removal.

Reliability, Safety/Security and Quality of Power— These are the main technical issues that emerge from the large-scale deployment of DESs. To tackle these rising difficulties, major technological and regulatory changes are required. Future power electronics can deliver a huge contribution to the implementation of most of the technological solutions that are needed (operation, protection, control, ...). Below, it is briefly explained what the terms 'security', 'reliability' and 'quality' of power actually mean [3].

- **Security**: the ability of the system to remain in operation after sudden disturbances that may occur, like short circuits, loss of equipment, ... It may take into account any actions causing such disturbances, such as human errors, extreme weather conditions, terrorist activity, ...;
- **Reliability**: the ability of the system to satisfy customer requirements in terms of power and energy, considering forced outages, and the scheduled maintenance outages of the system's equipment;
- **Quality**: power quality deals with the phenomena of various deviations in voltage or current waveforms and/or shifts in phases. These deviations can result in failure or malfunctioning of customer equipment.

Reliability and *security* of power are issues that are in the first place related to the global design and control of the power system. Nowadays the responsibility for a secure system operation is in the hands of the conventional power plants and system operators. In future smart grids, DESs can take over a part of this responsibility and provide the flexibility and controllability that are needed to support secure system operation. Hereby, power electronics are often seen as no more than the enabling components for the needed distributed control strategies. However, current operating strategies ensure the immediate disconnection of the DES in case of a disturbance.

Power quality in future smart grids is seen as an issue whereby power electronics can play an active and direct role in guaranteeing it to be within the norms/standards. The quality of the voltage is the most important aspect of power quality. This can

be both steady state variations or disturbances. Steady state variations include voltage regulation, harmonic distortion and flicker, while disturbances are transients, voltage dips and voltage swells. All these phenomena can lead to interruptions of the power supply, having a negative impact on the reliability of the whole system.

1.1.4 The Necessity of Multi-Objective Optimization (MOO)

In the design of power electronic converters, there is a historical trend toward lower volume and/or higher power density. This trend is mainly driven by the general requirement for decreasing the functional system volume and cost [16]. Moreover, due the aforementioned environmental issues, efficiency maximization of converter systems is a major concern. Consequently, for the design of a power electronic converter, typically multiple objectives need to be considered. Thereby, most prominent are:

- Minimization of the volume and thus maximization of the power density;
- Minimization of the weight;
- Minimization of the losses and thus maximization of the efficiency;
- Minimization of the costs;
- Minimization of the failure rate and thus maximization of the reliability.

These objectives can be translated into a set of mutually coupled and measurable 'Performance Indices' which enable the implementation of a quantitative plan of action in order to achieve technological and market economy goals for the further development of power electronic converters [17]. Figure 1.5 depicts the fundamental trends regarding the main Performance Indices involved in the design of power electronic systems.

At present, the definition and quantification of future performance targets, for example in the course of roadmapping, are strongly based upon the experience of development engineers and the extrapolation of earlier product generations. The same goes for the further improvement of converter designs, which relates in particular to the right topology selection and the choice of the component values and operating parameters. One of the main deficiencies of this traditional approach is that it is generally not checked whether a desired target performance is fundamentally achievable with a given technological base [17]. Therefore it is a rising trend to replace this evolutionary process by a mathematical procedure in which the relationship between the technological base and the performance of the system exists as a comprehensive mathematical representation whose optimization

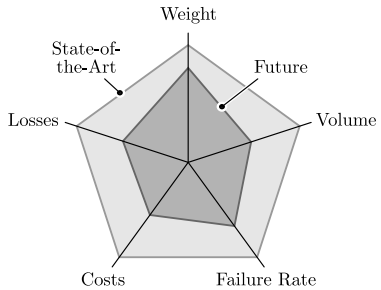


Figure 1.5: Representation of the main, state-of-the-art and required (future), Performance Indices involved in the design of power electronic systems [17].

(i.e. by means of multi-objective optimization (MOO)) assures the best possible exploitation of the available degrees of freedom and technologies [17].

The mathematical MOO procedure [17] makes abstraction of the realization of a power electronic system and thereby maps a multi-dimensional Design Space (Decision Space) into a multi-dimensional Performance Space (Objective Space), which is defined by the different Performance Indices p_i (see Figure 1.6). In Figure 1.6, vector $\mathbf{x}$ are the free design parameters, vector $\mathbf{k}$ the design constants (e.g. the permeability and saturation flux density of the considered magnetic materials), and vector $\mathbf{r}$ the system specifications and operating requirements (e.g. the input and output voltage, the output power, the electromagnetic compatibility (EMC) requirements, etc.). Each point in the multi-dimensional Design Space defined by $\mathbf{x}$ and $\mathbf{k}$, represents a single converter design, having a certain performance $\mathbf{p}$ which is determined by calculation of the different Performance Indices,

$$p_\mathrm{i} = f_\mathrm{i}(\mathbf{x}, \mathbf{k}). \tag{1.1}$$

Thereby a set of inner converter functions g_k is defined which reflect the physical behavior of the main functional elements of the converter system as well as their interaction, as determined by the circuit topology and mechanical construction:

$$g_\mathrm{k}(\mathbf{x}, \mathbf{k}, \mathbf{r}) = 0 \qquad k = 1, 2, 3, \ldots, p. \tag{1.2}$$

The desired system specifications are then formulated as a set of minimum requirements:

$$h_\mathrm{j}(\mathbf{x}, \mathbf{k}, \mathbf{r}) \geqslant 0 \qquad j = 1, 2, 3, \ldots, q. \tag{1.3}$$

Both g_k and h_j are included as side conditions (Condition Map) in the calculation procedure (see Figure 1.6). A probability density a_m can be assigned to the various

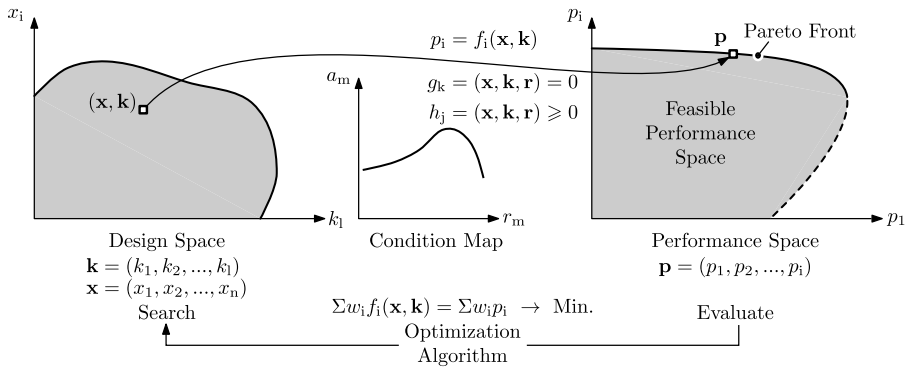


Figure 1.6: Abstract representation of the design and multi-objective optimization of a power electronic converter, where a multi-dimensional Design Space is mapped into a multi-dimensional Performance Space [17] which is bounded by the Pareto Front.

operating points in case the whole profile of the converter is considered in the optimization, resulting in a multi-dimensional Condition Map. From the resulting Performance Space (i.e. a variety of possible designs), the best design with regard to a Performance Index p_i (e.g. minimization of the total converter losses) can be directly found via single-objective optimization:

$$p_i \rightarrow \text{Min.} \tag{1.4}$$

Consequently the result p_i of this single-objective optimization is located on one of the axes of the Performance Space. However, for an industrial design it is desirable to find the best compromise between several competing requirements, e.g. with regard to efficiency (i.e. minimizing the losses) and system costs, which can be obtained using a multi-objective optimization where weighting of the individual performance goals may be applied by appointing a weighting factor w_i to each Performance Index p_i:

$$\sum w_i p_i = \sum w_i f_i(\mathbf{x}, \mathbf{k}) \rightarrow \text{Min.} \tag{1.5}$$

Each weighting factor yields an optimal point in the Design Space to which a point in the Performance Space is allocated. Consequently, different weightings w_i of the individual Performance Indices lead to a multitude of solutions in the Performance Space. These solutions represent the best possible compromise between competing performances, known as the Pareto Front and limiting the feasible Performance Space (see Figure 1.6).

The above mentioned MOO of converter systems (see Figure 1.6) requires that for a given set of specifications, circuit topology, and operating mode, the realization and functioning of the converter system are mathematically described, starting from a given technology base (i.e. the basic materials and components) [17]. However, the complexity of such an optimization might increase rapidly and most probably computer assistance may become unavoidable. Thereby, on-line parameter entry can be provided for the circuit components by means of a circuit simulation, so that an optimization algorithm can vary the values of the design variables until the optimal parameter combination is found. Separation of the partial converter functions can be considered, allowing local optimization loops to be applied to the design of the individual converter components (inductors, capacitors, power semiconductors, heat sinks,...). This results in a simplification of the mathematical description of the system behavior which is based on the relatively loose couplings that exist between the different elements, i.e. when parasitic effects such as wiring inductances, electromagnetic and thermal coupling of components, etc., are neglected. Apart from the circuit structure, solely parameters which depend on the geometry, such as thermal resistances and electromagnetic coupling, as well as temperature dependence of the power semiconductor properties, cause stronger couplings. These couplings, however, can be (partially) accounted for in the local optimization loops. As a result, only the switching frequency f_s and the component values are determined using an outer (global) optimization loop. Figure 1.7 shows an example of a flowchart for the design and local (component level) and global (system level) optimization of a power electronic converter, in particular regarding the optimization of the efficiency and power density. The MOO procedure consists of the following 7 steps (see Figure 1.7):

1. Determination of the converter specifications and application specific requirements;

2. Selection of the converter topology to be designed/optimized;

3. Derivation of the electric power circuit model of the investigated converter topology;

4. Derivation of a suitable modulation strategy/scheme, which might be adapted to optimally achieve the desired converter specifications;

5. Modeling and design of the main functional elements (i.e. the power semiconductors and heat sinks, the inductors/transformer, the capacitors, and the differential mode (DM) and common mode (CM) EMC filter) of the power circuit. The models for the individual components, used to calculate the required Performance Indices (e.g. efficiency and power density), can be applied to perform inner (local) and/or off-line optimizations. Couplings between the individual elements should be included in the corresponding models (e.g. thermal resistances, electromagnetic couplings, ...);

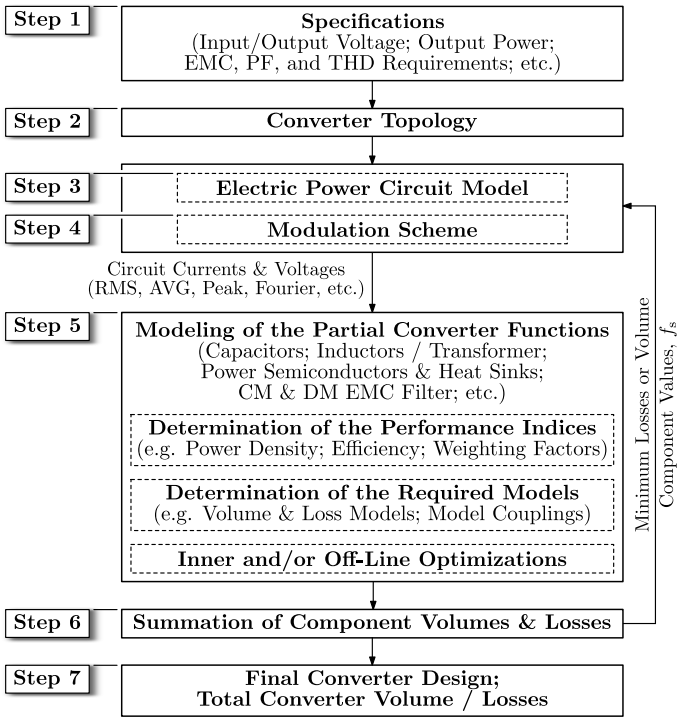


Figure 1.7: Flowchart for the design and the local (component level) and global (system level) optimization of a power electronic converter.

6. Summation of the individually calculated performances of the different converter components and iteration (i.e. using an outer optimization loop) of the component values and the switching frequency f_s in order to find the global optimum;

7. Prototyping, characterization, and testing of the final converter design/implementation.

The mathematically supported design approach (see Figures 1.6 and 1.7) for power electronic converters has been developed in the framework of the 2003 Roadmapping Initiative of the European Center for Power Electronics (ECPE) [18] in order to define the future role of power electronics, and to identify technological barriers and prepare new technologies well ahead in time [17]. A more elaborate and comprehensive discussion/description of the implementation, features, advantages, etc., regarding this approach can be found in [17]. Compared to the traditional experience based design methods, the main advantages are:

- A clear picture of the performance (i.e. by means of the Pareto Front) achievable through individual concepts (i.e. circuit concepts, control concepts, and operating modes) based on state-of-the-art technologies is acquired, enabling the full exploitation of the inherent potential of the technology;
- The state of the technology of a given converter class with reference to the envelope of the Pareto Fronts of various circuit concepts can be determined;
- Physical limits are implicitly taken into account;
- The internal coupling of the Performance Indices of a converter concept can be directly studied. For example, high power densities imply high switching frequencies which potentially lead to a reduced efficiency;
- It can be estimated whether a satisfactory suboptimal solution can be obtained with constant values of the selected design variables (e.g. the parameters related to the magnetic core geometry of inductors and transformers);
- The sensitivity of the system performance with regard to the technological base can be calculated. Therewith the effect of a change in the technology base (e.g. new magnetic materials, new semiconductor devices) on the target Performance Indices can be studied, enabling the effective introduction of new technologies.
- ...

Important to note is that generally, Performance Indices of different power electronic converters can only be used for objective comparison when the systems are similar with regard to the type of energy conversion, the system specifications (i.e. the input and output voltage ranges, power ranges, EMC and PF requirements, etc.), the applied design and optimization methods/procedures, the considered component technologies and cooling concept, etc.

1.2 Applications of Single-Phase, Utility Interfaced, Bidirectional, and Isolated AC–DC Converters

This work investigates a particular single-phase, bidirectional AC–DC converter that is interfaced with the distribution grid on the residential level (i.e. with the 230 V_{AC}, 50 Hz utility grid). Major applications areas for this type of converters are chargers for plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs) [19–21], and interfaces for multiple renewable energy sources (RESs, e.g. photovoltaic (PV) modules [22]) and energy storage systems (ESSs) [23]. Bidirectional conversion capability enables the development of smart interactive power networks in which the energy systems play an active role in providing different types of support to the grid [12, 15]. Examples are vehicle-to-grid (V2G) concepts [24], 'smart home' concepts [25], AC microgrids [12, 15], and residential DC distribution systems (DC nanogrids) [26–28]. In this work only AC–DC converters – in particular a single-stage (1-S) dual active bridge (DAB) AC–DC topology – with galvanic isolation are considered, providing the feasibility of system grounding solutions [26] and thus being advantageous concerning safety issues [29].

1.2.1 Chargers for Plug-in Hybrid Electric Vehicles (PHEVs) and Battery Electric Vehicles (BEVs)

Conventional cars only use internal combustion engines (ICEs) which burn fossil fuels (e.g. petrol, diesel) to generate the required propulsion power. Although internal combustion engine vehicles (ICEVs) have matured over the past 100 years, certainly on the short-term, a continued improvement of the ICEVs will take place, in particular with the aid of automotive electronic technology [30]. However, the excessive burning of fossil fuels not only causes local environmental pollution such as the emission of nitrous oxide (NO_x), carbon monoxide (CO), unburnt hydrocarbons (HCs),... [31], but also partly accounts for global warming, especially due to the exhalation of the nontoxic compound CO_2 (carbon dioxide) into the air[5] [6, 31]. As a result of the more stringent regulations on emissions and fuel economy, global warming, and constraints on energy resources, alternative vehicle concepts with higher potential for further improvement compared to ICEVs have attracted increased attention by car manufacturers, governments, and customers [30]. In particular electric vehicles (EVs), including hybrid electric vehicles (HEVs),

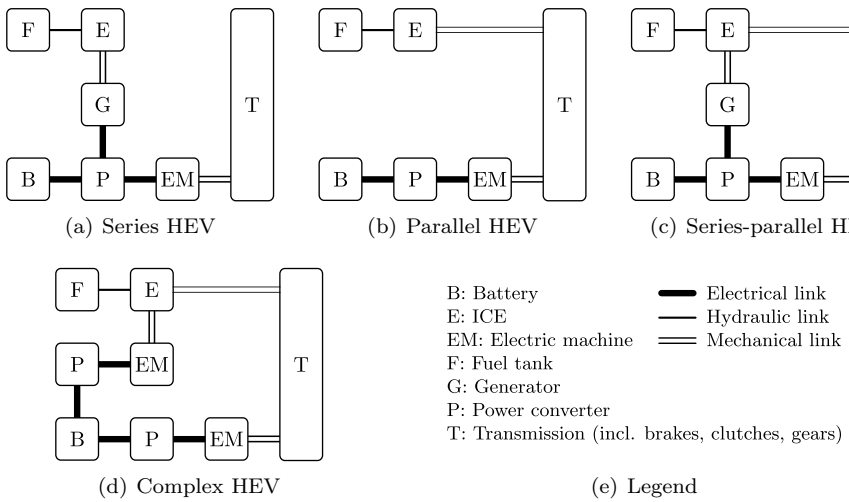
[5] However, water vapor (also a product of the combustion process) is somewhere between 50 % and 300 % as effective as CO_2 on a unit mass basis over a 100 year period [6]. If the global warming potential (GWP) of CO_2 is set at 1, the potential of water is on average about 1.75. Taking into account the global average level of atmospheric water vapor of about 3 % (i.e. 30000 ppmv) compared to a total of about 385 ppmv for CO_2, the total relative warming effect of atmospheric water vapor at the 3 % level is thus about 30000 x 1.75 or 52500 compared to 368 x 1.0 or 368 for CO_2 [6].

battery electric vehicles (BEVs), and fuel cell vehicles (FCVs), will most likely overtake the ICEV monopoly due to their superior fuel economy and performance. All three EV technologies (HEVs, BEVs, and FCVs) can effectively contribute to a lower environmental impact of the ever-increasing use of personal vehicles [30].

Research and development efforts on HEVs, BEVs, and FCVs are driven by different initiatives which have been taken in order to attain a reduction of CO_2 emissions (e.g. the California Zero Emission Vehicle (ZEV) program [32] and the European Green Cars Initiative (EGCI) [33]). Under the EU cars regulation, setting mandatory emission reduction targets, the fleet average to be achieved by all new cars is 130 grams of CO_2 per kilometer (g/km) by 2015 and 95 g/km by 2020. The 2015 and 2020 targets represent reductions of respectively 18 % and 40 % compared with the 2007 fleet average of 158.7 g/km. In terms of fuel consumption, the 2015 target is approximately equivalent to 5.6 liter per 100 km (l/100 km) of petrol or 4.9 l/100 km of diesel. The 2020 target equates to approximately 4.1 l/100 km of petrol or 3.6 l/100 km of diesel. HEVs, BEVs, and FCVs will play an essential role in achieving these goals. However, advanced energy sources and intelligent energy management are key factors to enable EVs competing with ICEVs [30]. Overall cost effectiveness is of course the fundamental factor for marketability of EVs. Below, the different technologies (HEVs, BEVs, and FCVs) are briefly discussed and the role that the investigated single-phase, utility interfaced AC–DC converter, in particular as plug-in battery charger, can play in the context of more electric vehicles (EVs) is highlighted. A summarizing overview and comparison of the main characteristics of HEVs, BEVs, and FCVs can be found in Table 1 of [34].

Hybrid Electric Vehicles (HEVs)

In order to increase the overall system efficiency, HEVs are propelled by an ICE and one or more electric machines (EMs, i.e. an electric motor which also can be used as a generator) in a series, a parallel, a series-parallel, or a 'complex' configuration. Besides the fuel for the ICE, HEVs have thus one or more additional sources of energy (typically electric energy stored in batteries and/or ultracapacitors) on-board the vehicle. The ICE enables an extended driving range while the EMs effectively increase the system efficiency and fuel economy by for example regenerating braking energy and storing excess energy from the ICE in the battery during low load conditions [30, 34, 35]. The latter enables optimization of the ICE operation. Coupled with greater efficiency, the hybrid electric drive train allows for a noticeable improvement of the car's handling and acceleration, being important regarding customer satisfaction [36]. The main concerns of HEVs compared to ICEVs include increased cost due to the introduction of EMs, energy storage elements, and power electronics; reliability and warranty issues; safety concerns due to the presence of high voltages; and electromagnetic interference caused by high-frequency high-current switching in the electric power train [30].



(a) Series HEV (b) Parallel HEV (c) Series-parallel HEV

(d) Complex HEV (e) Legend

Figure 1.8: Four common architectures of HEVs [30].

A first classification (see Figure 1.8) of HEVs can be made with respect to the system architecture and employed drive train [30, 34, 35, 37]:

- **Series HEVs**: in series HEVs (see Figure 1.8(a)), the mechanical output of the ICE is converted into electricity using a generator, after which it either charges the battery or directly propels the wheels via an EM and mechanical transmission. As a result of the decoupling between on the one hand the ICE revolution speed and on the other hand the cruising speed, an optimized operation of the ICE at its best operating point can be achieved. Further advantages are an extended driving range compared to that of a conventional ICEV and a relatively simple drive train with increased flexibility for locating the ICE generator set [30]. However, due to the need for three propulsion devices (the ICE, the generator, and the EM), implying multiple stages of energy conversion, the efficiency of series HEVs is typically lower compared to for example the parallel HEV drive topology [30, 38]. Furthermore, a much higher rated power of the electric system (power electronics, generator, EM) is required [38].
- **Parallel HEVs**: in parallel HEVs (see Figure 1.8(b)) both the ICE and the EM are mechanically connected to the transmission using two clutches. In this way, the propulsion power can be supplied by the ICE alone, by the EM, or by both. The EM can be used as a generator in order to allow regenerative braking and to absorb power from the ICE in case of low load conditions. In both cases energy is transferred to the battery. Advantageous over the series

HEV is the lower number of propulsion devices (i.e. only two propulsion devices: the ICE and the EM) which in turn can have a lower rated power [30]. However, less efficient operation of the ICE is obtained since it's revolution speed depends on the selected gear and the cruising speed [35].

- **Series-parallel HEVs**: the series-parallel HEVs (see Figure 1.8(c)) incorporate the features/advantages of both the series and parallel HEVs. Disadvantageous are the higher complexity and higher cost due to the additional mechanical link compared with the series HEV and the additional generator compared with the parallel HEV [30, 35].
- **Complex HEVs**: complex HEVs (see Figure 1.8(d)) involve complex configurations which cannot be classified into the three categories discussed above. The main difference with the series-parallel HEV is that the complex HEV uses a bidirectional EM that is coupled with the ICE, allowing three propulsion power (due to the ICE and two electric motors) [30]. Again, complex HEVs come with higher complexity and higher cost.

A second classification of HEVs can be made according to the power ratio between the ICE and the EM(s) and the function of the EM(s) [30, 34, 39]:

- **Micro hybrids**: micro HEVs use a limited-power EM which is used as starter-generator system, which allows regenerative braking up to a certain degree, which enables stop-and-go-functionality where the ICE can be stopped when the vehicle is at a standstill, and which can deliver a limited amount of the maximum traction power. This is economically achievable with relatively low system voltages. However, compared to conventional ICEVs, mostly a second battery and a second bus voltage are required (in addition to the existing 12 V battery and the 14 V DC bus) [39]. Fuel economy improvements in the range of 2 % to 10 % are feasible [34].
- **Mild hybrids**: besides the functionalities of the micro hybrids (starter-generator, regenerative braking, stop-and-go), mild HEVs have a boost function, supplementing the ICE's torque, for example during acceleration [34]. The power provided by the electric system is typically in the range of 10 kW to 20 kW, which is too limited to propel the vehicle on its own. Higher supply voltages in the range 100 V to 200 V are applied in order to obtain reasonable currents in the EMs and the converters [30]. Fuel economy improvements in the range of 10 % to 20 % are feasible [34].
- **Full hybrids**: full HEVs have an electric traction system where the electric motor can ensure the vehicle's propulsion on its own (full electric driving). However, propulsion with combined operation of the ICE and the EM or using the ICE only is also possible. Again, starter-generator, regenerative braking,

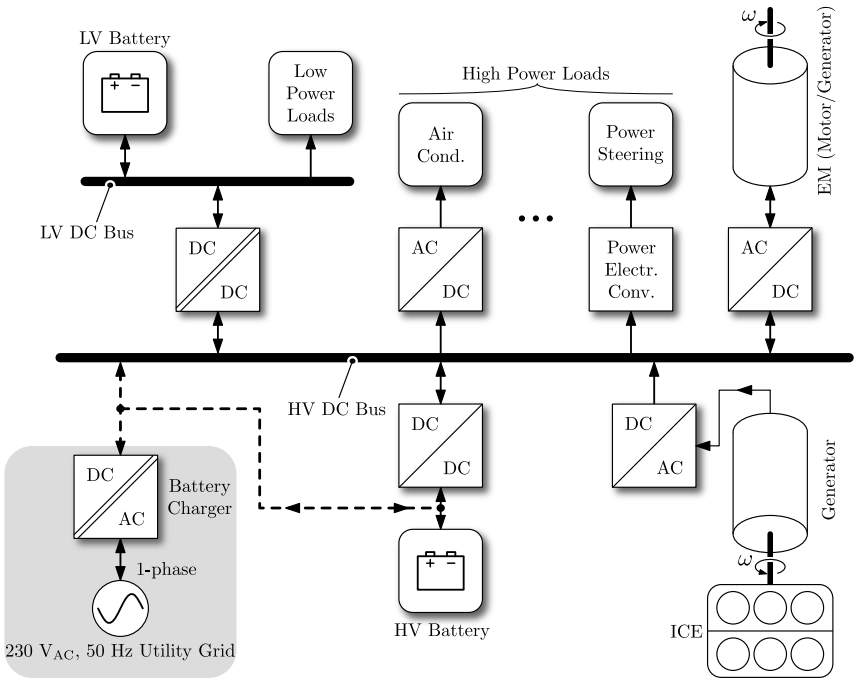


Figure 1.9: Typical series HEV electric power system architecture [35]. The HEV turns into a PHEV in case a utility interfaced battery charger is present [19]. This example shows an on-board, single-phase, bidirectional, isolated battery charger which can either be connected to the HV battery or to the HV DC bus.

stop-and-go functionalities are present. The high required electric power (up to 100 kW and more) demands for comparably high supply voltages, typically in the range of 200 V to 300 V [30] and even up to 800 V [40]. The Lexus GS 450h, for example, uses a 650 V HV DC bus in order to achieve the required EM power with reduced motor and converter currents [30]. Fuel economy improvements in the range of 20 % to 50 % are feasible [34].

A typical electric power system architecture used in a (series) HEV is shown in Figure 1.9 [19, 35]. The high electric load demands of HEVs have resulted in the need to scale up the on-board voltage levels [37, 41]. In order to distribute the electric power, future HEVs – apart from some micro hybrids – require a high voltage[6] (HV) DC bus in addition to the conventional low voltage (LV), 14 V,

[6]In automotive applications voltage levels of more than 60 V are often denoted as 'high voltage' (HV) while voltage levels below 60 V are referred to as 'low voltage' (LV). This classification is made for safety reasons [42].

DC bus to which the low power, low voltage automotive loads (e.g. lighting, instrumentation systems, electric motor driven fans/pumps/compressors,...) are connected [29]. Nowadays, voltage levels of 200 V to 300 V [30, 41] and even up to 600 V [19, 29] for the HV DC bus are rather common (e.g. a DC bus voltage level of 650 V is used for the Lexus GS 450h [30]). It can be assumed that a dual voltage (HV and LV DC bus) automotive power system will exist at least for a while since the low power loads are designed based on the 14 V standards [29, 37]. Thus, the 12 V LV battery will remain in order to provide backup to the electric power supply of the 14 V bus [39]. The HV DC bus primarily enables efficient power transfer between the main electrical energy storage element (mostly a HV battery) and the electric propulsion system (i.e. the EMs) [19]. Besides the bidirectional DC–AC converter(s), connecting the HV DC bus with the EM(s), most of the HEV concepts comprise further power electronic subsystems which are coupled to the HV DC bus like for example a (bidirectional [29, 39]) low power DC–DC converter for supplying the LV power net (as a replacement of the traditional 14 V generator), a bidirectional high power DC–DC converter for boosting the voltage of the HV battery to a higher (stabilized) level required for the HV DC bus (i.e. the HV battery interface), an inverter for the air conditioning system,... [19]. For safety reasons, the HV DC bus needs to be galvanically isolated from the 14 V DC bus and the vehicle chassis. Therefore the interfacing DC–DC converter requires a galvanic isolation [29, 40].

Plug-in Hybrids (PHEVs)— Plug-in HEVs (PHEVs) are able to externally charge the HV battery by plugging into the electricity grid (i.e. the low voltage distribution grid; utility grid), for example using a single-phase AC–DC converter (battery charger) as grid interface (see Figure 1.9) [34]. PHEVs use no fossil fuel during their all-electric range, resulting in zero emission operation. In case the batteries are charged from renewable electricity (e.g. wind, solar, ...), a substantial reduction of GHG emissions is achieved compared to regular gas station refueling HEVs and the fuel economy can be improved by 100 % when the ICE is not used to charge the battery, for example in urban drive cycles [34]. Moreover, the power flow of the grid interface can be bidirectional, so vehicles can not only charge but also discharge and thus inject energy into the grid. This vehicle-to-grid (V2G) option enables provision of different grid support services [15, 24]. The total fleet of PHEVs represents a substantial energy storage capability. At any given time, a high number of these vehicles are available for V2G [24]. As a result, the introduction of plug-in vehicles presents numerous small distributed energy storage elements, enabling the implementation of for example peak shaving, voltage control, and the integration of renewable energy sources into the grid [23, 24]. This leads to an improved grid efficiency and reliability. Due to limited oil reserves and increasing oil prices, PHEVs will attract more and more attention in the coming years.

Plug-in Battery Chargers— Chargers for PHEVs can be subdivided into two main classes: conductive chargers and inductive chargers [29]:

- **Conductive chargers:** the power flow takes place through metal-to-metal contact between on the one hand the connector on the charge port of the vehicle and on the other hand the AC mains power lines or a dedicated electric vehicle supply equipment (EVSE, i.e. a charging station) that is connected to the AC supply network (utility grid). When the AC–DC conversion takes place within the EV, an on-board charger (i.e. an on-board AC–DC converter) is required. Alternatively the AC–DC conversion can take place within the EVSE, involving an off-board charger. In this case, a DC voltage is provided to the vehicle and this method is further referred to as DC charging. The International Electrotechnical Commission (IEC) created an international standard, IEC 61851-1 [43], which applies to on-board and off-board conductive charging equipment for EVs. Thereby, the cable connection between the EV and the point of charging (i.e. a direct connection to the utility grid or to dedicated EVSE), the types of plugs, sockets, vehicle inlets,... used for this connection, as well as the different modes of charging along with the corresponding safety and communication features are defined [44, 45]. In particular of importance for this thesis are the different charging modes, which relate to the current and power levels of the chargers. Figures 1.10(a)-1.10(c) show the respective charging infrastructure that corresponds with each charging mode discussed below:

  - **Mode 1 (on-board) charging;** see Figure 1.10(a); *slow charging from a household-type socket*; stands for the connection of the EV to the AC supply network utilizing standardized sockets (single-phase or three-phase), not exceeding 16 A charging current and 250 V_{AC} (single-phase) or 480 V_{AC} (three-phase) at the supply side. For a 230/400 V_{AC}[7] utility grid, a 16 A rated socket permits a maximum charging power of 3.7 kW (single-phase) or 11 kW (three-phase) [45]. A resistor between the power indicator and the ground provides the resistive coding which is required to inform the EV on the available power rating of the grid connection [44].
  - **Mode 2 (on-board) charging;** see Figure 1.10(a); *slow charging from a household-type socket outlet with an in-cable protection device*; stands for the connection of the EV to the AC supply network utilizing standardized socket outlets (single-phase or three-phase), not exceeding 32 A charging current and 250 V_{AC} (single-phase) or 480 V_{AC} (three-phase) at the supply side. For a 230/400 V_{AC} utility grid, a 32 A rated socket permits a maximum charging power of 7.4 kW (single-phase) or 22 kW (three-phase) [45]. A socket with in-cable protection device is required, also providing the control pilot function which is used to inform the EV on the available power rating of the grid connection [44].

[7] 230/400 V_{AC} is the IEC recommended standard voltage.

  - **Mode 3 (on-board) charging;** see Figure 1.10(b); *slow or fast charging using a specific EV socket outlet with control and protection function installed*; stands for the connection of the EV to the AC supply network utilizing dedicated EVSE. Connection Case C (see [44]) allows charging currents up to 63 A while with connection Case B the charging current is limited to 32 A. For a 230/400 V_{AC} utility grid, the maximum power levels are: Case B, single-phase: 7.4 kW; Case B, three-phase: 22 kW; Case C, single-phase: 14.5 kW; Case C, three-phase: 43.5 kW. The control pilot signal and additional safety features are provided by the EVSE. The standard [43] also describes very high power AC charging with currents up to 250 A.
  - **Mode 4 (off-board) charging;** see Figure 1.10(c); *fast DC charging using an off-board charger*; stands for the connection of the EV to the EVSE utilizing an off-board charger which is located within the EVSE. High charging currents of up to 400 A are possible.

- **Inductive chargers:** the power is transferred magnetically (wireless) through inductive coupling [29, 46] rather than by direct electrical contact. This technology offers advantages of safety (galvanic isolation is inherently present), connector robustness, durability, and power compatibility, but, on the expense of a lower efficiency and the need of new infrastructure [29]. A separate international standard, SAE-J2954, for the wireless charging and positioning of EVs is currently being prepared by the Society of Automotive Engineers (SAE). The charging infrastructure required for inductive charging is depicted in Figure 1.10(d). Inductive charging is not further discussed.

Most of the EVs on the market are delivered with domestic-socket-compatible connection cables where the cable and its functionalities determine whether it supports mode 1 or mode 2 (see Figure 1.10(a)) charging [44]. Every domestic socket can be used as charging infrastructure, resulting in an extensive availability of charging opportunities for the user and a reduced range anxiety. However, due to the limited charging current (16 A socket outlets are the most widespread in Europe), charging time is relatively long with these charging modes. Due to the higher possible current, a shorter charging time can be achieved with mode 3 charging but, however, dedicated EVSE is required (see Figure 1.10(b)). This comes with increased infrastructure costs and reduced charging opportunities for the users, which negatively impacts the range anxiety. For charging at home, the investments in mode 3 EVSE might be unnecessary if the vehicle is parked at home for sufficiently long times to charge the battery with mode 1 or mode 2 [44]. Moreover, high charging currents can cause overheating and aging of the batteries. For mode 4 charging (i.e. DC charging, see Figure 1.10(c)) the advantages and disadvantages that come with mode 3 charging are even more pronounced. Additionally, EV purchase costs can be reduced as an on-board charger is not

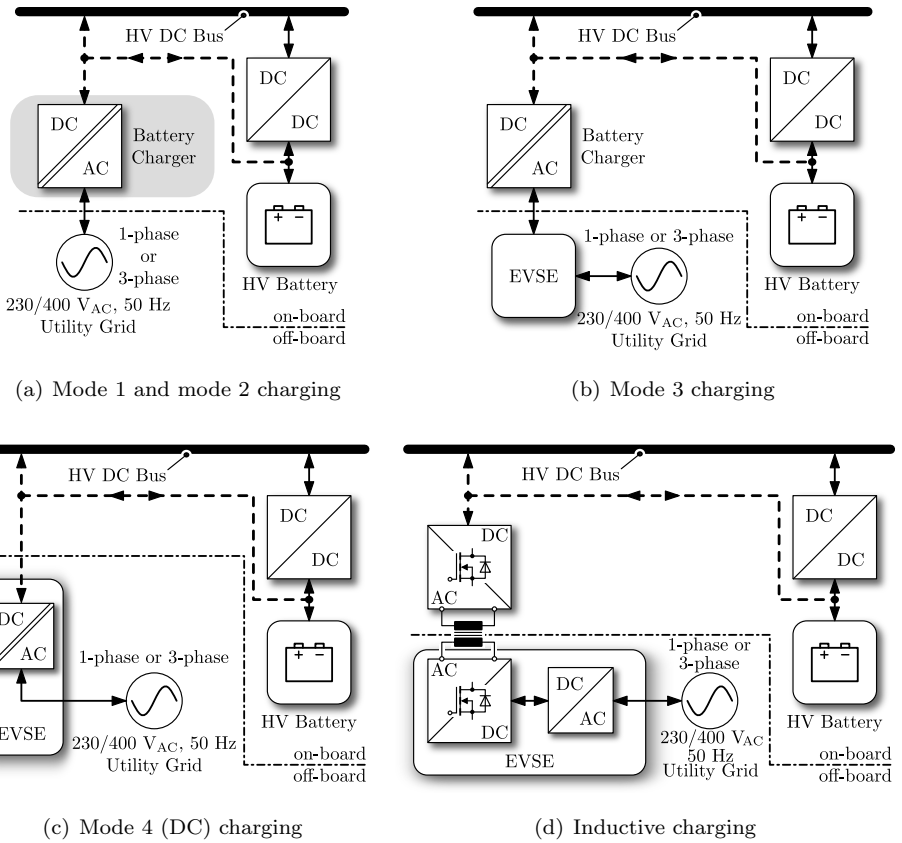


Figure 1.10: Charging infrastructure for conductive charging using (a) charging modes 1 and 2, (b) charging mode 3, (c) charging mode 4. (d) Charging infrastructure for inductive charging. The specifications of the AC–DC converter investigated in this work are based on single-phase mode 1 charging cf. inset (a).

anymore needed, which also leads to reduced weight and more space in the car. Nevertheless, the EVSE needs to be compatible with every car model that supports mode 4 charging.

Common issues of conductive chargers concern safety and the design of internationally standardized connection interfaces [43]. Galvanic isolation between the electric traction system and the mains power supply is a favorable option in conductive charger circuits [29]. Besides increased safety in the system it provides more convenience and freedom to fulfill the requirements given in the standard [43]. For example, in non-isolated chargers, a considerable effort is needed to

prevent unwanted earth fault protection trip due to the presence of common-mode currents, noise, and so on. By using a galvanic isolated charger, the impact of the (high-power) charging circuit on the earth path will be drastically reduced [29]. Furthermore, if the traction battery is bonded to the vehicle chassis, it is obligated that the charger provides a galvanic isolation between the mains (utility grid) and the battery [29, 43].

The specifications (see Section 1.3) of the single-phase, utility interfaced, bidirectional AC–DC converter investigated in this work are based on the requirements for single-phase, mode 1, on-board EV battery chargers[8] (cf. Figure 1.10(a)). They allow domestic charging at a maximum charging current of 16 A and a maximum charging power of 3.7 kW, assuming an IEC recommended standard grid voltage of 230/400 V_{AC}. Galvanic isolation is provided for the reasons mentioned above, while bidirectional power flow capability enables V2G operation. The DC output voltage range of the AC–DC converter strongly depends on whether the converter's DC output terminals are directly connected to the HV battery (HV battery connection) or to the HV DC bus (HV DC bus connection) (see Figure 1.10):

- **HV battery connection:** when the DC output terminals of the on-board AC–DC battery charger are connected to the HV battery terminals [20], the charging energy is directly transferred from the charger to the battery during charging and vica versa during V2G operation. This requires a relatively large output voltage range of the AC–DC converter, which has to cover the whole battery voltage range.
- **HV DC bus connection:** when the DC output terminals of the on-board AC–DC battery charger are connected to the HV DC bus terminals [19], the charging energy is indirectly (i.e. via the HV-battery-interfacing DC–DC converter) transferred from the charger to the battery during charging and vica versa during V2G operation. Now the output voltage range of the AC–DC converter can be kept relatively small since during charging the voltage of the HV DC bus can be stabilized to an optimal value by the HV-battery-interfacing DC–DC converter. Moreover, the other power electronic circuits which are interfaced with the HV DC bus can now directly draw energy from the grid in order to for example charge the LV battery and to feed energy to the low power and the high power loads during charging. However, compared to the previous case, charging of the HV battery now encompasses an additional energy conversion stage: the HV-battery-interfacing DC–DC converter.

[8] In order to reduce weight, volume, and costs, charging systems are described (e.g. in [19, 29]) which use the available traction hardware, inverter, and motor to have an integrated battery-charger-and-drive-system. However, disadvantageous are efficiency and maintainability [47].

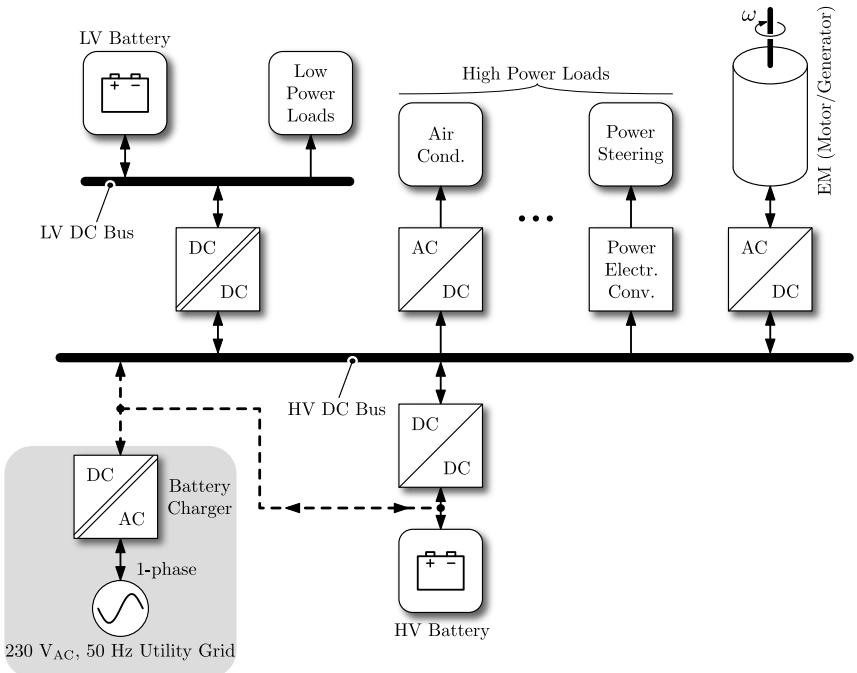


Figure 1.11: Typical BEV electric power system architecture. This example shows an on-board, single-phase, bidirectional, isolated battery charger which can either be connected to the HV battery or to the HV DC bus.

Battery Electric Vehicles (BEVs)

The drive train of a battery electric vehicle (BEV) is exclusively powered from an electric machine which draws energy from a high energy density HV battery [48, 49] during propulsion and recharges the battery during regenerative braking [50]. With BEVs zero (local[9]) CO_2 emissions can be achieved [34], making them very attractive for urban areas where traffic emissions considerably pollute the local environment. However, market penetration of BEVs is limited due to their high initial cost, the relatively short driving range, and long charging (refueling) time [30]. Concepts with several energy sources (e.g. HV batteries, ultracapacitors, and even reduced power fuel cells) have been proposed to expand the driving range of BEVs [34, 50].

The power system architecture of a BEV's drive train (see Figure 1.11) is similar

[9]The ultimate target of zero global CO_2 emissions by personal vehicles can be achieved in case the batteries are charged from renewable electricity (e.g. wind, solar, ...).

to that of a series PHEV (cf. Figure 1.9) without ICE and electric generator. Although several variants exist [50], common for each architecture is the need for a plug-in battery charger which again (similar to PHEVs) can be directly connected to the HV battery pack or to the HV DC bus. Contrary to the architecture shown in Figure 1.11, in some BEV concepts – the so called passive topologies – the energy storage devices (HV battery, ultracapacitors,...) are directly connected to the HV DC bus without DC–DC converter. In this case the plug-in battery charger directly interfaces the storage devices with the utility grid [50].

Plug-in Battery Chargers— Since the electric system architectures of BEVs and (P)HEVs are rather similar (they both include a HV battery pack and a HV DC bus), the considerations, remarks, and requirements for plug-in battery chargers used in PHEVs (especially full hybrids) still apply for the plug-in battery chargers used in BEVs. Furthermore, BEVs and (P)HEVs have very similar optimal system voltages (HV battery and HV DC bus) as a function of power rating [41].

Fuel Cell Vehicles (FCVs)

In FCVs, the on-board fuel cells – typically proton exchange membrane fuel cells (PEMFCs) or solid oxide fuel cells (SOFCs) [35] – produce the electricity which is used to provide propulsion power to the EM(s) [30, 51]. Similar to BEVs, FCVs enable zero emission since fuel cells do not burn fossil fuels and therefore do not produce pollutants (the byproduct of a hydrogen fuel cell is water). The achievable cruising range is comparable to that of ICEVs. Issues related to FCVs include the high fuel cell cost, the storage of hydrogen, the transportation and production of hydrogen, and the fuel cell life cycle.

Generally, other high power density devices such as lithium-ion HV batteries and/or ultracapacitors are used in conjunction with the fuel cell [35, 51, 52] in order to stabilize the HV DC bus using a bidirectional DC–DC converter. This is done due to the fact that fuel cell stacks cannot respond to sudden load changes and system transients. Also, the fuel cell cannot absorb regenerative energy. As a result, from the electric system architecture viewpoint, FCVs can be considered as a type of series hybrid vehicles (similar to Figure 1.9), in which the fuel cell acts a an electrical generator that uses hydrogen (see Figure 1.12) [34]. Besides providing propulsion power, the fuel cell stack also powers all the auxiliary fuel cell components (compressors, pumps,...) as well as the conventional 14 V bus (low power loads) and the high power loads (see Figure 1.12). The fuel cell, the HV battery (and/or ultracapacitors), and the 14 V bus are all connected to the HV DC bus using separate DC–DC converters.

Plug-in Battery Chargers— Usually FCVs do not include a plug-in battery charger (the HV battery only has a buffer function), but in case a charger would be required, the considerations, remarks, and requirements for plug-in battery

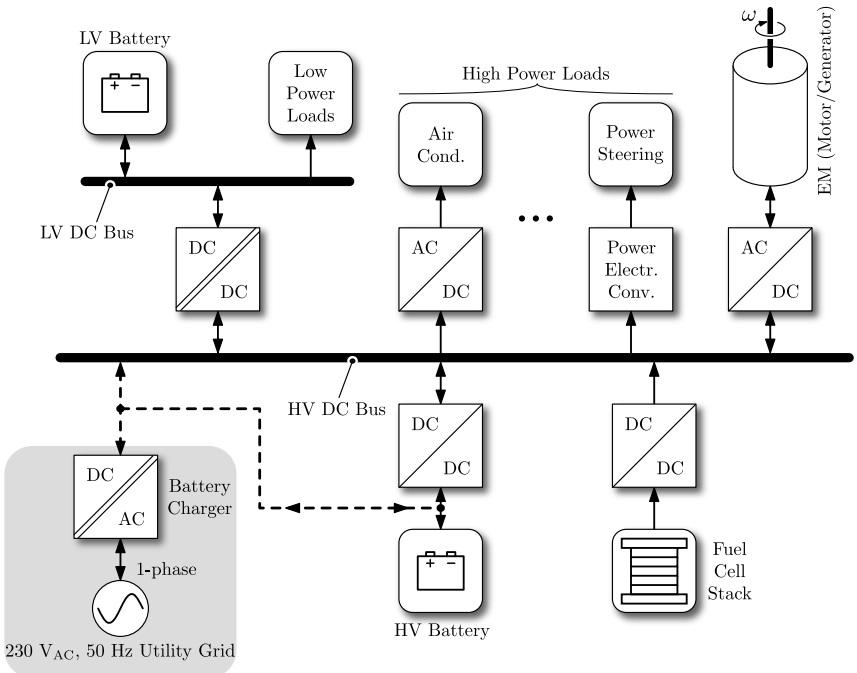


Figure 1.12: Typical FCV electric power system architecture, including a HV battery which stabilizes the HV DC bus voltage during transient load conditions and which buffers the regenerative braking energy. The FCV turns into a plug-in FCV in case a utility interfaced battery charger is present. This example shows an on-board, single-phase, bidirectional, isolated battery charger which can either be connected to the HV battery or to the HV DC bus.

chargers used in PHEVs still apply for the plug-in battery chargers used in FCVs since the electric system architectures of FCVs and HEVs are rather similar (they both include a HV battery pack and a HV DC bus).

1.2.2 Interfaces for Renewable Energy Sources (RESs) and Energy Storage Systems (ESSs)

Grid Interfaces for Individual RESs

The integration of renewable energy sources (RESs) and microsources, such as for example PV modules, fuel cells (FCs), small wind turbines, and microturbines (e.g. hydro power and combined heat and power (CHP)), into the grid – in the form of

distributed generation (DG) – requires power electronic systems as grid interfaces [12]. Thus, power converters enable the effective utilization of the electric energy generated by the RESs. The vast majority of DG systems are connected to the low voltage distribution networks [12, 15] where the single-phase, utility interfaced, isolated AC–DC converter investigated in this work (power level 3.7 kW; connected to the 230 V_{AC}, 50 Hz utility grid; see also Section 1.3) finds its application in for example small (1 - 5 kW) commercial DG systems such as residential PV modules [22] and FC units [53] (see Figure 1.13(a)). The 3 kW, isolated DC–AC PV converter presented in [22] interconnects a 150 V - 400 V PV array with the 230 V_{AC}, 50 Hz utility grid, while the 1 kW, isolated DC–AC FC converter presented in [53] interfaces a 300 V_{nom} FC stack with the 200 V_{AC}, 50 Hz utility grid. The direct connection of the DC–AC converter's DC terminals to either a PV array or a fuel cell stack implies a wide DC voltage range for the DC–AC converter (e.g. 150 V - 400 V [22]). However, PV and FC DC–AC converters do not require the bidirectional power flow capability of the converter investigated in this work since they only have to deliver power to the grid (grid-feeding).

Grid Interfaces for ESSs, Enabling Smart Home Concepts, AC Microgrids, and DC Nanogrids

The increasing amount of RESs and DGs requires new strategies for the operation and management of the electricity grid in order to maintain and even improve the power supply reliability and quality [13]. Additionally, liberalization of the electricity markets leads to new management structures in which trading of energy and power will become increasingly important. This has led to several new concepts which allow an efficient exploitation of the DG capacity, as well as a more effective and flexible operation of the grid. Prominent examples of these novel grid structures are 'smart home' concepts [25], AC microgrids [12, 15] and residential DC distribution systems (DC nanogrids) [26, 28]. Common to these concepts is the indispensable requirement of energy storage systems, enabling the decoupling of electricity generation from the electricity demand. Appropriate integration of intermittent RESs with storage systems allows for a greater market penetration of RESs and a reduction of primary energy use and emissions [13].

- **Smart home concepts;** see Figure 1.13(b); the 'smart home' solution from SMA [25] is an example where electrical energy storage (i.e. battery storage) together with 'smart' energy management are used on a household level in order to help PV system owners to use the produced solar power in a more optimal and profitable way by increasing the rate of self-consumption. Thereby, the energy produced by the PV modules is primarily used by the household loads, while excess power is stored in the batteries for later use or fed into the utility grid. A top level energy manager harmonizes power generation and consumption schedules by for example applying demand side

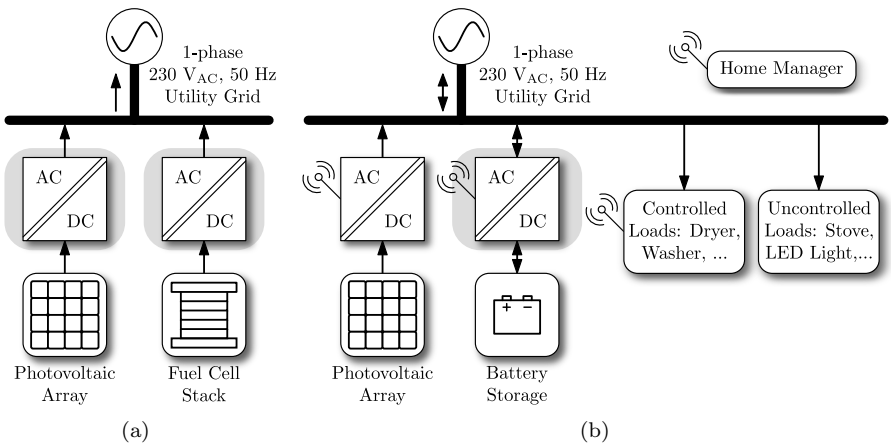


Figure 1.13: Applications of single-phase, utility interfaced, isolated AC–DC converters: (a) unidirectional grid interfaces for individual (residential) RESs such as PV modules and FC stacks [22, 53]; (b) grid interfaces for (residential) battery storage systems, enabling 'smart home' concepts such as for example proposed by SMA [25]. In this case, bidirectional AC–DC converters are required.

management to the controllable loads. As a result, the load on the utility grid is reduced through increased self-consumption, implying less power consumption from the grid and less PV power that is fed into the grid. The single-phase, bidirectional, AC–DC converter that is used to interface the batteries with the utility grid (230 V_{AC}, 50 Hz) is the SMA Sunny Island 6.0H [54], having a maximum rated (apparent) power of 4.6 kVA (20 A AC current) and a DC voltage range of 41 V to 63 V [55]. The bidirectional AC–DC converter topology investigated in this work (see further) is suited for this sort of applications.

- **AC microgrids;** see Figure 1.14; a systematic organization of distributed generation (DG) units, each consisting of an energy source (e.g. a RES), an ESS, and a grid-interfacing, bidirectional AC–DC converter (see Figure 1.14, left inset), forms a microgrid (see Figure 1.14, right inset) [12]. The microgrid is connected to the utility system through a static transfer switch (STS) at the point of common coupling (PCC) and presents itself to the utility as a dispatchable load which can operate in grid-connected mode or autonomous islanding mode. Compared to a single DG unit, the microgrid has more capacity and control flexibilities to fulfill system reliability and power quality requirements, and to avoid problems caused by single DG units. These features benefit both the utility and the customers [12]. Further features of

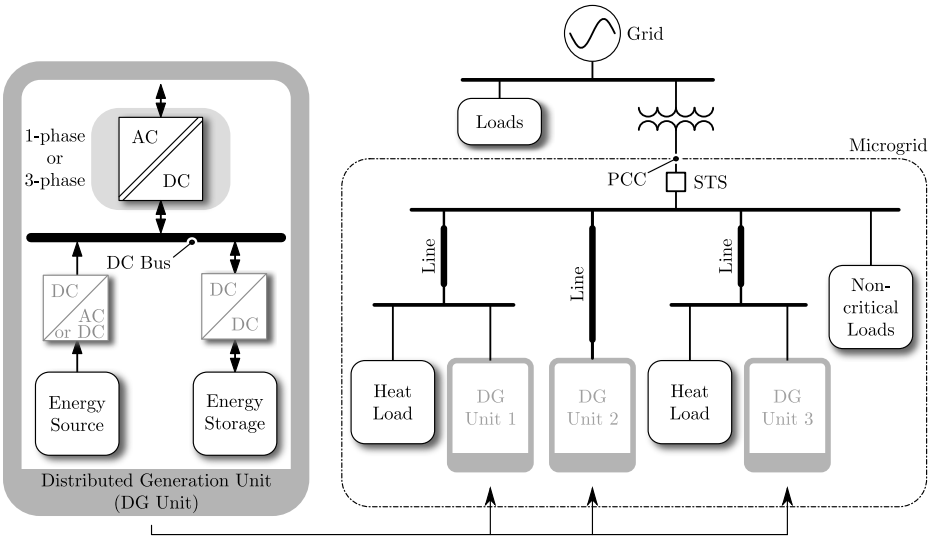


Figure 1.14: Example of an AC microgrid with DG units which are interfaced with the grid through bidirectional AC–DC converters [12].

microgrids, which can increase the performance and reliability of the electrical system, are [12, 15]:

- *Grid support services* such as generation scheduling optimization, enhanced system control and dispatch services, reactive power supply and voltage and frequency control, black-start restoration, energy imbalance compensation, spinning reserve operation, extension of operational reserve capability, peak shaving, optimized power flow and energy management,...;
- *Island operation* which ensures continued operation in the event of a utility interruption;
- *Plug-and-play capability* which enables the installation of additional DG units without changing the control strategies of already installed DG units;
- *Power quality improvement* such as harmonics and unbalance compensation, flicker reduction, transient voltage support during grid-faults, or reactive power compensation;
- *Line loss reduction*;
- ...

Since most of the RESs are of relatively low power capacities at up to several hundred kilowatts (domestic kilowatt-level DG units are also feasible),

microgrids are typically situated at the residential level (i.e. the LV distribution grid) [12, 15]. The DG units are individually interfaced with the utility grid through single-phase or three-phase (depending on the power level), bidirectional AC–DC converters (see Figure 1.14, left inset) which favorably include a galvanic isolation due to safety reasons. Therefore the single-phase, bidirectional AC–DC converter topology investigated in this work (see further) is suited for this application. The DC voltage range for the AC–DC converter depends on whether the RES and the ESS use individual power converters to connect to a (stabilized) DC-bus or not. Furthermore, the non-radial system configuration of a microgrid substantially increases the control complexity of the utility interfaced AC–DC converters, and the capability for providing ancillary services by a microgrid depends mainly on the capability of these converters to accurately control the active and reactive power flow in the system in a coordinated manner [15]. For example, once transferred to islanding operation the DG systems must immediately form a grid, share the power demand, and continue supplying power to at least all critical loads [12]. Depending on their operation in an AC microgrid, power converters can be classified into grid-feeding, grid-supporting, and grid-forming power converters [15]. Note that the reactive power transfer capability of the AC–DC converter investigated in this work (i.e. in particular the single-stage DAB AC–DC converter topology) is very limited. Moreover, it can only be used for grid-feeding purposes since it is controlled as a current source and therefore needs a generator or a power converter to form the grid voltage in order to be able to operate.

- **Residential DC distribution systems (DC nanogrids);** see Figure 1.15; in (residential) DC distribution systems, multiple energy sources (preferably RESs), ESSs and loads are connected to a HV DC bus through different power converters, forming a DC nanogrid [26–28]. This DC system can for example be implemented in residential buildings or home environments, enabling self-sustainability with zero net energy consumption, optimized power management, and operation which is fully dynamically decoupled from the AC grid. A top level energy manager can be used to harmonize power generation and consumption schedules by for example applying demand side management to the controllable loads. The DC voltage used in DC nanogrids is a straightforward and simple solution to integrate multiple energy sources, ESSs, and loads as there are no AC losses, no reactive power issues, and no frequency synchronization issues [26]. Moreover, the power factor correction (PFC) stages in appliances are eliminated since most of the household appliances are electronic loads. A single-phase or three-phase (depending on the power level) bidirectional AC–DC converter is used to interconnect the DC bus of the DC nanogrid with the AC utility grid. This utility interfaced AC–DC converter is sometimes called the energy control center (ECC) [26]. In fact, a DC nanogrid can be seen as an extension of

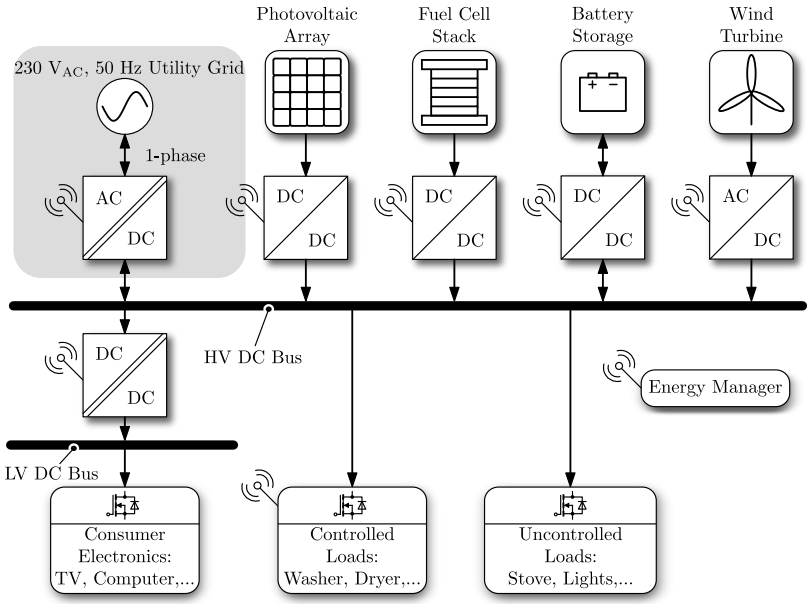


Figure 1.15: Example of a DC nanogrid implemented at home and consisting of a HV DC bus that is interfaced with the 230 V_{AC}, 50 Hz utility grid through a single-phase, bidirectional, and isolated AC–DC converter.

the previously mentioned microgrid-coupled DG units where the ECC can perform similar tasks than the utility interfaced AC–DC converter of the DG unit. Besides the HV DC bus, typically an additional LV 24 V or 48 V DC bus is used for supplying energy to the consumer electronic devices and portable equipment (see Figure 1.15) [26]. Due to the connection to a HV DC bus, a relatively narrow DC voltage range for the utility interfaced AC–DC converter (i.e. the ECC) is feasible (e.g. 360 V - 400 V [26]). The single-phase, utility interfaced, bidirectional, and isolated AC–DC converter investigated in this work (power level 3.7 kW; connected to the 230 V_{AC}, 50 Hz utility grid) finds its application in the realization of the ECC. However, as explained above for microgrids, this converter (i.e. the single-stage DAB topology) allows only a limited reactive power transfer and can only be used for grid-feeding purposes. In [26] a 10 kW, bidirectional, non-isolated AC–DC converter is presented for being used as an ECC, interfacing the 360 V - 400 V (380 V_{nom}) DC bus of a DC nanogrid with a 240 V_{AC}, 60 Hz utility grid. A 500 W_{nom}, 1 kW_{peak}, unidirectional, isolated DC–AC converter which interfaces a 200 V DC bus with a 208 V_{AC}, 60 Hz utility grid is presented in [27] for similar purposes. However, there power can only be fed into the grid.

1.3 Specifications of the Investigated AC–DC Converter

The specifications (see Table 1.1) of the single-phase, utility interfaced, bidirectional, and isolated AC–DC converter investigated in this work are based on the requirements for future, mode 1 compatible, on-board electric vehicle (EV) battery chargers. They allow domestic charging at a maximum/nominal (active) charging current of $I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$. Assuming an IEC recommended standard/nominal grid voltage of $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$ and a line frequency of $f_{\mathrm{L}} = 50$ Hz, the maximum/nominal charging power is $P_{\mathrm{nom}} = 3.7$ kW. The AC–DC converter comprises an AC port with a terminal voltage V_{AC} of $230\ \mathrm{V_{rms}} \pm 10\%$, nominal voltage $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$, and a high voltage (HV) DC port. The voltage level V_{DC2} at the DC port is chosen based on the forecasts that, with the increasing power demand of electric vehicles, the vehicular power system voltages tend to rise [37, 41]. Concerning this voltage level it is assumed that the HV DC terminals of the AC–DC converter are connected to the HV DC bus of the EV (see Figure 1.16). Since during charging the voltage of this DC bus can be stabilized to an optimal value by the HV-battery-interfacing DC–DC converter, a relatively narrow range for the DC terminal voltage V_{DC2} is feasible. Therefore, this range is (arbitrarily) selected as $370\ \mathrm{V} \leqslant V_{\mathrm{DC2}} \leqslant 470\ \mathrm{V}$, nominal voltage $V_{\mathrm{DC2,nom}} = 400\ \mathrm{V}$, $100 \cdot (V_{\mathrm{DC2,max}} - V_{\mathrm{DC2,min}})/V_{\mathrm{DC2,nom}} = 25\ \%$.

The selected DC port voltage levels allow the use of high performance, high voltage, metal oxide semiconductor field-effect transistors (MOSFETs) which are the primary considered semiconductor switching devices. Furthermore, galvanic isolation is required between the AC port and the HV DC port for reasons of safety,

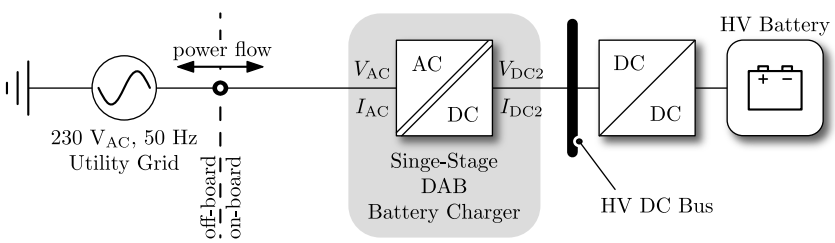


Figure 1.16: Schematic of the scenario considered for the connection of the HV DC port of the investigated AC–DC converter: the HV DC terminals of the AC–DC converter are connected to the HV DC bus of the EV, having a voltage range of $370\ \mathrm{V} \leqslant V_{\mathrm{DC2}} \leqslant 470\ \mathrm{V}$.

Property		*Value*	*Description*
AC-side	V_{AC}	$207 \leqslant V_{\mathrm{AC}}\ (\mathrm{V_{rms}}) \leqslant 253$ $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$	min. and max. AC input voltages nominal AC input voltage
	$I_{\mathrm{AC,P}}$	$-16 \leqslant I_{\mathrm{AC,P}}\ (\mathrm{A_{rms}}) \leqslant 16$ $I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$	min. and max. (active) AC input currents nominal (active) AC input current
	f_{L}	50 Hz	line frequency
DC-side	V_{DC2}	$370\ \mathrm{V} \leqslant V_{\mathrm{DC2}} \leqslant 470\ \mathrm{V}$ $V_{\mathrm{DC2,nom}} = 400\ \mathrm{V}$	min. and max. voltages at the HV DC port nominal voltage at the HV DC port
EMC compliance		CISPR 22 Class B	requirements related to the EMC input filter design
PF		> 0.9 (at $I_{\mathrm{AC,P}} \geqslant 0.1 \cdot I_{\mathrm{AC,P,nom}}$)	power factor requirement
THD compliance		IEC 61000-3-2 standard, and THD $\leqslant 5$ % (at $I_{\mathrm{AC,P}} \geqslant 0.3 \cdot I_{\mathrm{AC,P,nom}}$)	requirements related to the input current harmonics

Additional requirements

- galvanic isolation
- bidirectional power flow capability
- high conversion efficiency ($\eta > 95$ % at the nominal operating point and $\eta > 93$ % within reasonable voltage and current ranges)
- high power density ($\rho \geqslant 2$ kW/liter)
- autonomous air cooling
- semiconductor switching devices: MOSFETs

Table 1.1: Specifications and requirements of the investigated single-phase, utility interfaced, bidirectional, and isolated AC–DC converter.

while bidirectional power flow[10] capability must enable V2G operation. The power range is defined by the converter's (active) AC input current which must be in the range $-16\ \mathrm{A_{rms}} \leqslant I_{\mathrm{AC,P}} \leqslant 16\ \mathrm{A_{rms}}$ for all input and output voltage conditions. Moreover, the converter should be designed using autonomous air cooling, avoiding extension of the existing (typically) water cooling system in the vehicle. Further objectives regarding the selection and the design of the bidirectional AC–DC converter are:

- A high converter efficiency of $\eta > 95$ % at the nominal operating point ($V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$, $I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, $V_{\mathrm{DC2,nom}} = 400$ V);

[10] Positive power flow values denote a power transfer from the AC port to the HV DC port and negative power flow values denote power transfer from the HV DC port to the AC port, (cf. (3.10), see Section 3.1 of Chapter 3).

- A converter efficiency of $\eta > 93$ % within reasonable input and output voltage ranges and reasonable input current ranges;
- A high power density (i.e. low converter volume) of $\rho \geqslant 2$ kW/liter;
- Electromagnetic compatibility (EMC) compliance with the CISPR 22 Class B standard [56];
- A power factor (PF) close to one (unity power factor; UPF) with an absolute minimum of PF > 0.9 (at $I_{\mathrm{AC,P}} \geqslant 0.1 \cdot I_{\mathrm{AC,P,nom}}$);
- Compliance with the IEC 61000-3-2 standard [57] for input current harmonics, which must result in a low total harmonic distortion (THD) of the AC input current, goaling for THD $\leqslant 5$ % (at $I_{\mathrm{AC,P}} \geqslant 0.3 \cdot I_{\mathrm{AC,P,nom}}$).

Apart from the EMC and THD requirements, which are mandatory, the design objectives (e.g. efficiency and power density) listed above are compiled based on the performance of the single-phase, utility interfaced, and isolated AC–DC EV battery charger (dual-stage topology, see Section 1.4.2) recently presented in [20], which is taken as a benchmark. Although not bidirectional, the system specifications of this converter (3.3 kW, 16 A maximum input current, 200 V - 450 V DC output voltage range) are similar to the specifications for the converter investigated in this work. For the reference converter in [20] a peak efficiency of 93.6 % (at $V_{\mathrm{AC}} = 240$ $\mathrm{V_{rms}}$; $V_{\mathrm{DC2}} = 400$ V; $P = 3.3$ kW), a power density of 0.66 kW/liter, an input current THD of less than 5 % from half load to full load, a PF greater than 0.99 from half load to full load, and compliance with the IEC 61000-3-2 standard is reported. Note that the input voltage range of the AC–DC converter in [20] is defined as 85 $\mathrm{V_{rms}} \leqslant V_{\mathrm{AC}} \leqslant 265$ $\mathrm{V_{rms}}$ where, however, the AC–DC converter in this work is designed for 207 $\mathrm{V_{rms}} \leqslant V_{\mathrm{AC}} \leqslant 253$ $\mathrm{V_{rms}}$.

Besides increased efficiency and power density (i.e. reduced volume), reduction of the cost and weight of the power electronics and electric machinery are one of the main design goals for future EVs [19, 21, 58, 59]. A low converter weight and volume allow simple installation, handling and maintenance of the system, while cost is the fundamental factor for marketability. Additionally, expansion of the EV's driving range can be achieved through reduction of the weight. Although the primary emphasis of this work is on achieving a high conversion efficiency and high power density, implicitly these objectives also contribute to a lower weight and cost. Higher conversion efficiencies, for example, lead to reduced cooling requirements and thus lower weight, volume, and cost [16, 17, 60]. Moreover, provided that no thermal limitations apply, a high power density can be achieved through increasing the switching frequency, which consequently results in smaller passive elements such as inductors, transformers, and capacitors [61], and thus again in lower weight and cost [16, 17, 60]. However, this is on the expense of switching frequency related losses such as conduction losses due to high-frequency effects, core losses and

semiconductor switching losses [61]. Moreover, thermal limitations apply at high switching frequencies, resulting in an increased total converter volume [16]. Details about the selection of the switching frequencies in order to accommodate a compact converter design without causing excessive switching frequency related losses and without bouncing into the thermal limits are given in Section 4.1.1 of Chapter 4. High switching frequencies (e.g. > 100 kHz) are enabled by on the one hand the soft-switching nature of the investigated AC–DC topology (see Section 1.4.4), and on the other hand the fast switching behavior of the latest MOSFET generations, which are considered for the semiconductor switching devices. The selection of the employed MOSFETs is detailed in Section 5.1.1 of Chapter 5. Another important objective in the design of future power electronic converters is the maximization of the system reliability which, however, is considered out of the scope of this work due to the complexity of the design task.

1.4 Single-Phase, Bidirectional, and Isolated AC–DC Converters: Topology Selection

1.4.1 Introduction

A proper topology selection is crucial for the successful fulfillment of the converter requirements specified in Section 1.3. However, the great variety of different topologies and circuit implementations available for the realization of the considered single-phase, bidirectional, and isolated AC–DC energy conversions makes it quasi impossible to perform a comprehensive evaluation of all options. Therefore, a good strategy is to pick a number of candidates and subject them to the multi-objective optimization (MOO) procedure outlined in Section 1.1.4. A pre-selection of suitable topologies can for example be made based on designs that are already carried out successfully in the past (experience based), based on comparative evaluations that are already performed in literature, or based on simplified pre-analyses. By evaluating the results obtained from the individual MOOs, the topology which is capable of meeting the specifications/requirements in the best possible way, i.e. with regard to one or more (weighted) Performance Indices, can then be taken for the final converter realization. This rather top-down approach strongly relies on the availability of well established and proven converter concepts/topologies and corresponding modulation schemes, making steps 2 to 4 (i.e. "Converter Topology, Electric Power Circuit Model, and Modulation Scheme") in the MOO procedure (see Section 1.1.4, Figure 1.7) relatively straightforward. Nevertheless, in this work a different, rather bottom-up approach is used for the selection of the converter topology to be investigated. If fact, only a (single-stage, 1-S) AC–DC topology based on the well known dual active bridge (DAB) DC–DC converter is considered. This choice is the direct result of a collaboration with an industry partner, in particular with the company Triphase NV [62]. Within the course of this collaboration, several major shortcomings in the existing analyses and circuit implementations of DAB converters have come into light, especially regarding the available (soft-switching) modulation schemes and regarding the way the high-frequency (HF) AC-link of the DAB is implemented. It is the principle goal of this doctorate to address these shortcomings. This means that instead of subjecting a set of preselected topologies with given modulation schemes to the MOO procedure and evaluating the outcome, here the focus is mainly on the (re)development of the DAB modulation schemes as well as on the provision of solutions for the fundamental limitations of the existing DAB HF AC-link implementation(s). In Section 1.4.4 the topology selection is further motivated and the considered DAB AC–DC converter variant is detailed. Based on this discussion, the objectives and the main contributions of the work are compiled, which are summarized in Section 1.5. As detailed in the chapter overview (see Section 1.6), there is a strong relation between the MOO procedure outlined in Section 1.1.4 and the structure of

this thesis. A complete overview of the state-of-the-art, i.e. regarding the existing analyses and circuit implementations of DAB converters, is given in Section 2.2 of Chapter 2, highlighting the above mentioned shortcomings. For the sake of completeness and for further reference, first a short overview of the most common single-stage and dual-stage converter topologies that can alternatively be used to realize single-phase, bidirectional, and isolated AC–DC converters is given below.

1.4.2 Dual-Stage (2-S) AC–DC Converter Topologies

Single-phase, bidirectional, and isolated AC–DC converters are most commonly realized using two conversion stages (dual-stage, 2-S, see Figure 1.17), involving a utility interfaced, single-phase power factor correction (PFC) rectifier (first conversion stage) followed by an isolated DC–DC converter (second conversion stage) [63]. The PFC front-end rectifies the AC line voltage $v_{\mathrm{AC}}(t)$ into a DC voltage which is typically 'boosted' to a higher level and transferred into a regulated intermediate HV DC-link voltage V_{DC1} (usually 380 V ... 450 V in the European grid). Moreover, the PFC rectifier must assure a high power quality in terms of PFC and total harmonic distortion (THD). Regarding these goals, a PFC rectifier is preferred over a passive rectifier circuit, such as a line commutated diode rectifier, since it is able to both reduce the line current harmonics in order to meet the worldwide THD standards (cf. [57]), and to achieve a high power factor (PF) by actively shaping the line current $i_{\mathrm{AC}}(t)$ in phase with the line voltage $v_{\mathrm{AC}}(t)$. Furthermore, 2-S AC–DC power conversion is typically identified by the presence

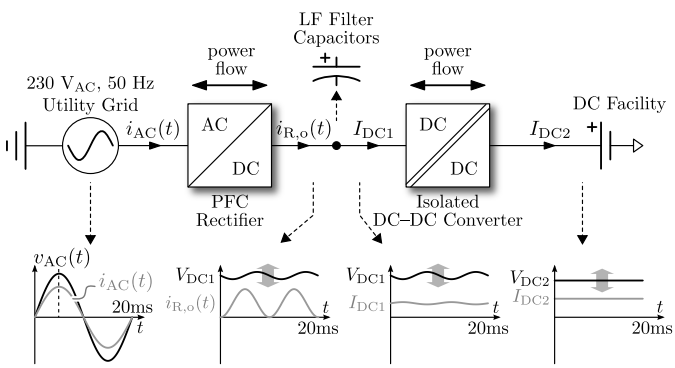


Figure 1.17: General block diagram and principle waveforms of the single-phase, dual-stage (2-S), bidirectional, and isolated AC–DC converter topologies (i.e. the ones where LF filter capacitors are present in the DC-link).

of a DC-link storage element[11], smoothing the inherent power variation (i.e. the double line frequency component of the input power) of single-phase AC–DC converters. Therefore, the DC-link mostly consists of large, low frequency (LF) filter capacitors (e.g. electrolytic capacitors (ELCOs)). The smoothed DC-link voltage V_{DC1} is further input to the DC–DC converter, providing galvanic isolation and performing the regulation of the DC output voltage V_{DC2}. Consequently, a 2-S topology with DC-link storage allows for a dynamic and tight output voltage control without having direct impact on the input current quality [64]. It is evident that, regarding bidirectional AC–DC converters, both the PFC rectifier and the isolated DC–DC converter must allow bidirectional power flow, a feature that is also not possible when using a diode rectifier as AC–DC front-end.

In literature, numerous topologies are proposed for realizing the PFC rectifier stage and the isolated DC–DC conversion stage, making it quasi impossible to provide a comprehensive overview/evaluation of all possible implementations/combinations. A comprehensive topology survey and comparative evaluation of unidirectional PFC rectifier topologies for use in PEV battery chargers is given in [63]. There the focus is on several single-phase and three-phase boost PFC rectifiers which operate in continuous conduction mode (CCM) and boundary conduction mode (BCM), and which offer high efficiency, high power factor, high power density, and low cost. CCM operation has become particularly popular as reduced electromagnetic interference (EMI) levels result from its utilization. An extensive review of unidirectional and bidirectional single-phase PFC rectifier topologies with improved power quality is presented in [65], including a selection of some variants with galvanic isolation. In [66], single-phase, non-isolated PFC topologies based on the boost converter approach are summarized. Furthermore, a bidirectional, non-isolated, multi-cell totem-pole PFC rectifier, employing a triangular current mode (TCM) soft-switching modulation scheme over the complete mains period, is described in [67, 68]. Extensive overviews, topology surveys, and comparative evaluations of common topologies used for the isolated DC–DC converter stage are presented in [69–73], inter alia including numerous (soft-switching) dual active bridge (DAB) topologies and resonant topologies, whether or not combined with active auxiliary snubber circuits and/or a second, typically hard-switched and non-isolated, DC–DC conversion stage. Also the isolated, bidirectional cuk topology, as well as several hard-switching and/or unidirectional DC–DC architectures are discussed in the above mentioned references. The AC–DC converter presented in [20], and which is taken as a benchmark for the AC–DC converter investigated in this work (see Section 1.3), is an example of a dual-stage AC–DC topology. It is implemented using a combination of an interleaved boost PFC rectifier and an isolated full-bridge DC–DC converter. However, this topology only allows unidirectional power flow from the utility grid to the DC facility at its output.

[11] Note that although 2-S AC–DC power conversion is typically identified by the presence of a DC-link storage element, this does not apply as a general definition.

1.4.3 Single-Stage (1-S) AC–DC Converter Topologies

Besides the traditional dual-stage approach, several single-stage (1-S, see Figure 1.18) converter topologies have been proposed for the realization of single-phase, bidirectional, and isolated AC–DC converters. These 1-S AC–DC architectures are typically identified by the absence of an intermediate HV DC-link storage element, inter alia enabling the omission of large, bulky, failure prone electrolytic DC-link capacitors. As a result, the AC–DC energy conversion takes place in a single conversion stage, which is now responsible for all the required functionalities such as the PFC, the galvanic isolation, the reduction of the line current harmonics, and the regulation of the DC output voltage V_{DC2}. Consequently, compared to the 2-S topologies, 1-S AC–DC converters have the potential to benefit the system performance with regard to efficiency, volume (power density), number of components (reliability), weight, and costs due to the effective omission of a complete energy conversion stage [74]. However, this is at the expense of an increased filtering effort on the DC output side where large LF filter capacitors (e.g. ELCOs) are required in case a low output voltage ripple is desired[12]. This deficiency vanishes completely when the single-phase, 1-S AC–DC converters are used in a three-phase architecture where, in case of symmetrical sinusoidal current consumption, a constant instantaneous power is delivered and only storage at the switching frequency is required. However, although 1-S systems do not require a PFC front-end and consequently contain less components, 2-S topologies have the benefit that the PFC stage and the DC–DC stage are decoupled via the DC-link and thus both systems can be optimized with narrow specifications which might even result in a better global performance [75, 76].

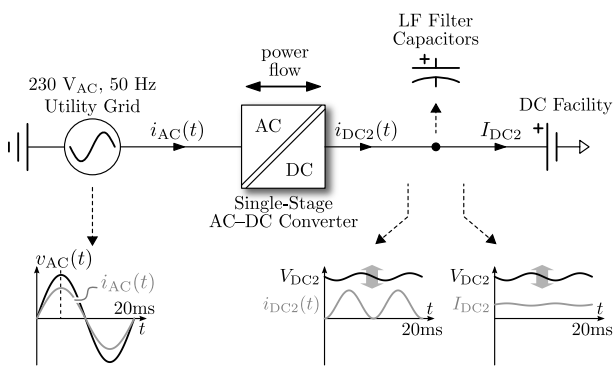


Figure 1.18: General block diagram and principle waveforms of the single-phase, single-stage (1-S), bidirectional, and isolated AC–DC converter topologies.

[12]Note that a 1-S AC–DC converter handles the double line frequency component of the input power.

In literature, numerous 1-S AC–DC converter topologies are presented. In [77], a new isolated single-phase, single-stage PFC AC–DC converter based on the Cuk concept ("true bridgeless PFC") is proposed, which in [78] is compared against a conventional two-stage approach based on a bridgeless PFC rectifier and a subsequent LLC-resonant DC–DC converter. However, the converter system only allows for unidirectional power flow. An isolated single-stage AC–DC converter with bidirectional power flow is introduced in [79, 80], using a cycloconverter on the primary side and a voltage source converter on the secondary side of a medium frequency transformer. The subject of this thesis is the single-stage DAB AC–DC converter topology [81–88], which is extensively discussed in the following.

1.4.4 Topology Selection and Motivation

As mentioned above (see Section 1.4.1), the converter topology investigated in this work for the realization of the energy conversion specified in Section 1.3 is a single-stage (1-S) AC–DC topology that is based on the well known dual active bridge (DAB) DC–DC converter. This choice origins from a collaboration with industry partner Triphase NV [62]. During the initial period of the doctoral studies at the KU Leuven, Triphase was developing a (potentially) high performance three-phase AC–DC converter for hydrogen generation and fuel cell applications. The converter architecture was composed of multiple 2.2 kW single-phase, bidirectional, and isolated AC–DC modules for interfacing the individual phases (230 V_{AC}) of the 400 V_{AC}, 50 Hz three-phase utility grid with a HV DC-bus (DC-bus voltage range: 135 V - 190 V), i.e. an energy conversion that regarding the converter functionalities (single-phase, bidirectional, isolated, AC–DC) is identical to the one considered in this work (see Section 1.3). The topology chosen by Triphase for the implementation of the single-phase AC–DC modules was a 1-S DAB AC–DC architecture, consisting of a half bridge - full bridge (HBFB) DAB DC–DC converter as the main building block. This converter topology was selected based on the conclusions drawn from extensive literature studies, thorough evaluation of numerous alternative candidate topologies, and the insights gained from the design and testing of a number of 2-S prototype systems. It was identified to have a high potential to enable high performance AC–DC energy conversions. However, a plurality of fundamental research questions arose after the unsuccessful testing of a first 1-S HBFB DAB AC–DC prototype module. This caused the development by Triphase to be stopped temporarily but directly led to the core research topic and converter topology investigated in this Ph.D., and resulted in the definition of the main research objectives outlined in Section 1.5.

In contrast to Triphase, who used a 1-S DAB AC–DC converter that consists of a half bridge - full bridge (HBFB) DAB, in this work the focus is on a 1-S DAB AC–DC converter implemented using a full bridge - full bridge (FBFB) DAB. The reason is that the FBFB DAB has the highest possible flexibility with regard to the

modulation of the DAB's HF AC-link voltages (see Section 2.2.3). Consequently, regarding the realization of the single-phase, utility interfaced, bidirectional, and isolated AC–DC converter specified in Section 1.3, which is to be applied as an on-board electric vehicle (EV) battery charger, the investigated 1-S FBFB DAB AC–DC converter provides a significant advantage compared to the 1-S HBFB DAB AC–DC variant developed by Triphase. Below, the structure of the 1-S DAB AC–DC converter topology is briefly described.

Investigated Single-Stage (1-S) DAB AC–DC Converter

Figure 1.19 shows the general block diagram of the 1-S DAB AC–DC converter investigated in this work, being originally presented in [81, 82]. Thereby, a line voltage rectifier is followed by a bidirectional DAB DC–DC converter (single power conversion stage), putting a small high-frequency (HF) filter capacitor[13] in between. The line voltage rectifier performs a quasi lossless rectification, folding the AC line voltage $v_{\mathrm{AC}}(t)$ into a DC voltage $v_{\mathrm{DC1}}(t)$ that is pulsating at twice the AC line frequency f_{L} and that varies according to the absolute value of $v_{\mathrm{AC}}(t)$. Voltage $v_{\mathrm{DC1}}(t)$ is further fed into the DAB DC–DC converter which, consequently, is operated within a wide input voltage range. Furthermore, the DAB performs the regulation of the DC output voltage V_{DC2} and provides galvanic isolation by means of a HF transformer. For the line voltage rectifier an efficient synchronous rectifier (SR) is preferred over a passive diode bridge in order to reduce the conduction losses and to enable bidirectional power flow. As no energy storage is present in the DC-link (a HF filter capacitor is placed between the SR and the DAB), the power factor correction (PFC) is also performed by the DAB, which has to actively shape its input current[14] $i_{\mathrm{R,o}}(t)$ in phase with its input voltage $v_{\mathrm{DC1}}(t)$. As $i_{\mathrm{R,o}}(t)$ is unfolded towards the AC input side by the SR, a sinusoidal AC input current $i_{\mathrm{AC}}(t)$ that is in phase (unity power factor) with the AC input voltage $v_{\mathrm{AC}}(t)$ is obtained. Only a small HF capacitance is allowed to be put between the SR and the DAB in order to not impair the sinusoidal input current shaping. The DAB handles the double line frequency component of the input power, requiring a LF filter capacitor to be placed at the DC output side in order to limit the output voltage ripple if a constant voltage output is desired.

Besides the fact that the AC–DC energy conversions take place in a single conversion stage, an important advantage of the 1-S DAB AC–DC architecture is that it produces high quality waveforms and is capable of complying to regulations on low and high frequency distortions of the mains AC power lines without the need for increasing the size and reactance value of the passive filter elements [82, 84, 85]. This is due to the fact that the small HF filter capacitors in the DC-link quasi fully

[13] The HF filter capacitor is not shown in Figure 1.19.

[14] The nomenclature '$i_{\mathrm{R,o}}$' is used to indicate that this is the output current of the synchronous rectifier.

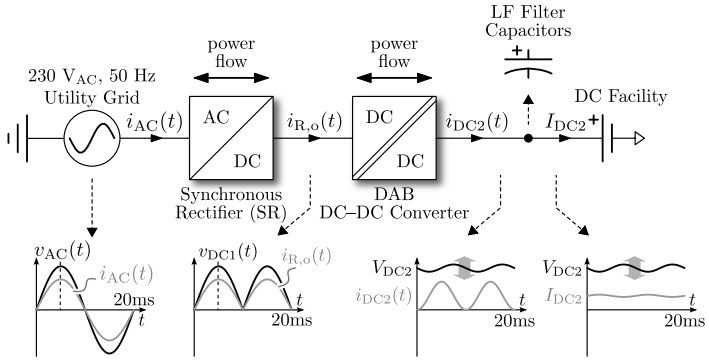


Figure 1.19: General block diagram and principle waveforms of the single-phase, single-stage (1-S), bidirectional, and isolated DAB AC–DC converter investigated in this work.

absorb the HF switched DAB currents and thus act as an inherently integrated input filter. Nevertheless, still an additional EMC filter is required in order to attenuate the remaining HF harmonic distortion on the AC line current. The DAB DC–DC converter (see Chapter 2), as the main building block of this AC–DC topology, is known for its ability to achieve high-efficiency, high-power-density, isolated DC–DC conversion with ultra fast dynamic response and the capability of buck-boost operation as well as bidirectional power flow. Thereby, DABs have the inherent capability to be operated within conditions where quasi zero switching losses occur (i.e. by virtue of zero voltage switching, ZVS), allowing higher switching frequencies to be applied without causing excessive switching losses, which leads to an increased converter power density. The difference between the 1-S DAB AC–DC architecture developed by Triphase (see above) and the one investigated in this work can be found in the particular implementation of the DAB. The 1-S DAB AC–DC developed by Thripase consists of a half bridge - full bridge (HBFB) DAB DC–DC converter while the the 1-S DAB AC–DC investigated in this work consists of a full bridge - full bridge (FBFB) DAB DC–DC converter. The latter has the highest possible degree of freedom to optimally modulate the voltages applied to the terminals of the DAB's HF AC-link. The main differences between the HBFB DAB and the FBFB DAB are summarized in Section 2.2.3 of Chapter 2, also presenting the detailed schematics. The overall schematic of the complete 1-S FBFB DAB AC–DC converter is presented in Chapter 3.

1.5 Objectives and New Contributions

The **main objective** of this work is to investigate the feasibility and suitability of a single-stage (1-S) dual active bridge (DAB) AC–DC converter for the realization of the single-phase, utility interfaced, bidirectional, and isolated energy conversion specified in Table 1.1 of Section 1.3, which relates to an on-board, 3.7 kW, EV battery charger. The main building block of the considered 1-S AC–DC topology is the full bridge - full bridge (FBFB) DAB DC–DC converter which, compared to other DAB variants, provides the highest possible flexibility regarding optimal modulation of the voltages applied to its high-frequency (HF) AC-link terminals.

The **main challenge** to achieve the above objective lies in addressing the major shortcomings of the existing, state-of-the-art analyses and circuit implementations of DAB converters. These shortcomings relate in particular to the (soft-switching) modulation schemes that are available in literature, as well as to the way the HF AC-link of existing DAB converters is implemented, being especially problematic for DAB converters with large input and/or output voltage variations and large power variations such as is the case for the investigated 1-S DAB AC–DC architecture. As a result, the **main focus** of this work is put on the (re)development of the DAB (soft-switching) modulation schemes and on the provision of essential DAB circuit modifications, rather than on subjecting a set of preselected topologies with given modulation schemes to the multi-objective optimization (MOO) procedure outlined in Section 1.1.4. In order to validate the presented analyses and proposed solutions, a **second objective** is to design, build and test a high-efficiency and high-power-density converter prototype system that is designed in order to meet the requirements specified in Section 1.3, and that is developed using state-of-the art design methods/procedures. To some extent, i.e. using local rather than global optimization algorithms, the hardware prototype should be optimized with respect to efficiency and power density.

The **new contributions*** of this work are:

- A new method for the description of the soft-switching (i.e. by virtue of zero voltage switching, ZVS) behavior of DAB converters and a corresponding method which allows to verify whether, for a given set of modulation parameters and circuit variables, ZVS is obtained in all semiconductor power devices of the DAB. This method is named the 'current-dependent charge-based (CDCB) ZVS verification method' since it takes into account the amount of charge that is required to charge the nonlinear parasitic output capacitances of the switches during commutation, as well as the time dependency of the currents available for commutation;
- A complete analysis of all (twelve) switching modes that are possible with the (FBFB) DAB converter;

- The introduction of 'commutation inductances', which are shown to be an essential HF AC-link modification in order to achieve full-operating-range (CDCB) ZVS of a DAB converter;
- A generally applicable, numerical calculation procedure for the derivation of optimal, full-operating-range CDCB ZVS modulation schemes for DAB converters. Contrary to the DAB analyses reported in literature, the proposed numerical optimization algorithm examines all twelve switching modes that are possible with the (FBFB) DAB converter;
- A generally applicable, directly employable analytical solution for the calculation of a full-operating-range CDCB ZVS modulation scheme for DAB converters;
- A generally applicable, semi-analytical calculation procedure for the derivation of a full-operating-range CDCB ZVS modulation scheme for DAB converters;
- Guidelines for the effective selection of the circuit level variables (transformer's turns ratio, the inductances values,...) and of the switching frequency pattern to be applied;
- A guideline for the design, the optimization, and the realization of single-phase, single-stage, bidirectional, and isolated DAB AC–DC converters;
- A framework that includes detailed loss and volume models for the investigated DAB AC–DC converter, enabling local and global system optimizations regarding efficiency and power density, as well as comprehensive comparisons with alternative topology candidates;
- A multi-objective (i.e. with respect to the losses and/or the volume) optimization procedure for the design of magnetic components (i.e. inductors and transformers);
- A fully operational, successfully tested, high-efficiency and high-power-density converter prototype that is in compliance with the requirements specified in Section 1.3, being the first ever reported single-stage DAB AC–DC converter that is operated under full-operating-range ZVS.

*Although the proposed methods for the analysis of DAB converters are demonstrated for the design of a 1-S full bridge - full bridge (FBFB) DAB AC–DC converter topology, they are generally applicable for any conversion type which involves a FBFB DAB (e.g. DC–DC, 1-S AC–DC, 2-S AC–DC, 1-S AC–AC, etc.). With minor adjustments, the methods are also employable for other (less flexible) DAB variants, for example the half bridge - full bridge (HBFB) DAB or the half bridge - half bridge (HBHB) DAB.

1.6 Chapter Overview

In **Chapter 2**, an introduction to the working principle of the soft-switching dual active bridge (DAB) DC–DC converter, which is the main building block of the investigated single-stage (1-S) DAB AC–DC converter, is given. By means of a brief introductory discussion, the shortcomings of the original modulation strategy (i.e. phase-shift modulation, PSM) and soft-switching conditions, and the need for improvements are summarized. Furthermore, a comprehensive overview of the most relevant publications on improved (soft-switching) modulation schemes for DAB converters that have the goal to deal with the deficiencies of the conventional PSM is presented. Lastly, after a brief discussion of the different DAB variants, the full bridge - full bridge (FBFB) DAB implementation is selected as the most suitable candidate for the realization of the 1-S DAB AC–DC converter. Therewith, the main context of the presented work is provided and the focus of the performed research is motivated.

Chapter 3 consists of three major parts. In the first part, the general operating principle of the DAB AC–DC converter is discussed, the exact operating range of the FBFB DAB DC–DC converter, which is the main building block of the AC–DC converter, is derived, and a control equation for the averaged DAB input current is obtained. In the second part, the steady-state analysis of the DAB is presented, considering dual-sided duty-cycle modulation (DSPWM) and including all twelve possible switching modes. Furthermore, 'commutation inductance(s)' are introduced which, using a simple calculation example, are shown to be an essential HF AC-link modification in order to achieve full-operating-range ZVS. In the third part, a novel current-dependent charge-based (CDCB) ZVS verification method is proposed in order to deal with the deficiencies of the existing current-based (CB) and energy-based (EB) ZVS analyses.

Chapter 4 is devoted to the derivation of full-operating-range ZVS modulation schemes for the DAB, which is employed in the investigated 1-S DAB AC–DC converter. Three different approaches are presented, being a numerical approach, an analytical approach, and a semi-analytical approach. All three approaches rely on the CDCB ZVS verification method proposed in Chapter 3, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions.

In **Chapter 5**, the main functional elements of the DAB AC–DC converter are designed, employing the values for the circuit level variables and the CDCB ZVS modulation schemes derived in Chapter 4. Thereby, the partial converter functions are separated and outer (global) optimization loops (i.e. with regard to the circuit level variables and the switching frequency) are omitted. Nevertheless, state-of-the art design methods/procedures, models for the component losses, and volume models are combined with custom developed (local) optimization algorithms in

order to obtain a high-efficiency and high-power-density converter design that is in compliance with the system requirements specified in Table 1.1 of Section 1.3.

In **Chapter 6**, first a DC–DC system characterization is performed, which allows to investigate if the measured HF AC-link voltages and currents are in agreement with the calculated waveforms and, consequently, if ZVS operation is achieved as predicted. This validates the theoretical analysis, i.e. the steady-state converter model and the ZVS analysis presented in Chapter 3, as well as the CDCB ZVS modulation schemes proposed in Chapter 4. In a next step, an AC–DC system characterization is performed, allowing to evaluate the performance of the prototype converter with regard to the reached efficiency and with regard to the quality of the AC input power. Lastly, the system is briefly compared with several (similar) state-of-the-art dual-stage prototype systems reported in literature. The chapter starts with detailing the implementation of the measurement setup that is used to perform above characterizations.

In **Chapter 7** the results obtained are summarized and the conclusions of the work are given. Furthermore, an outlook regarding future research in the field of DAB converters is presented.

The **Appendices** are supplementing the different chapters:

- **Appendix A** is a supplement to Chapter 3: 'Steady-State Operation of the DAB AC–DC Converter', bundling the mode equations for the FBFB DAB and providing additional examples of the mode-related voltage and current waveforms;
- **Appendix B** is a supplement to Chapter 4: 'ZVS Modulation Schemes', providing additional simulation results regarding the ZVS modulation schemes derived in Chapter 4;
- **Appendix C** is a supplement to Chapter 5: ' Modeling of the Main Converter Components', outlining the procedure used for the optimization of the forced-convection-cooled heat sinks of the DAB converter prototype system.

The structure of the thesis is summarized in Figure 1.20, which is a reflection of the different chapters (i.e. 'Ch. 1' ... 'Ch. 6') and which is in strong relation with the flowchart depicted in Figure 1.7 of Section 1.1.4, regarding the design and the local (component level) and global (system level) optimization of power electronic converters. The main difference with Figure 1.7 is that here outer (global) optimization loops are omitted. This means that no top-level iteration of the values for the circuit level variables and of the switching frequency is applied in order to find the global optimum and, consequently, that only local component optimizations are performed with the goal to obtain a high-efficiency and high-power-density converter design.

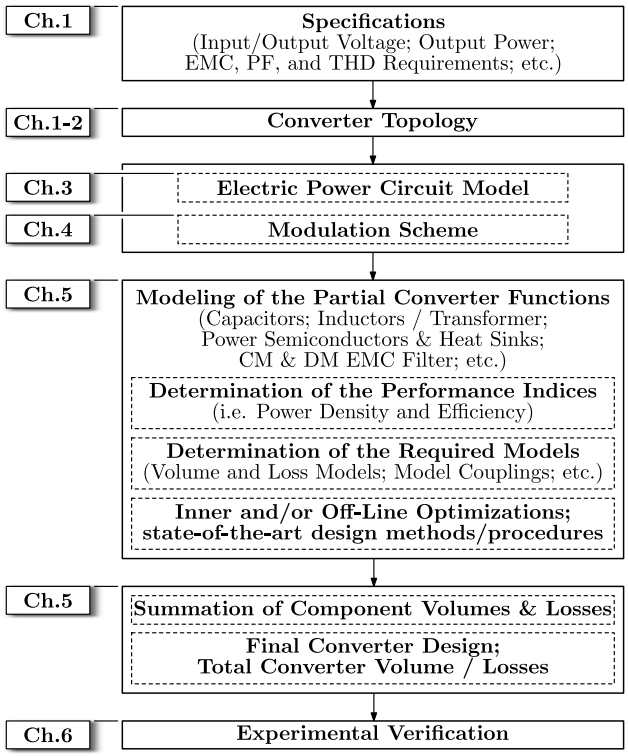


Figure 1.20: Schematic representation of the structure of the thesis, being a reflection of the different chapters (i.e. 'Ch. 1' ... 'Ch. 6').

2

The Dual Active Bridge (DAB) DC–DC Converter

This chapter starts with an introduction to the working principle of the soft-switching dual active bridge (DAB) DC–DC converter, which is the main building block of the investigated single-stage (1-S) DAB AC–DC topology, referring to the original circuit implementation, modulation strategy, and zero voltage switching (ZVS) considerations. In a brief introductory discussion, the shortcomings of the traditional modulation strategy and soft-switching conditions, and the need for improvements are summarized. Thereafter, a comprehensive overview of the most relevant publications on improved (soft-switching) modulation schemes for DAB converters is given, highlighting the parts in the existing DAB analyses that need further investigation. Furthermore, after a brief discussion of the different DAB variants, the full bridge - full bridge (FBFB) DAB implementation is selected as the most suitable candidate for the realization of the investigated 1-S DAB AC–DC converter. Therewith, the main context of the presented work is provided and the focus of the performed research is motivated.

2.1 Introduction: The Original DAB Converter

The dual active bridge (DAB) converter, consisting of two voltage sourced active bridges interfaced by a high-frequency (HF) transformer and optionally an additional (external) series inductor, was originally introduced in [89] (1988) for realizing high-efficiency, high-power-density, isolated DC–DC conversions with ultra fast dynamic response and the capability of buck-boost operation as well as bidirectional power flow. Figure 2.1 shows the circuit schematic of the DAB DC–DC converter in the form that it was proposed in [89] and patented in [90] (publication date: June 25$^{\text{th}}$ 1991; priority date: September 29$^{\text{th}}$ 1989). In the following, the steady-state working principle of the soft-switching DAB converter is explained based on this original circuit implementation, the accompanying modulation scheme, and the applied zero voltage switching (ZVS) considerations. This allows for an introductory discussion (see Section 2.1.4) of the main features of the DAB, the shortcomings of the original modulation strategy and soft-switching (i.e. by virtue of zero voltage switching, ZVS) conditions, and the need for improvements, positioning the context of the presented work. Furthermore, the general considerations given in the following sections serve as a reference base for the derivation of the steady-state equations for the DAB considered for the realization of the 1-S DAB AC–DC converter in Section 3.2. There, contrary to the traditional modulation strategy discussed below (i.e. the phase-shift modulation, PSM), all possible degrees of freedom available for controlling the DAB's active bridges are exploited, providing the highest degree of freedom regarding the search toward optimal ZVS modulation schemes in Chapter 4.

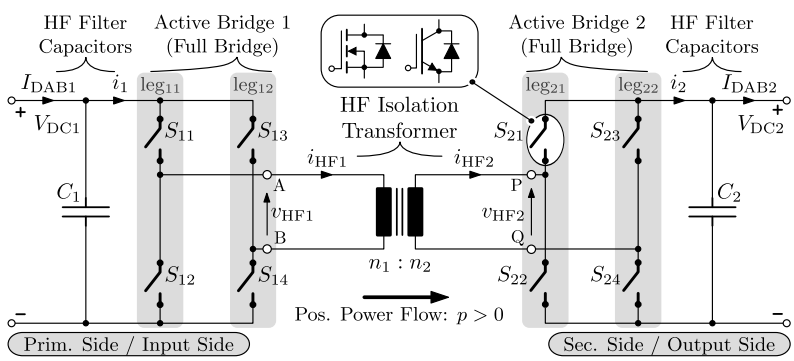


Figure 2.1: Circuit schematic of the bidirectional, isolated dual active bridge (DAB) DC–DC converter topology as originally proposed in [89], consisting of two full bridge circuits (active bridges) interfaced by a HF isolation transformer.

2.1.1 Lossless DAB Model

In [89] and conform Figure 2.1, the two active bridges of the DAB are implemented as full bridge circuits which are composed of active gate controlled switching devices accompanied with anti-parallel freewheeling diodes[1]. Both active bridges produce edge-resonant square wave voltages, further referred to as quasi square wave voltages, $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$ at the terminals of a HF AC-link transformer. Voltage $v_{\mathrm{HF1}}(t)$ is generated by the input bridge and appears between nodes A and B. It has an amplitude $\hat{v}_{\mathrm{HF1}}$ equal to the DC bus voltage of the input bridge, $\hat{v}_{\mathrm{HF1}} = V_{\mathrm{DC1}}$. Voltage $v_{\mathrm{HF2}}(t)$ is generated by the output bridge and appears between nodes P and Q. It has an amplitude $\hat{v}_{\mathrm{HF2}}$ equal to the DC bus voltage of the output bridge, $\hat{v}_{\mathrm{HF2}} = V_{\mathrm{DC2}}$. Generally, in order to simplify the analysis, it is assumed that the resonant transition duration is substantially less than the period of the quasi square waves, allowing to replace the voltage sourced input and output side full bridge circuits by ideal voltage sources v_{HF1} and v_{HF2}. In the ideal case, assuming an infinite transformer magnetizing inductance ($L_{\mathrm{M}} = \infty$), zero transformer winding resistances ($R_{\mathrm{tr1}} = R_{\mathrm{tr2}} = 0\ \Omega$), and zero core losses ($R_{\mathrm{M}} = \infty$), the HF AC-link transformer in Figure 2.1 can be represented as an equivalent series inductance L which is referred to the one or to the other side of the transformer. Using the equivalent circuit model of a transformer according to Figure 2.2 (left inset), and referring the model to the transformer's primary side, the equivalent inductance value L becomes:

$$L = L_{\mathrm{tr1}} + \left(\frac{n_1}{n_2}\right)^2 \cdot L_{\mathrm{tr2}}, \tag{2.1}$$

[1]The anti-parallel freewheeling diodes can be the body diodes of the active switching devices as well as external diodes placed in anti-parallel with the switches, whereas the active switching devices of the bridges can be implemented by a variety of conventionally utilized switching elements with gate controlled turn-off capability such as for example MOSFETs (metal oxide semiconductor field-effect transistors) and IGBTs (insulated gate bipolar transistors).

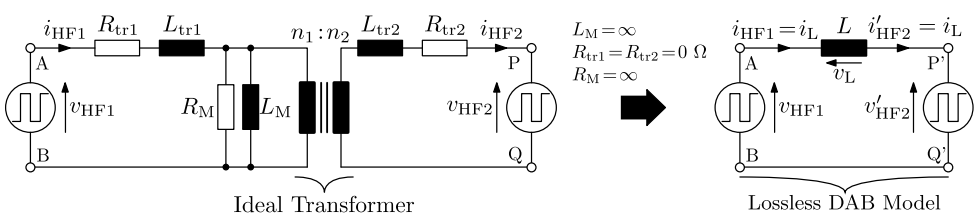


Figure 2.2: Derivation of the lossless FBFB DAB model regarding phase-shift modulation (PSM).

where L_{tr1} and L_{tr2} are respectively the primary and secondary side leakage inductances of the transformer. Thus in its simplest form, neglecting all losses and parasitic elements such as the transformer's coupling capacitances, and assuming instantaneous switching transitions, the DAB converter can be represented by two ideal voltages sources v_{HF1} and v'_{HF2} interfaced by the equivalent series inductance L, where v'_{HF2} is the secondary side AC-link terminal voltage referred to the transformer's primary side:

$$v'_{\mathrm{HF2}}(t) = \frac{n_1}{n_2} \cdot v_{\mathrm{HF2}}(t). \tag{2.2}$$

The resulting lossless DAB model is depicted in Figure 2.2 (right inset). Figure 2.3 shows two examples of the voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$ that are applied to L. According to the original DAB modulation scheme, $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$ are modulated with 50 % duty-cycle and constant frequency (i.e. the switching frequency f_{s}). As a result, the pulse-width modulation (PWM) angles τ_1 and τ_2 of respectively $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, as defined in Figure 2.3, are fixed to $\tau_1 = \tau_2 = T_{\mathrm{s}}/2 \cdot \omega_{\mathrm{s}} = \pi$ radians (rad.), with $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$ the switching period and with $\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$. The (averaged) DAB DC input current I_{DAB1} or the (averaged) DC output current I_{DAB2}, and thus the power transfer, are controlled by solely varying the phase-shift delay ($= \phi/\omega_{\mathrm{s}}$) between $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, as is explained in the following section. This modulation principle is most commonly used to operate the DAB converter and is further referred to as the phase-shift modulation (PSM). The phase-shift angle ϕ is defined as the angle between the falling edge of $v_{\mathrm{HF1}}(t)$ and the falling edge of $v'_{\mathrm{HF2}}(t)$ (see Figure 2.3). Note that τ_1, τ_2, and ϕ are expressed in angular quantities (unit radians; angular axes '$\omega_{\mathrm{s}}t$') for the reason of normalization (i.e. normalized with respect to the switching period T_{s}). It should also be noted that the average values of $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$, evaluated over one switching period during steady-state converter operation (i.e. the DC components of $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$), should be zero in order to avoid saturation of the HF transformer.

Calculation Examples: Used Circuit Level Variables

In the following introductory description of the original DAB converter, the accompanying modulation scheme, and the applied soft-switching considerations, all calculation examples and waveforms are obtained using the circuit level variables of the final prototype converter design:

- $L = 13\ \mu\mathrm{H}$;
- $\frac{n_1}{n_2} = 1$.

Furthermore, for the given examples a switching frequency of $f_s = 120$ kHz is applied. The derivation of the above circuit variables is detailed in Chapter 4.

2.1.2 Phase-Shift Modulation (PSM): Inductor Current, Input and Output Current, and Power Transfer

With the conventional PSM, $v_{HF1}(t)$ and $v'_{HF2}(t)$ are modulated with 50 % duty-cycle (i.e. $\tau_1 = \tau_2 = \pi$ rad.; Figure 2.3). As a result, voltage $v_{HF1}(t)$ alters between the two voltage levels $\hat{v}_{HF1}$ ($= V_{DC1}$) and $-\hat{v}_{HF1}$ ($= -V_{DC1}$) which, within a switching period T_s, are each applied during one uninterrupted half period $T_s/2$. When defining the states ($st_{leg_{1x}}$) of the input bridge legs (the different bridge legs are named in Figure 2.1) as

$$st_{leg_{11}} = \begin{cases} 1 & : \ S_{11} \text{ on, } S_{12} \text{ off,} \\ 0 & : \ S_{11} \text{ off, } S_{12} \text{ on,} \end{cases} \tag{2.3}$$

$$st_{leg_{12}} = \begin{cases} 1 & : \ S_{13} \text{ on, } S_{14} \text{ off,} \\ 0 & : \ S_{13} \text{ off, } S_{14} \text{ on,} \end{cases} \tag{2.4}$$

the two levels of voltage $v_{HF1}(t)$ correspond with:

$$v_{HF1}(t) = \begin{cases} +V_{DC1} & \text{for } st_{leg_{11}}{=}1,\ st_{leg_{12}}{=}0, \\ -V_{DC1} & \text{for } st_{leg_{11}}{=}0,\ st_{leg_{12}}{=}1. \end{cases} \tag{2.5}$$

Note that when a switch S_{xx} is in the on-state, either its transistor T_{xx} or its diode

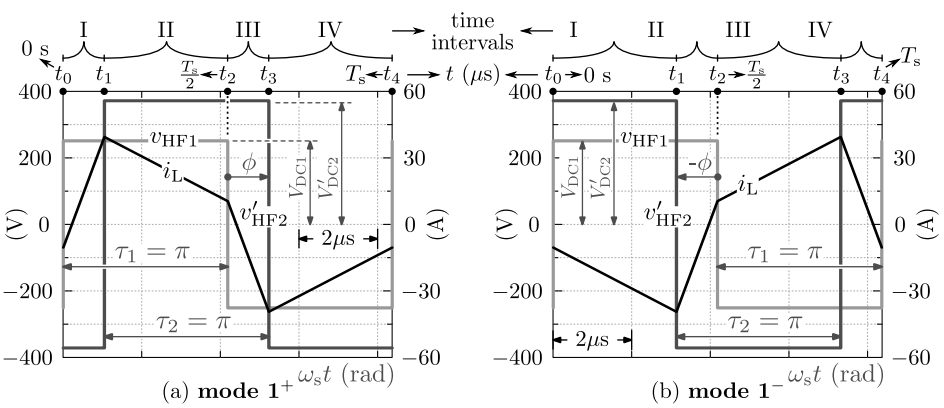


Figure 2.3: Primary side referred AC-link terminal voltages and inductor currents for phase-shift modulation (PSM). (a) Mode 1^+, $\phi \geqslant 0$, positive power flow. (b) Mode 1^-, $\phi \leqslant 0$, negative power flow. The waveforms are derived using $V_{DC1} = 250$ V, $V_{DC2} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, and $f_s = 120$ kHz.

D_{xx} is conducting (conduction state) and when a switch S_{xx} is in the off-state, neither its transistor T_{xx}, neither its diode D_{xx} is conducting (blocking state).

Similarly, voltage $v_{HF2}(t)$ alters between the two voltage levels $\hat{v}_{HF2}$ ($= V_{DC2}$) and $-\hat{v}_{HF2}$ ($= -V_{DC2}$) within a switching period T_s, where

$$v_{HF2}(t) = \begin{cases} +V_{DC2} & \text{for } st_{leg_{21}}{=}1,\ st_{leg_{22}}{=}0, \\ -V_{DC2} & \text{for } st_{leg_{21}}{=}0,\ st_{leg_{22}}{=}1, \end{cases} \tag{2.6}$$

with

$$st_{leg_{21}} = \begin{cases} 1 & : \quad S_{21} \text{ on, } S_{22} \text{ off}, \\ 0 & : \quad S_{21} \text{ off, } S_{22} \text{ on}, \end{cases} \tag{2.7}$$

$$st_{leg_{22}} = \begin{cases} 1 & : \quad S_{23} \text{ on, } S_{24} \text{ off}, \\ 0 & : \quad S_{23} \text{ off, } S_{24} \text{ on}. \end{cases} \tag{2.8}$$

Consequently, the resulting two-level, 50 % duty-cycle voltage patterns $v_{HF1}(t)$, $v_{HF2}(t)$, and $v'_{HF2}(t)$ are determined by:

$$v_{HF1}(t) = V_{DC1} \cdot (st_{leg_{11}} - st_{leg_{12}}), \tag{2.9}$$

$$v_{HF2}(t) = V_{DC2} \cdot (st_{leg_{21}} - st_{leg_{22}}), \tag{2.10}$$

$$v'_{HF2}(t) = \frac{n_1}{n_2} \cdot v_{HF2}(t). \tag{2.11}$$

The sign of the applied phase-shift angle ϕ determines the sequence in time of the rising and falling edges of $v_{HF1}(t)$ and $v'_{HF2}(t)$, and therewith the so called switching mode of the DAB converter. The examples in Figure 2.3 correspond with the two different switching modes that are possible with the conventional PSM, being a mode for positive power flow (further referred to as mode 1^+; Figure 2.3(a)) and a mode for negative power flow (further referred to as mode 1^-; Figure 2.3(b)). Using Figure 2.3, the mode boundary conditions are:

$$\begin{aligned} &\text{mode } 1^+ \text{ (positive power flow, } dir = 1): && 0 \leqslant \phi \leqslant \pi, \\ &\text{mode } 1^- \text{ (negative power flow, } dir = -1): && -\pi \leqslant \phi \leqslant 0, \end{aligned} \tag{2.12}$$

where the power flow direction dir is defined in Figure 2.1 as:

$$dir = \begin{cases} 1 & \text{if } p > 0 : \text{prim.} \rightarrow \text{sec. side (positive power flow)}, \\ -1 & \text{if } p < 0 : \text{sec.} \rightarrow \text{prim. side (negative power flow)}. \end{cases} \tag{2.13}$$

In accordance with Figure 2.2, for each of the two switching modes the dynamics of the inductor current $i_L(t)$ are expressed as:

	t_i for mode 1^+	t_i for mode 1^-
t_0	0	0
t_1	$\dfrac{\phi}{\omega_\mathrm{s}}$	$\dfrac{\pi+\phi}{\omega_\mathrm{s}}$
t_2	$\dfrac{\pi}{\omega_\mathrm{s}}=\dfrac{T_\mathrm{s}}{2}$	$\dfrac{\pi}{\omega_\mathrm{s}}=\dfrac{T_\mathrm{s}}{2}$
t_3	$t_1+\dfrac{T_\mathrm{s}}{2}$	$t_1+\dfrac{T_\mathrm{s}}{2}$
t_4	$t_2+\dfrac{T_\mathrm{s}}{2}=T_\mathrm{s}$	$t_2+\dfrac{T_\mathrm{s}}{2}=T_\mathrm{s}$

Table 2.1: Switching instances $t_0 \dots t_4$ for mode 1^+ and mode 1^-, choosing the rising edge of $v_{\mathrm{HF1}}(t)$ as the time reference t_0 ($= 0$ s).

$$\frac{\mathrm{d}i_\mathrm{L}(t)}{\mathrm{d}t} = \frac{v_\mathrm{L}(t)}{L}, \tag{2.14}$$

were the time dependent inductor voltage $v_\mathrm{L}(t)$ is determined by applying Kirchhoff's voltage low:

$$v_\mathrm{L}(t) = v_{\mathrm{HF1}}(t) - v'_{\mathrm{HF2}}(t) = v_{\mathrm{HF1}}(t) - \frac{n_1}{n_2}\cdot v_{\mathrm{HF2}}(t). \tag{2.15}$$

From Figure 2.3 it can be seen that within one switching period T_s there are four time intervals (numbered with index counter i; $m = 4$) with constant voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, and thus with constant inductor voltage $v_\mathrm{L}(t)$:

$$\begin{aligned}
&\text{time interval I } (i=1): && t_0 < t \leqslant t_1,\\
&\text{time interval II } (i=2): && t_1 < t \leqslant t_2,\\
& && \vdots\\
&\text{final time interval } (i=m): && t_{\mathrm{m}-1} < t \leqslant t_\mathrm{m} = t_0 + T_\mathrm{s}.
\end{aligned} \tag{2.16}$$

Each switching mode (i.e. mode 1^+ and mode 1^- for PSM) is identified by a unique sequence of these time-voltage intervals. The boundaries $t_{\mathrm{i}-1}$ and t_i of a time interval i correspond with a change of voltage $v_{\mathrm{HF1}}(t)$ or voltage $v_{\mathrm{HF2}}(t)$ which is equal to two times the associated DC bus voltage and which, according to (2.5) and (2.6), is initiated by a simultaneous state change of both legs of the particular active bridge. Consequently these boundaries are further referred to as the switching instances[2] of the DAB's active bridges.

[2]Note that within one switching cycle T_s four switching instances take place, e.g. $t_0 \dots t_3$.

For the calculation of $i_{\mathrm{L}}(t)$ in steady-state operation, it can be assumed that the phase shift angle ϕ between voltage $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$ remains the same during the whole switching period T_{s}. Choosing the rising edge of $v_{\mathrm{HF1}}(t)$ as the time reference t_0 (= 0 s; see Figure 2.3), the switching instances $t_0 \ldots t_4$ for the two switching modes are as listed in Table 2.1. The inductor current at a certain switching instant t_{i} is now calculated by rewriting equation (2.14):

$$i_{\mathrm{L}}(t_{\mathrm{i}}) = i_{\mathrm{L}}(t_{\mathrm{i}-1}) + \frac{1}{L}\int_{t_{\mathrm{i}-1}}^{t_{\mathrm{i}}} v_{\mathrm{L}}\mathrm{d}t \quad \forall \quad t_{\mathrm{i}-1} < t_{\mathrm{i}}. \tag{2.17}$$

In steady-state operation, the voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, and thus also the inductor voltage $v_{\mathrm{L}}(t)$ and the inductor current $i_{\mathrm{L}}(t)$, repeat every half-cycle with reversed signs,

$$\begin{aligned} v_{\mathrm{HF1}}(t + T_{\mathrm{s}}/2) &= -v_{\mathrm{HF1}}(t), \\ v'_{\mathrm{HF2}}(t + T_{\mathrm{s}}/2) &= -v'_{\mathrm{HF2}}(t), \\ v_{\mathrm{L}}(t + T_{\mathrm{s}}/2) &= -v_{\mathrm{L}}(t), \\ i_{\mathrm{L}}(t + T_{\mathrm{s}}/2) &= -i_{\mathrm{L}}(t), \end{aligned} \tag{2.18}$$

since it can be assumed that besides ϕ, also the supply voltages V_{DC1} and V_{DC2} remain constant during a switching cycle T_{s}. Therefore, in order to derive the expressions for the inductor current at the different switching instances it is sufficient to establish equation (2.17) in the two first time intervals I and II which occur within $0 < t \leqslant T_{\mathrm{s}}/2$ (see Figure 2.3) while applying (2.18). The resulting systems of equations for mode 1^+ and mode 1^- are respectively:

mode 1^+:

$$\begin{aligned} i_{\mathrm{L}}(t_1) &= i_{\mathrm{L}}(t_0) + \frac{(V_{\mathrm{DC1}} + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\phi}{\omega_{\mathrm{s}}} && : \text{interval I}, \\ i_{\mathrm{L}}(t_2) &= i_{\mathrm{L}}(t_1) + \frac{(V_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(\pi - \phi)}{\omega_{\mathrm{s}}} && : \text{interval II}, \\ i_{\mathrm{L}}(t_2) &= -i_{\mathrm{L}}(t_0). \end{aligned} \tag{2.19}$$

mode 1^-:

$$\begin{aligned} i_{\mathrm{L}}(t_1) &= i_{\mathrm{L}}(t_0) + \frac{(V_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(\pi + \phi)}{\omega_{\mathrm{s}}} && : \text{interval I}, \\ i_{\mathrm{L}}(t_2) &= i_{\mathrm{L}}(t_1) + \frac{(V_{\mathrm{DC1}} + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{-\phi}{\omega_{\mathrm{s}}} && : \text{interval II}, \\ i_{\mathrm{L}}(t_2) &= -i_{\mathrm{L}}(t_0). \end{aligned} \tag{2.20}$$

	$i_{\mathrm{L}}(t_{\mathrm{i}})$ for mode 1^{+}	$i_{\mathrm{L}}(t_{\mathrm{i}})$ for mode 1^{-}
$i_{\mathrm{L}}(t_0)$	$\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2} \cdot (\pi - 2\phi) - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$	$\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2} \cdot (\pi + 2\phi) - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_1)$	$\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2}\pi + \phi - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$	$-\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2}\pi - \phi - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_2) = -i_{\mathrm{L}}(t_0)$	$-\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2} \cdot (\pi - 2\phi) - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$	$-\frac{V_{\mathrm{DC1}} \cdot \left(\frac{d}{2} \cdot (\pi + 2\phi) - \frac{\pi}{2}\right)}{\omega_{\mathrm{s}} L}$

Table 2.2: Expressions for the inductor current $i_{\mathrm{L}}(t)$ at the different switching instances $t_0 \ldots t_2$ within $0 < t \leqslant T_{\mathrm{s}}/2$ for mode 1^{+} and mode 1^{-} operation.

Solving these systems of equations yields the expressions in Table 2.2 for the inductor current $i_{\mathrm{L}}(t)$ at the switching instances $t_0 \ldots t_2$ within $0 < t \leqslant T_{\mathrm{s}}/2$ for both mode 1^{+} and mode 1^{-}. Note that d is the primary side referred voltage conversion ratio:

$$d = \frac{\hat{v}'_{\mathrm{HF2}}}{\hat{v}_{\mathrm{HF1}}} = \frac{V'_{\mathrm{DC2}}}{V_{\mathrm{DC1}}} = \frac{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}{V_{\mathrm{DC1}}}. \tag{2.21}$$

The respective HF AC-link currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ (bridge currents; see Figures 2.2 and 2.1) are calculated with:

$$i_{\mathrm{HF1}}(t) = i_{\mathrm{L}}(t), \tag{2.22}$$

$$i_{\mathrm{HF2}}(t) = \frac{n_1}{n_2} \cdot i'_{\mathrm{HF2}}(t) = \frac{n_1}{n_2} \cdot i_{\mathrm{L}}(t). \tag{2.23}$$

$i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ for the example in Figure 2.3(a) (i.e. for mode 1^{+}) are respectively shown in Figure 2.4(a), depicting the primary side bridge quantities, and in Figure 2.4(b), depicting the secondary side bridge quantities. The states of the different bridge legs that need to be applied during the switching cycle in order to obtain the depicted voltages patterns ($v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$) are also indicated in the figures. Both input and output active bridges act as AC–DC converters to their DC side, transforming the AC-link currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ into net DC currents $i_1(t)$ and $i_2(t)$ at the respective sides. $i_1(t)$ and $i_2(t)$ are also depicted in Figures 2.4(a) and 2.4(b) and are further referred to as the instantaneous DAB input and output currents. They can be derived from respectively $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ by analyzing the (conduction) states of the bridge legs and the associated switching devices that are conducting, yielding:

$$i_1(t) = i_{\mathrm{HF1}}(t) \cdot (st_{\mathrm{leg}_{11}} - st_{\mathrm{leg}_{12}}), \tag{2.24}$$

$$i_2(t) = i_{\mathrm{HF2}}(t) \cdot (st_{\mathrm{leg}_{21}} - st_{\mathrm{leg}_{22}}). \tag{2.25}$$

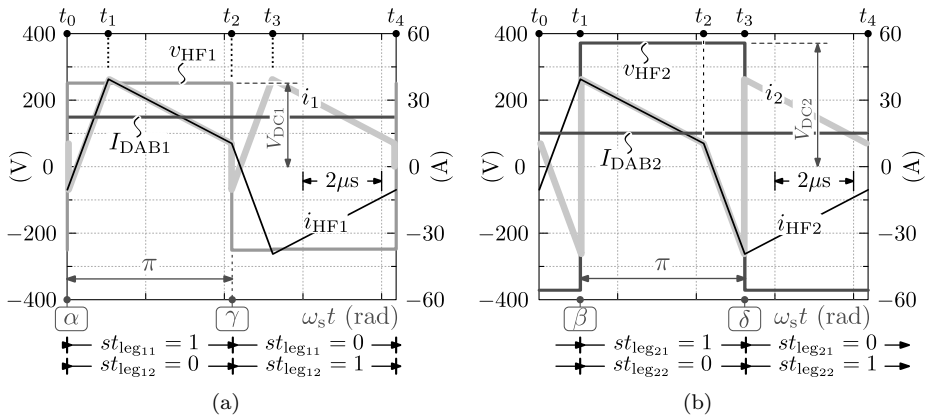


Figure 2.4: (a) Primary side and (b) secondary side bridge quantities (voltages and currents) that correspond with the example in Figure 2.3(a).

Filter capacitors C_1 and C_2 bypass the HF components of $i_1(t)$ and $i_2(t)$ while the DC components I_{DAB1} and I_{DAB2} propagate to the DAB's input and output terminals. I_{DAB1} and I_{DAB2} are further referred to as the averaged DAB input and output currents and are obtained by averaging $i_1(t)$ respectively $i_2(t)$ over one switching period T_{s}, e.g. at a random instant k:

$$I_{\mathrm{DAB1,k}} = i_{1,\mathrm{avg,k}} = \frac{1}{T_{\mathrm{s}}} \int_{kT_{\mathrm{s}}}^{(k+1)T_{\mathrm{s}}} i_1(t)\mathrm{d}t, \tag{2.26}$$

$$I_{\mathrm{DAB2,k}} = i_{2,\mathrm{avg,k}} = \frac{1}{T_{\mathrm{s}}} \int_{kT_{\mathrm{s}}}^{(k+1)T_{\mathrm{s}}} i_2(t)\mathrm{d}t. \tag{2.27}$$

Applying (2.26), the expressions for I_{DAB1} in mode 1^+ and mode 1^- operation are:

$$\text{mode } 1^+: \quad I_{\mathrm{DAB1,1^+}} = \frac{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}} \cdot \phi \cdot (\pi - \phi)}{\omega_{\mathrm{s}} L \pi} \qquad \forall \;\; 0 \leqslant \phi \leqslant \pi, \tag{2.28}$$

$$\text{mode } 1^-: \quad I_{\mathrm{DAB1,1^-}} = \frac{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}} \cdot \phi \cdot (\pi + \phi)}{\omega_{\mathrm{s}} L \pi} \qquad \forall \;\; -\pi \leqslant \phi \leqslant 0. \tag{2.29}$$

The averaged DAB input power, P_1, is finally calculated with:

$$P_1 = I_{\mathrm{DAB1}} \cdot V_{\mathrm{DC1}}. \tag{2.30}$$

The expressions for the averaged DAB output current I_{DAB2} and output power P_2 can be derived in a similar way, or can be obtained by evaluating the DAB's power balance which is:

$$P_1 = P_2, \tag{2.31}$$

since the considered DAB model is lossless. The maximum and minimum achievable averaged DAB input currents $I_{\mathrm{DAB1,max}}$ and $I_{\mathrm{DAB1,min}}$, respectively regarding positive power flow (mode 1^+) and negative power flow (mode 1^-), occur for $\partial I_{\mathrm{DAB1}}/\partial\phi = 0$ with the solutions:

$$I_{\mathrm{DAB1,max}} = \frac{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{8 f_{\mathrm{s}} L} \qquad \text{for } \phi = \pi/2;\ \text{mode } 1^+, \tag{2.32}$$

$$I_{\mathrm{DAB1,min}} = -\frac{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{8 f_{\mathrm{s}} L} \qquad \text{for } \phi = -\pi/2;\ \text{mode } 1^-, \tag{2.33}$$

presenting an upper limit to the employed equivalent inductance value L with respect to the desirable averaged DAB input current. The expressions for the phase-shift angle ϕ, required to achieve a given I_{DAB1}, are derived by rearranging (2.28) and (2.29):

$$\text{mode } 1^+: \qquad \phi_{1^+} = \frac{\pi}{2} \pm \sqrt{\frac{\pi^2}{4} - \frac{I_{\mathrm{DAB1}}\cdot\omega_{\mathrm{s}} L\pi}{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}}, \tag{2.34}$$

$$\text{mode } 1^-: \qquad \phi_{1^-} = -\frac{\pi}{2} \pm \sqrt{\frac{\pi^2}{4} + \frac{I_{\mathrm{DAB1}}\cdot\omega_{\mathrm{s}} L\pi}{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}}. \tag{2.35}$$

Figure 2.5(a) shows the averaged DAB input current I_{DAB1} (black lines) for the complete range of the phase-shift angle (i.e. $-\pi \leqslant \phi \leqslant \pi$) at different DC output voltages V_{DC2} which lie in the range defined in Table 1.1 of Section 1.3. The phase-shift angle $\phi_{\mathrm{A}} = \pi/4$ rad. in Figure 2.5(a) corresponds with the example in Figure 2.3(a) (i.e. mode 1^+ operation; positive power flow; $dir = 1$), which is repeated in Figure 2.5(b), yielding $I_{\mathrm{DAB1}} = 22.2$ A. This angle-current combination (ϕ_{A}, I_{DAB1}) relates to the '$-\sqrt{}$' solution of (2.34). The same averaged DAB input current, $I_{\mathrm{DAB1}} = 22.1$ A, is obtained when calculating ϕ with the '$+\sqrt{}$' solution of (2.34), yielding $\phi_{\mathrm{B}} = 3\pi/4$ rad. However, as can be seen from the gray lines in Figure 2.5(a), the RMS value I_{L} of the inductor current is much higher when using ϕ_{B} instead of ϕ_{A} ($I_{\mathrm{L}} = 24.9$ $\mathrm{A_{rms}}$ for $\phi = \phi_{\mathrm{A}} = \pi/4$ rad. compared to $I_{\mathrm{L}} = 52.9$ $\mathrm{A_{rms}}$ for $\phi = \phi_{\mathrm{A}} = \pi/4$ rad.), leading to unacceptably high conduction losses in the passive elements (inductor, transformer, capacitors) and in the semiconductor power devices. The primary side referred AC-link terminal

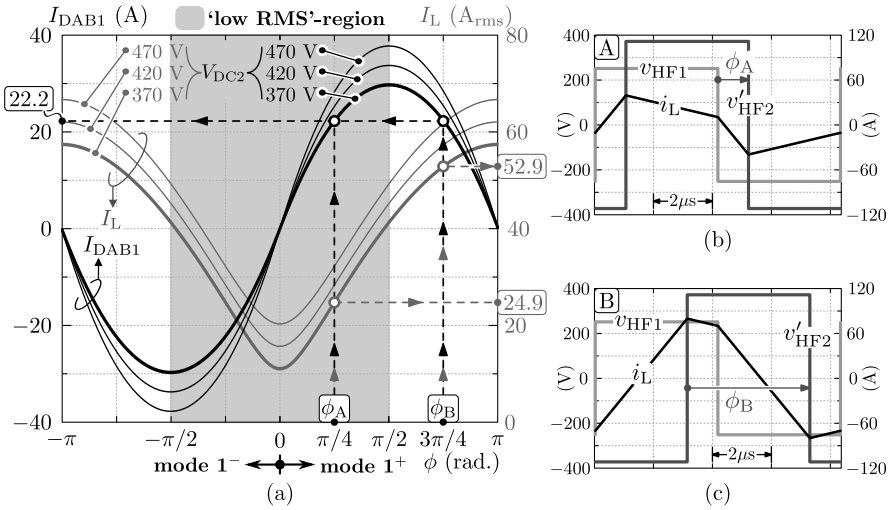


Figure 2.5: (a) Averaged DAB input current I_{DAB1} (black lines) and RMS value of the inductor current I_L (gray lines) for the complete range of the phase-shift angle (i.e. $-\pi \leqslant \phi \leqslant \pi$) at different DC output voltages V_{DC2}. (b)-(c) Primary side referred AC-link terminal voltages and inductor currents for (b) $\phi_A = \pi/4$ rad., mode 1^+, cf. Figure 2.3(a) and for (c) $\phi_B = 3\pi/4$ rad., mode 1^+. The waveforms are derived using $V_{DC1} = 250$ V, $n_1/n_2 = 1$, $L = 13$ μH, and $f_s = 120$ kHz.

voltages and inductor current that correspond with phase-shift angle ϕ_B are depicted in Figure 2.5(c), showing much higher values for $i_L(t)$ and thus increased HF AC-link circulating currents compared to the case for ϕ_A in Figure 2.5(b). Consequently, efficient DAB operation in mode 1^+ (positive power flow; $dir = 1$) is only possible in the region $0 \leqslant \phi \leqslant \pi/2$, where ϕ is calculated with the '$-\sqrt{}$' solution of (2.34). Similarly, for mode 1^- the efficient DAB operating region lies in the interval $-\pi/2 \leqslant \phi \leqslant 0$, where ϕ needs to be calculated with the '$+\sqrt{}$' solution of (2.35). By combining these solutions, a single expressions for the phase-shift angle ϕ is obtained that is valid for both operating modes and that should be used in order to assure low-loss DAB operation in the region $-\pi/2 \leqslant \phi \leqslant \pi/2$:

$$\text{mode } 1^+ \text{ \& mode } 1^- : \phi = dir \cdot \left(\frac{\pi}{2} - \sqrt{\frac{\pi^2}{4} - dir \cdot \frac{I_{DAB1} \cdot \omega_s L \pi}{\frac{n_1}{n_2} \cdot V_{DC2}}} \right) \tag{2.36}$$

$$\rightarrow \text{ assuring: } -\pi/2 \leqslant \phi \leqslant \pi/2.$$

Note that the RMS value of the inductor current at a random instant k is calculated with:

$$I_{\mathrm{L,k}} = \sqrt{\frac{1}{T_\mathrm{s}} \int_{kT_\mathrm{s}}^{(k+1)T_\mathrm{s}} \left(i_\mathrm{L}(t)\right)^2 \mathrm{d}t}, \tag{2.37}$$

As can be seen from Figure 2.5(a), and as predicted by (2.32)-(2.33), the values $\phi = \pi/2$ and $\phi = -\pi/2$ result in the maximum respectively the minimum averaged DAB input currents ($I_{\mathrm{DAB1,max}}$ resp. $I_{\mathrm{DAB1,min}}$).

2.1.3 Current-Based Zero Voltage Switching (CB ZVS) Conditions

DAB converters can be operated in a soft-switched manner in which automatic and lossless resetting of the intrinsic parasitic output capacitances of the switching devices occurs trough an appropriate recirculation of the trapped energy [89, 90]. This capability to eliminate losses associated with the switch capacitances results in dramatically reduced semiconductor switching losses, enabling an increased switching frequency to be applied in order to reduce the volume of the system compared to hard-switching converters.

The soft-switching behavior of the DAB relies on the zero voltage switching (ZVS) principle. Thereby it must be ensured that turn-on of a switch only takes place when its anti-parallel diode is conducting. If this condition is fulfilled, the drain to source[3] voltage of the switch is quasi zero at turn-on, almost completely eliminating the turn-on losses. A detailed description of the ZVS principle is given in Section 3.3 of Chapter 3. There is can be seen that ZVS commutation of a bridge leg involves three steps:

1. Initiation of the leg commutation by turn-off of the switch which is initially in the conduction state, i.e. the switch which conducts the current before the moment of commutation;
2. Automatic resetting of the parasitic switch capacitances by a resonance that takes place between the switch output capacitances and the HF AC-link inductances;
3. Turn-on of the switch which is initially in the blocking state after its anti-parallel diode in put into conduction by the above resonance.

It is shown in Section 3.3 that not only ZVS turn-on but also ZVS turn-off can be achieved by the effective exploitation of the highly nonlinear characteristic of

[3]Remind that in this work MOSFETs are the primary considered semiconductor switching devices.

the MOSFET's output capacitances. The resetting of the switch capacitances and the associated state change of the corresponding bridge leg thus involves a resonance between the switch output capacitances on the one hand and the HF AC-link inductances on the other, causing the HF AC-link terminal voltages to be edge-resonant square waves (also called quasi square waves). The description of the DAB's ZVS conditions given in [89, 90], however, does not take into account this resonant transition and neglects the energy resetting mechanism. The parasitic switch capacitances are thus not included in the analysis and it is assumed that ZVS of a bridge leg is achieved when the drain to source current $i_{\mathrm{DS,S_{xx}}}$ of the switch S_{xx} which initiates the commutation, i.e. the switch which is turned off, is positive at the switching instant. Expressions which describe this 'current-based (CB)' ZVS condition can be obtained by analyzing the drain to source currents of the individual switches:

Primary side active bridge:

$$i_{\mathrm{DS,S_{11}}} = st_{\mathrm{leg_{11}}} \cdot i_{\mathrm{HF1}}, \tag{2.38}$$

$$i_{\mathrm{DS,S_{12}}} = (st_{\mathrm{leg_{11}}} - 1) \cdot i_{\mathrm{HF1}}, \tag{2.39}$$

$$i_{\mathrm{DS,S_{13}}} = -st_{\mathrm{leg_{12}}} \cdot i_{\mathrm{HF1}}, \tag{2.40}$$

$$i_{\mathrm{DS,S_{14}}} = (1 - st_{\mathrm{leg_{12}}}) \cdot i_{\mathrm{HF1}}, \tag{2.41}$$

Secondary side active bridge:

$$i_{\mathrm{DS,S_{21}}} = -st_{\mathrm{leg_{21}}} \cdot i_{\mathrm{HF2}}, \tag{2.42}$$

$$i_{\mathrm{DS,S_{22}}} = (1 - st_{\mathrm{leg_{21}}}) \cdot i_{\mathrm{HF2}}, \tag{2.43}$$

$$i_{\mathrm{DS,S_{23}}} = st_{\mathrm{leg_{22}}} \cdot i_{\mathrm{HF2}}, \tag{2.44}$$

$$i_{\mathrm{DS,S_{24}}} = (st_{\mathrm{leg_{22}}} - 1) \cdot i_{\mathrm{HF2}}. \tag{2.45}$$

The drain to source currents $i_{\mathrm{DS,S_{xx}}}$ and corresponding drain to source voltages $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} of the DAB, regarding mode 1^+ operation according to the example in Figure 2.3(a), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure 2.4, are shown in Figures 2.6(a)-2.6(b) (switches $S_{1\mathrm{x}}$ of the primary side active bridge) and Figures 2.6(c)-2.6(d) (switches $S_{2\mathrm{x}}$ of the secondary side active bridge). The turn-off currents of the individual switches are indicated by a '★' and are clearly positive, confirming that CB ZVS is achieved.

By analyzing the current and voltage patterns for the two different switching modes, the CB ZVS criterion in [89, 90], in which the condition $i_{\mathrm{DS,S_{xx}}}(t = t_{\mathrm{turn-off}}) \geqslant 0$ needs to be fulfilled, can be translated into a general set of CB ZVS constraints. By defining

- t_α: switching instant that corresponds with the rising edge of $v_{\mathrm{HF1}}(t)$, i.e.
  - Mode 1^+: $t_\alpha = t_0$, $i_{\mathrm{HF1}}(t_\alpha) = i_{\mathrm{HF1}}(t_0)$;
  - Mode 1^-: $t_\alpha = t_0$, $i_{\mathrm{HF1}}(t_\alpha) = i_{\mathrm{HF1}}(t_0)$;
  - Multiplier[4] $s^\pm = -1$.

[4]Multiplier $s^\pm$ is introduced and used throughout the text in order to bring generality to the DAB's ZVS conditions/equations (see inter alia (2.46)).

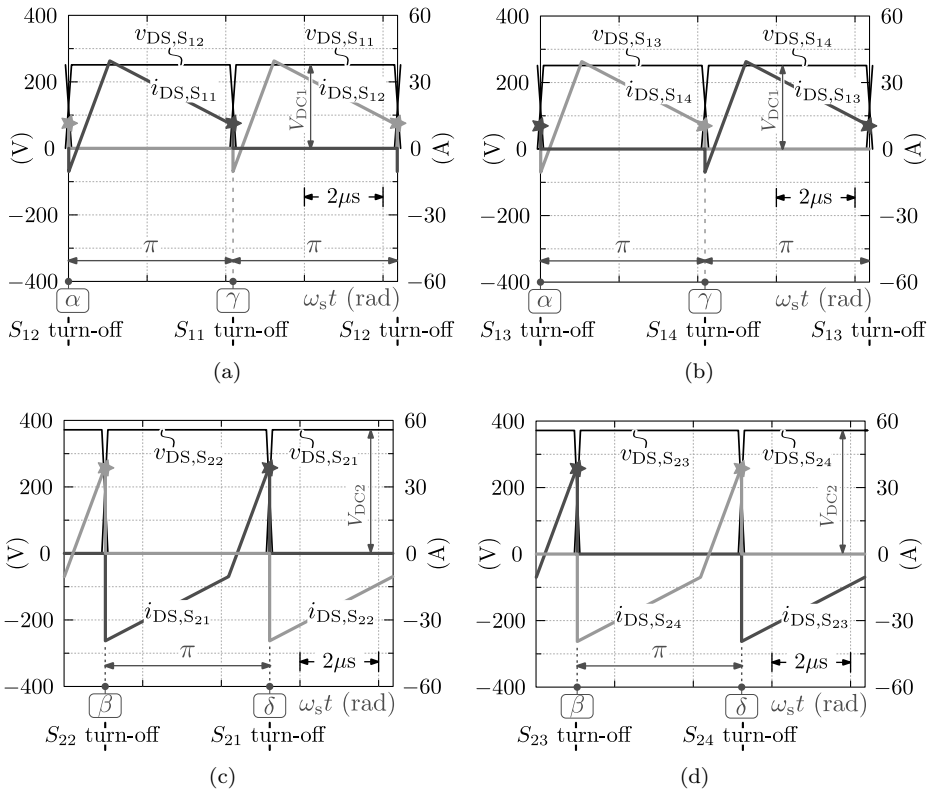


Figure 2.6: Drain to source currents $i_{\mathrm{DS,S_{xx}}}$ and corresponding drain to source voltages $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} of the DAB regarding mode 1^+ operation according to the example in Figure 2.3(a), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure 2.4. (a)-(b) Switches $S_{1\mathrm{x}}$ of the primary side active bridge: (a) bridge leg_{11}, (b) bridge leg_{12}. (c)-(d) Switches $S_{2\mathrm{x}}$ of the secondary side active bridge: (c) bridge leg_{21}, (d) bridge leg_{22}.

- t_β: switching instant that corresponds with the rising edge of $v_{\mathrm{HF2}}(t)$, i.e.
  - Mode 1^+: $t_\beta = t_1$, $i_{\mathrm{HF2}}(t_\beta) = i_{\mathrm{HF2}}(t_1)$;
  - Mode 1^-: $t_\beta = t_3$, $i_{\mathrm{HF2}}(t_\beta) = i_{\mathrm{HF2}}(t_3) = -i_{\mathrm{HF2}}(t_3 - T_\mathrm{s}/2) = -i_{\mathrm{HF2}}(t_1)$;
  - Multiplier $s^\pm = 1$.
- t_γ: switching instant that corresponds with the falling edge of $v_{\mathrm{HF1}}(t)$, i.e.
  - Mode 1^+: $t_\gamma = t_2$, $i_{\mathrm{HF1}}(t_\gamma) = i_{\mathrm{HF1}}(t_2)$;

  - Mode 1^-: $t_\gamma = t_2$, $i_{\mathrm{HF1}}(t_\gamma) = i_{\mathrm{HF1}}(t_2)$;
  - Multiplier $s^\pm = 1$.

- t_δ: switching instant that corresponds with the falling edge of $v_{\mathrm{HF2}}(t)$, i.e.
  - Mode 1^+: $t_\delta = t_3$, $i_{\mathrm{HF2}}(t_\delta) = i_{\mathrm{HF2}}(t_3) = -i_{\mathrm{HF2}}(t_3 - T_\mathrm{s}/2) = -i_{\mathrm{HF2}}(t_1)$;
  - Mode 1^-: $t_\delta = t_1$, $i_{\mathrm{HF2}}(t_\delta) = i_{\mathrm{HF2}}(t_1)$;
  - Multiplier $s^\pm = -1$.

the generalized set of CB ZVS constraints becomes:

$$\begin{aligned} s^\pm \cdot i_{\mathrm{HF1}}(t_\alpha) &\geqslant 0, & s^\pm \cdot i_{\mathrm{HF2}}(t_\beta) &\geqslant 0, \\ s^\pm \cdot i_{\mathrm{HF1}}(t_\gamma) &\geqslant 0, & s^\pm \cdot i_{\mathrm{HF2}}(t_\delta) &\geqslant 0. \end{aligned} \tag{2.46}$$

By using equations (2.22)-(2.23) and by applying the expressions for the inductor current at the different switching instances in Table 2.2, and subsequently solving for d, these CB ZVS constraints are translated into:

$$\underbrace{\left(d_\mathrm{l} = 1 - dir \cdot \frac{2\phi}{\pi}\right)}_{\text{Sec. side bridge ZVS limit}} \leqslant d \leqslant \underbrace{\left(\frac{1}{1 - dir \cdot \frac{2\phi}{\pi}} = d_\mathrm{u}\right)}_{\text{Prim. side bridge ZVS limit}}. \tag{2.47}$$

Consequently, for a certain phase-shift angle ϕ (cf. (2.36)) and a certain power flow direction dir (cf. (2.13)), the efficient CB ZVS operating region of the DAB is limited by the primary side referred voltage conversion ratio d which is defined by (2.21). d_u corresponds with the CB ZVS boundary for the primary side active bridge while d_l corresponds with the CB ZVS boundary for the secondary side active bridge. Figure 2.7 depicts the CB ZVS region within the 'low-RMS' region (i.e. $-\pi/2 \leqslant \phi \leqslant \pi/2$) defined in Figure 2.5(a). For the voltage conversion ratio used for the calculation examples shown in Figure 2.3, i.e. $d = 1 \cdot 370/250 = 1.48$, the CB ZVS region is thus defined by d_u (i.e. the ZVS boundary for the secondary side active bridge, see top inset of Figure 2.7), yielding that CB ZVS within the 'low-RMS' region of the DAB is achieved when $0.51 \leqslant \phi \leqslant \pi/2$ rad. and when $-\pi/2 \leqslant \phi \leqslant -0.51$ rad. (see Figure 2.7, bottom inset). The means that hard-switching operation occurs in the region $-0.51 < \phi < 0.51$ rad., i.e. at low averaged DAB input currents I_{DAB1} (cf. (2.28)-(2.29), see also Figure 2.7 (bottom inset)) and thus at low power levels.

Note that similar to τ_1, τ_2, and ϕ, for the reason of normalization, switching instances $t_{\theta_\mathrm{i}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ (time axes) can be translated into angular quantities $\theta_\mathrm{i} = \{\alpha, \beta, \gamma, \delta\}$ (unit radians; angular axis) defined by $\theta = \omega_\mathrm{s} t$, e.g. $\alpha = \omega_\mathrm{s} \cdot t_\alpha$, as shown in Figures 2.4 and 2.6 (mode 1^+).

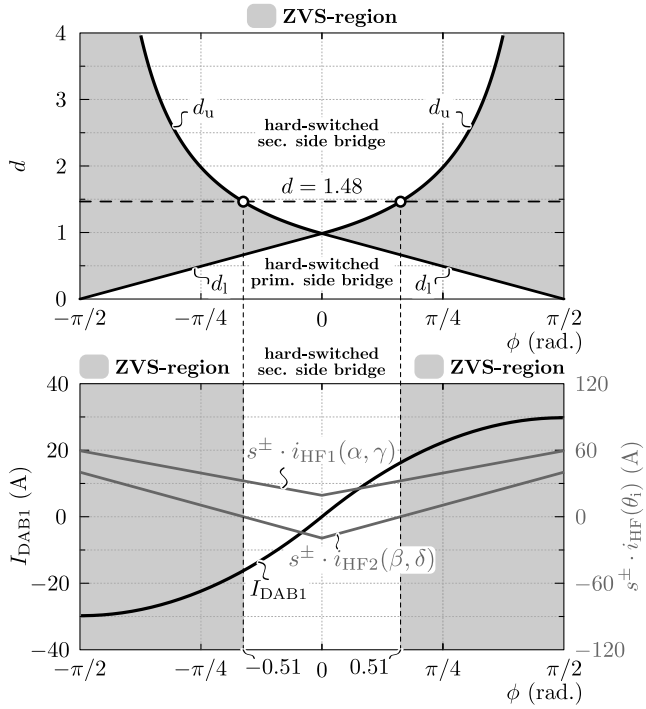


Figure 2.7: CB ZVS regions for the full bridge - full bridge DAB operated with phase-shift modulation (PSM). The figure is obtained using $n_1/n_2 = 1$, $L = 13$ μH, and $f_\mathrm{s} = 120$ kHz.

2.1.4 Discussion

The main idea behind the invention of the DAB DC–DC converter is to combine the best of two worlds. On the one hand *hard-switching pulse-width modulation (PWM) topologies* operate with quasi no (reactive) circulating power and have a large dynamic range while, on the other hand, *resonant topologies* are able to operate in a soft-switching manner (i.e. with quasi zero switching losses) with a reduced electromagnetic interference (EMI) and an effective utilization of component parasitics but, however, with strongly increased circulating power and a limited dynamic range. The DAB converter is a resonant transition topology in which edge-resonant square wave voltages (also called quasi square wave voltages) are applied across an equivalent inductance L that serves as the main energy transfer element. Thereby, the DAB is controlled as a voltage dependent current source and can be operated under soft-switching conditions (i.e. by virtue of zero voltage switching, ZVS) with utilization of component parasitics (e.g. the transformer's

leakage inductances) and with only a moderate increase of the circulating power compared to the hard-switching PWM topologies. Therewith, high-efficiency, high-power-density, isolated DC–DC conversions with ultra fast dynamic response and the capability of buck-boost operation as well as bidirectional power flow can be realized. However, the original modulation scheme presented in [89] and detailed in Section 2.1.2, operates the full bridges of the DAB with maximum (i.e. 50 %) duty-cycles and solely adjusts the phase-shift angle ϕ between the HF AC-link terminal voltages v_{HF1} and v_{HF2} in order to achieve a certain averaged input current I_{DAB1} and input power P_1. The only modulation parameter is thus the phase-shift angle ϕ between $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$:

$$\mathbf{x} = (\phi). \tag{2.48}$$

This modulation scheme, termed phase-shift modulation (PSM), facilitates simple control of the DAB but, however, suffers from a limited soft-switching range (see Section 2.1.3). Moreover, due to the limit degrees of freedom available[5] to modulate the HF AC-link voltages and to tailor the HF AC-link currents, a significantly increased reactive circulating power is obtained for voltage conversion ratios $d \gg 1$ or $d \ll 1$ (d is defined by equation (2.14)), leading to increased losses and a reduced conversion efficiency. High converter efficiencies are thus only achievable at rated power and for $d \approx 1$ [91]. Consequently, the traditional PSM is problematic for DAB converters that are operated within wide input and/or output voltage ranges, such as is the case for the single-stage (1-S) DAB AC–DC converter investigated in this work, where the input voltage of the DAB is a rectified (folded) sine-wave, implying a highly variable voltage conversion ratio.

[5]Note that besides the phase-shift angle ϕ, also the switching frequency f_{s} can be adjusted.

2.2 The DAB Converter: Literature Overview

Ever since its introduction in 1989, research on the DAB converter has been focusing on several topics such as for example modulation schemes, steady-state and dynamic characteristics, converter control,... However, due to the general demand for high conversion efficiency and/or power density, research on improved DAB modulation schemes has been particularly prominent. In order to enable an improved converter performance, the majority of these modulation schemes tries to deal with the above mentioned deficiencies of the conventional phase-shift modulation (PSM), being a limited ZVS operating range and large RMS currents in the HF AC-link for most operating points when the DAB is operated within wide voltage ranges [92]. Whether the DAB is used in a DC–DC, a 1-S AC–DC (this work), or any other configuration, one of the main goals has been to optimally (i.e. minimizing a certain, mostly loss related, cost function) operate the DAB within conditions where quasi zero switching losses occur (i.e by virtue of zero voltage switching, ZVS). Therefore, below, publications on DAB modulation schemes are classified according their ZVS considerations.

2.2.1 Current-Based (CB) ZVS Modulation Schemes

The largest group of publications does not take into account the parasitic output capacitances of the DAB's semiconductor power devices and assumes that ZVS of a bridge leg is achieved when the drain to source current of the switch which initiates the commutation (turn-off) is positive at the switching instant. These conditions are in accordance with the first publication on the DAB [89] (1988), and are discussed in Section 2.1.3. Besides the traditional phase-shift-modulation (PSM[6]) outlined above, where full-power-range ZVS is only possible at a voltage conversion ratio d equal to one [82, 89], modulation schemes with increased degree of freedom regarding the search toward an optimal CB ZVS scheme are introduced. These schemes combine PSM with either single-sided duty-cycle modulation (further referred to as SSPWM) or dual-sided duty-cycle modulation (further referred to as DSPWM, highest degree of freedom) and use a low power and a high power switching mode in order to reduce the reactive circulating power in the HF AC-link, to lower the transformer's core flux, and to obtain full-operating-range CB ZVS [93]. Especially DSPWM enables significant improvements for low-load operation and for widely varying input and/or output voltage ranges such as is the case for the investigated 1-S AC–DC converter, where the DAB input voltage is a rectified sine-wave (see Figure 1.19) and d is highly variable [74]. Simple suboptimal solutions for the calculation of the modulation parameters in order to achieve full-operating-

[6]PSM: the two active bridges are operated to generate 50 % duty-cycle high-frequency AC-link voltages which are phase-shifted relative to each other in order to achieve the required power transfer (one degree of freedom).

range CB ZVS are given in [83, 94] using SSPWM, and in [84] using DSPWM. A SSPWM scheme for minimizing the reactive circulating power is presented in [95]. In [92] an optimal DSPWM scheme with respect to minimum inductor RMS current values is proposed.

2.2.2 Energy-Based (EB) ZVS Modulation Schemes

It was already shown in [96] that when considering CB ZVS, substantial parts of the calculated ZVS regions involve incomplete bridge commutations due to the presence of (parasitic) switch output capacitances. Consequently, the above mentioned CB ZVS modulation schemes result in (partly) hard-switching operation for certain intervals of the operating range[7], leading to reduced efficiency and in the worst case destruction of the semiconductor switching devices. The influence of the parasitic output capacitances of the semiconductor switching devices on the (resonant) bridge commutations is described in [85, 96–99] by evaluating the energy balance between the switch capacitances and the HF AC-link inductances (energy-based (EB) ZVS). However, in [85, 97] the state of the one active bridge is not taken into account in the ZVS verification of the other, leading to easy implementable but incomplete EB ZVS constraints. A simple suboptimal modulation scheme based on these simplified constraints is presented in [85] using SSPWM and variable switching frequency (f_s) control[8]. However, EB ZVS could not be fully achieved for the low power mode and the transition between the low and high power modes encompasses highly undesirable discontinuous steps in the modulation variables. The harder to implement EB ZVS constraints given in [96, 98, 99] are still incomplete as the state of the one active bridge is taken into account in the ZVS verification of the other, but, however, a (quasi) simultaneous state change within the one and/or together with the other active bridge is not allowed. Therefore in [98] simplifications had to made, yielding a suboptimal modulation scheme which uses DSPWM and variable f_s. Full-operating-range EB ZVS was reported but, again, the mode transition involves discontinuous steps. Additionally, EB ZVS analyses are typically based on constant energy equivalent switch capacitances [85] which can result in significant errors [101].

2.2.3 DAB Variants

It should be noted that some of the DAB modulation schemes reported in literature relate to an implementation of the DAB converter which differs from the original circuit schematic shown in Figure 2.1. This difference relates to the implementation

[7]This effect is most pronounced in the regions where $d >> 1$ and along the boundary between the low power and the high power switching mode [96].

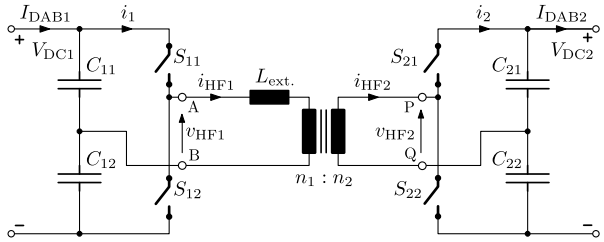
[8]In [100] it is shown that the use of a variable switching frequency f_s enables improved DAB efficiency.

possibilities of the two active bridges. For each active bridge (input and output side) the switching devices can be connected in a half bridge configuration or a full bridge configuration. This results in the following four possibilities (see Figure 2.8):

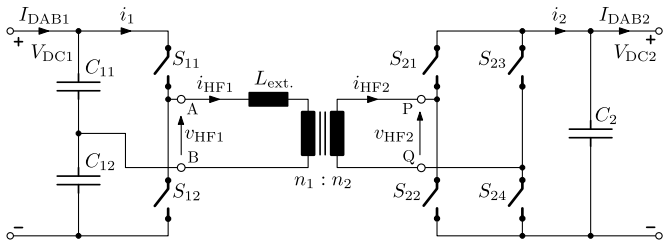
- Half bridge - half bridge (HBHB) DAB; Figure 2.8(a); DAB consisting of a half bridge circuit at both the input and the output side of the converter;
- Half bridge - full bridge (HBFB) DAB; Figure 2.8(b); DAB consisting of a half bridge circuit at the input side of the converter and a full bridge circuit at the output side of the converter;
- Full bridge - half bridge (FBHB) DAB; Figure 2.8(c); DAB consisting of a full bridge circuit at the input side of the converter and a half bridge circuit at the output side of the converter;
- Full bridge - full bridge (FBFB) DAB; **this work**; Figure 2.8(d); DAB consisting of a full bridge circuit at both the input and the output side of the converter.

The main difference in the above DAB implementations[9] lies in the difference in amplitude and shape of the quasi square wave voltages $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$ generated by each active bridge and applied to the terminals of the HF AC-link. Using a half bridge configuration, an active bridge can produce a two-level, 50 % duty-cycle terminal voltage with an amplitude equal to half the DC voltage of the respective bridge. Using a full bridge configuration, an active bridge can produce a three-level $\leqslant$ 50 % duty-cycle terminal voltage with an amplitude equal to the DC voltage of the respective bridge. As a result, the degrees of freedom available for modulating the voltage $v_{\mathrm{L}}(t)$ which appears across the equivalent series inductance L, and thus for wave-shaping the resulting $i_{\mathrm{L}}(t)$, increase with the number of full bridges used in the DAB. Moreover, as the amplitude of the terminal voltage generated by a full bridge is twice the value of the amplitude that is generated by a half bridge, generally the HF AC-link currents decrease with the number of full bridges. However, this does not necessarily lead to lower conduction losses as the number of switching devices in the current path is higher for a full bridge (i.e. two switching devices in the current path) compared to a half bridge (i.e. one switching device in the current path). For the four previously mentioned implementations of the DAB converter, Figure 2.9 show examples of typical HF AC-link voltage and current waveforms. In this work, the FBFB DAB implementation (see Figure 2.8(d)) is selected as the most suitable candidate for the realization of the investigated 1-S DAB AC–DC converter since it provides the highest possible flexibility regarding the modulation of the HF AC-link terminal voltage $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$, implying a better capability to achieve soft-switching operation within the whole operating range compared to the other DAB variants.

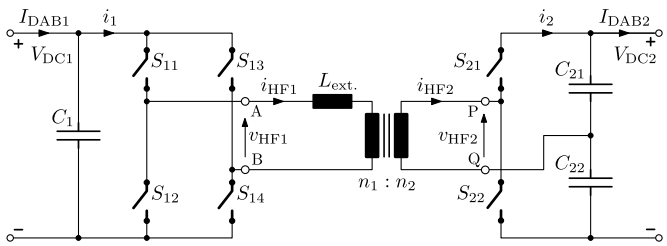
[9]Note that for all DAB implementations shown in Figure 2.8, bidirectional power flow is possible.



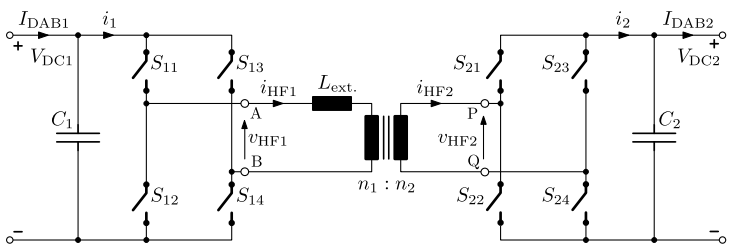
(a) Half bridge - half bridge (HBHB) DAB



(b) Half bridge - full bridge (HBFB) DAB

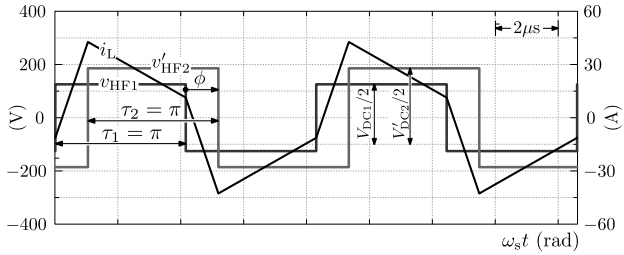


(c) Full bridge - half bridge (FBHB) DAB

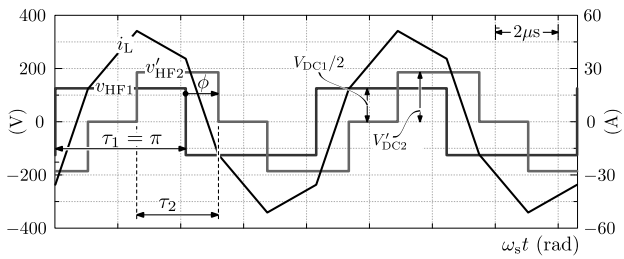


(d) Full bridge - full bridge (FBFB) DAB

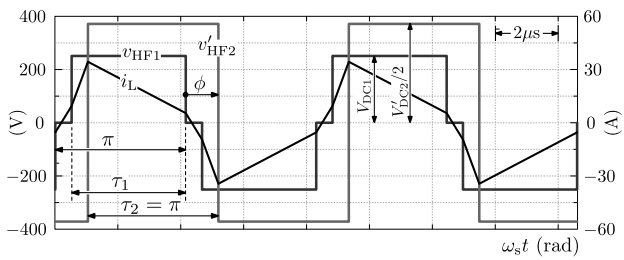
Figure 2.8: Four different DAB implementations.



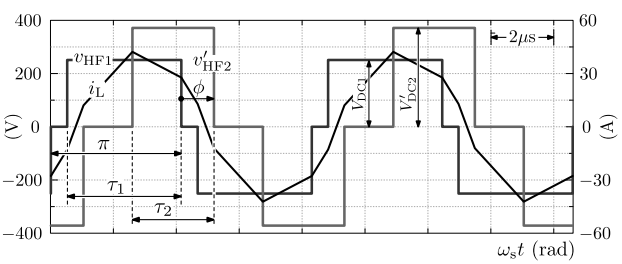
(a) Typical waveforms for the HBHB DAB.



(b) Typical waveforms for the HBFB DAB.



(c) Typical waveforms for the FBHB DAB.



(d) Typical waveforms for the FBFB DAB.

Figure 2.9: Examples of typical HF AC-link voltage and current waveforms for the four DAB converter implementations shown in Figure 2.8.

2.2.4 General Lossless DAB Model

Contrary to the schematic of the original DAB (Figure 2.1), for generality in Figures 2.8(a)-2.8(d) an additional (external) inductor L_{ext} is used in series with the transformer. Nevertheless, under the same assumptions as in Section 2.1, the equivalent AC-link circuit model can still be reduced to a single series inductance L, which is referred to the one or to the other side of the HF transformer (see Figure 2.10). Now the equivalent inductance value L has to be calculated with:

$$L = L_{\text{ext}} + L_{\text{tr1}} + \left(\frac{n_1}{n_2}\right)^2 \cdot L_{\text{tr2}}. \tag{2.49}$$

For a HF AC-link which consists of a transformer and external series inductance L_{ext} (i.e. two discrete components), typically the combined VA (power) rating is higher than is the case for a 'composite' transformer where the external inductance L_{ext} is integrated in the transformer's leakage inductances [89]. As for a given operating frequency, lower VA ratings lead to a decreased size, and as fewer magnetic components are needed, composite transformers enable an increased power density of the system. Moreover, composite transformers have lower core losses (efficiency) and involve simple connections [102–104]. However, the natural leakage inductance of the transformer might not be large enough for this purpose, especially when a considerably high equivalent inductance value L is required and when the applied switching frequencies are rather modest. This problem can be addressed by for example inserting a magnetic shunt into the transformer core [102–104]. Nevertheless, the use of an external inductor L_{ext} is a more straightforward and easy solution, especially concerning design complexity, cooling requirements, and reproducibility. For this reason it is decided to use a combination of a transformer with external inductor L_{ext} for the realization of the 1-S DAB AC–DC converter investigated in this work.

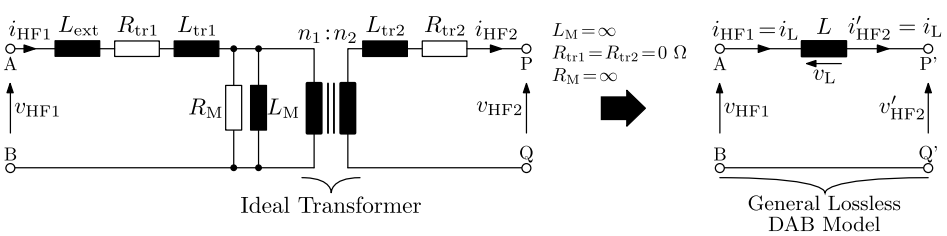


Figure 2.10: General lossless DAB model, involving an external series inductor L_{ext} placed at the transformer's primary side.

2.3 Conclusion

In order to provide the main context of the presented work and in order to motivate the focus of the performed research, in this chapter an introduction (see Section 2.1) to the working principle of the soft-switching dual active bridge (DAB) DC–DC converter, which is the main building block of the investigated single-stage (1-S) DAB AC–DC architecture, is given, referring to the original circuit implementation, modulation strategy, and zero voltage switching (ZVS) considerations. The disadvantages of the original DAB modulation scheme, which is termed phase-shift modulation (PSM), are:

- Using PSM, the soft-switching (i.e. by virtue of zero voltage switching, ZVS) range of the DAB is very limited;
- Besides the switching frequency, there is only one single modulation parameter (i.e. the phase-shift angle ϕ) available for modulating the voltages applied to the terminals of the DAB's HF AC-link. This results in large HF AC-link RMS currents for most operating points when the DAB is operated with wide voltage ranges.

In the second section (i.e. Section 2.2) of this chapter, a comprehensive overview of the most relevant publications on improved (soft-switching) modulation schemes for DAB converters that have the goal to deal with the above listed disadvantages of the conventional PSM is presented. These publications are classified according their ZVS considerations. It is concluded that regardless their objective, all DAB modulation schemes so far presented are based on 'theoretical' current-based (CB) or energy-based (EB) ZVS analyses. The crucial disadvantage of the CB ZVS modulation schemes is that substantial parts of the calculated ZVS regions involve incomplete bridge commutations due to the presence of parasitic switch capacitances (i.e. the nonlinear output capacitances of the semiconductor power devices), which are not taken into account in the CB ZVS analysis. This inevitably leads to hard-switching operation, reduced conversion efficiency, and, in all probability, destruction of the semiconductor switching devices. The EB ZVS modulation schemes try to deal with this deficiency but, however, thereby:

- The state of the one active bridge is not taken into account in the ZVS verification of the other, or;
- The state of the one active bridge is taken into account in the ZVS verification of the other, but, however, a (quasi) simultaneous state change within the one and/or together with the other active bridge is not allowed, and;
- The EB ZVS analyses are based on constant, energy equivalent switch capacitances, resulting in significant errors.

Furthermore, EB ZVS modulation schemes encompass discontinuous steps in the modulation parameter trajectories, being highly undesirable. This problem relates to the way the HF AC-link of the traditional DAB converter is implemented (i.e. without commutation inductances, see further). Especially when the DAB is operated within wide input and/or output voltage ranges, such as is the case for the investigated single-stage DAB AC–DC converter where the input voltage of the DAB is a rectified (folded) sine-wave voltage, the above deficiencies are problematic and lead to significantly increased losses for most operating points. Furthermore, in this chapter, after a brief discussion of the different DAB variants, the full bridge - full bridge (FBFB) DAB implementation is selected as the most suitable candidate for the realization of the investigated 1-S DAB AC–DC converter.

It is concluded that on the one hand, the DAB has a great potential for realizing the single-phase, utility interfaced, bidirectional, and isolated on-board EV battery charger according to the specifications/requirements listed in Table 1.1 of Section 1.3 but, on the other hand, that there are still important parts in the existing DAB analyses that need further investigation.

3

Steady-State Operation of the DAB AC–DC Converter

In this chapter, the steady-state operation of the single-stage (1-S) DAB AC–DC converter is discussed. After outlining the general operating principle, the operating range of the full bridge - full bridge (FBFB) DAB DC–DC converter, which is the main building block of the 1-S AC–DC converter, is derived, as well as a control equation for the (averaged) DAB input current that is required in order to achieve a certain requested AC line current. Thereafter, the steady-state analysis of the FBFB DAB is presented, considering all possible degrees of freedom available to modulate the voltages applied to the terminals of the DAB's HF AC-link and including all possible switching modes while referring to the general considerations regarding the traditional phase-shift modulation (PSM, lowest possible degrees of freedom) presented in Chapter 2. Furthermore, 'commutation inductance(s)' are introduced as an essential HF AC-link modification in order to achieve full-operating-range zero voltage switching (ZVS) of the DAB, and the implication on the DAB model is discussed. Lastly, the ZVS behavior of the DAB is studied in detail, and a novel current-dependent charge-based (CDCB) ZVS verification method is proposed in order to tackle the deficiencies of the commonly used (theoretical) current-based (CB) and the energy-based (EB) ZVS analyses, assuring that the DAB is safely operated with quasi zero switching losses within the calculated ZVS regions.

3.1 Operating Range

Figure 3.1 shows the overall schematic of the investigated single-phase, single-stage (1-S), bidirectional, and isolated dual active bridge (DAB) AC–DC converter, consisting of a synchronous rectifier (SR) followed by a DAB DC–DC converter which is represented by a simplified 'block'. In Section 2.2.3, the full bridge - full bridge (FBFB) DAB implementation (see Figure 2.8(d)) is selected since it provides the highest possible flexibility regarding the modulation of the HF AC-link voltages and currents, implying a better capability to achieve soft-switching operation within the whole operating range compared to the other three DAB variants. Before the steady-state equations for the FBFB DAB are derived (see next section, i.e. Section 3.2), in this section the operating range (i.e. with regard to the operating conditions specified in Section 1.3) of the DAB is outlined first. The detailed schematic of the FBFB DAB is given in Figure 3.7 of Section 3.2, where the connection points X_1, X_2, Y_1, and Y_2 indicate how the DAB is connected in the overall schematic shown in Figure 3.1. The small HF filter capacitance at the input of the DAB, i.e. C_1 (see Figure 3.7), is the only capacitance that is present in the DC-link (i.e. between connection points X_1 and Y_1). This capacitance quasi completely absorbs the HF components of the instantaneous, HF switched, DAB input current i_1 and thus acts as an inherently integrated

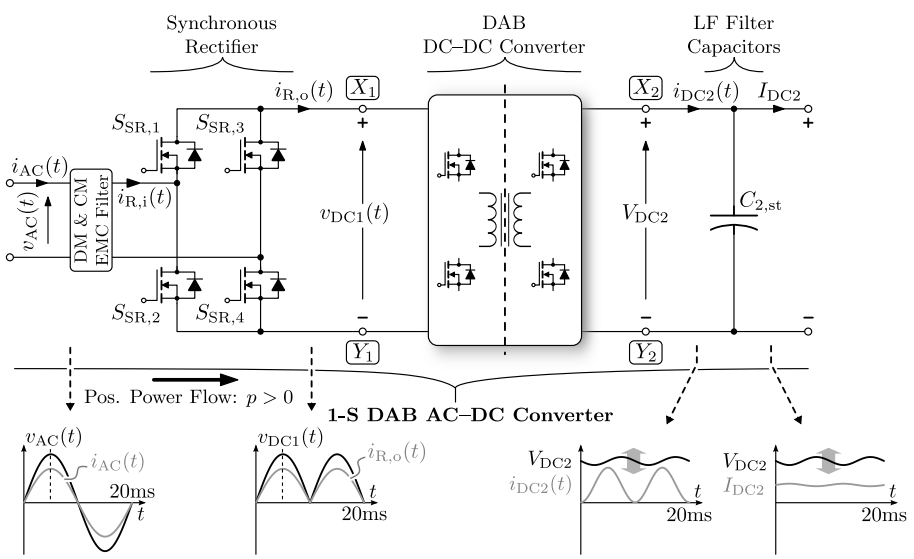


Figure 3.1: Overall schematic and principle waveforms of the single-phase, single-stage (1-S), bidirectional, and isolated DAB AC–DC converter investigated in this work.

input filter. Nevertheless, still an additional differential mode (DM) EMC filter is required in order to attenuate the HF components of i_1 that are not bypassed by C_1 and which thus propagate to the DAB's input port, i.e. the remaining HF harmonic distortion on the AC line current, and a common mode (CM) EMC filter to suppress the CM noise on the earth wire.

During operation the state st_{SR} of the SR changes two times each period of the AC line voltage $v_{\mathrm{AC}}(t)$, according to:

$$st_{\mathrm{SR}} = \begin{cases} 1 & \text{if } v_{\mathrm{AC}}(t) > 0: \quad S_{\mathrm{SR},1},\, S_{\mathrm{SR},4} \text{ on; } S_{\mathrm{SR},2},\, S_{\mathrm{SR},3} \text{ off,} \\ -1 & \text{if } v_{\mathrm{AC}}(t) < 0: \quad S_{\mathrm{SR},1},\, S_{\mathrm{SR},4} \text{ off; } S_{\mathrm{SR},2},\, S_{\mathrm{SR},3} \text{ on.} \end{cases} \tag{3.1}$$

Due to this continuous state change the AC line voltage $v_{\mathrm{AC}}(t)$ is folded into a DC voltage $v_{\mathrm{DC1}}(t)$ that is pulsating a twice the 50 Hz AC line frequency f_{L} and that varies according to the absolute value of $v_{\mathrm{AC}}(t)$:

$$v_{\mathrm{DC1}}(t) = |v_{\mathrm{AC}}(t)| = |\hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t)| = st_{\mathrm{SR}} \cdot \hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t), \tag{3.2}$$

where $\hat{V}_{\mathrm{AC}}$ is the amplitude of the AC line voltage and $\omega_{\mathrm{L}} = 2\pi f_{\mathrm{L}}$. This goes with the assumption that the voltage drop across the DM input filter inductors can be neglected in steady-state operation, being verified in Section 5.4. Voltage $v_{\mathrm{DC1}}(t)$ is directly fed to the input of the DAB DC–DC converter, which is thus operated with a constantly varying input voltage. Consequently, the input voltage range of the DAB is very wide:

$$\begin{gathered} 0 \text{ V} \leqslant v_{\mathrm{DC1}} \leqslant \hat{V}_{\mathrm{AC,max}} \quad \text{with} \quad \hat{V}_{\mathrm{AC,max}} = \sqrt{2} \cdot V_{\mathrm{AC,max}} = \sqrt{2} \cdot 253 \text{ V}, \\ \rightarrow \quad 0 \leqslant v_{\mathrm{DC1}} \leqslant 358 \text{ V}. \end{gathered} \tag{3.3}$$

It is explained in Section 3.2 that the DAB draws a HF switched current i_1 at its input, having a net DC value over one switching period T_{s}. The HF components of i_1 are bypassed by the small HF DC-link capacitance C_1 while the DC component i_{DAB1} of i_1, referred to as the averaged DAB input current, propagates to the DAB's input terminal and further to the SR. It is detailed in Section 3.2 how i_{DAB1} can be controlled by proper modulation of the DAB's active bridges.

For the exact calculation of $i_{\mathrm{DAB1}}(t)$ that is required in order to realize a given amplitude of the (active) AC line current $\hat{I}_{\mathrm{AC,P}}$, at a given power factor PF $= \cos(\varphi)$, the general schematic in Figure 3.1 is replaced by the schematic in Figure 3.2. There the DAB is represented by a variable current source i_{DAB1} connected in parallel with the SR and the DM EMC input filter. Note that a two-stage DM filter architecture with passive damping is considered (see Section 5.4). Conform Figure 3.7 (see Section 3.2), the capacitive part C_{DM1} of the first DM filter stage[1]

[1] In Figure 3.2 the components of the first DM filter stage are indexed 'DM1' while those of the second DM filter stage are indexed 'DM2'.

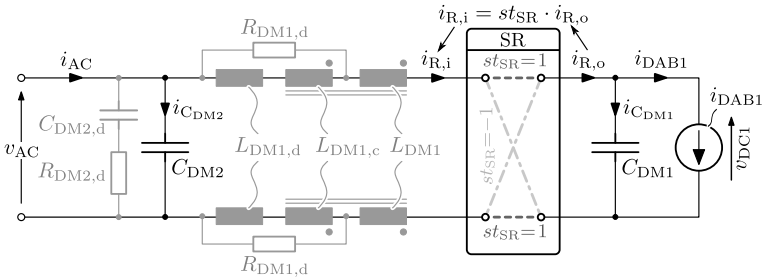


Figure 3.2: Equivalent circuit of the 1-S AC–DC converter's AC input side, with a controllable current source i_{DAB1} representing the averaged DAB input current, the SR, and the 2-stage DM EMC input filter.

is effectively realized by the HF DC-link capacitance C_1:

$$C_{\mathrm{DM1}} = C_1. \tag{3.4}$$

According to Figure 3.2, in steady-state operation the output current $i_{\mathrm{R,o}}(t)$ of the SR is calculated with:

$$i_{\mathrm{R,o}}(t) = i_{\mathrm{DAB1}}(t) + i_{\mathrm{C_{DM1}}}(t), \tag{3.5}$$

where

$$\begin{aligned} i_{\mathrm{C_{DM1}}}(t) &= C_{\mathrm{DM1}} \cdot \frac{\mathrm{d}v_{\mathrm{DC1}}(t)}{\mathrm{d}t} = C_{\mathrm{DM1}} \cdot \frac{\mathrm{d}(st_{\mathrm{SR}} \cdot \hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t))}{\mathrm{d}t} \\ &= st_{\mathrm{SR}} \cdot \omega_{\mathrm{L}} C_{\mathrm{DM1}} \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t). \end{aligned} \tag{3.6}$$

The continuous state change of the SR, i.e. according to (3.1), causes $i_{\mathrm{R,o}}(t)$ to be unfolded towards the SR's input:

$$i_{\mathrm{R,i}}(t) = st_{\mathrm{SR}} \cdot i_{\mathrm{R,o}}(t). \tag{3.7}$$

Knowing that $st_{\mathrm{SR}}^2 = 1$, and combining (3.7), (3.5), and (3.6), this yields:

$$\begin{aligned} i_{\mathrm{R,i}}(t) &= st_{\mathrm{SR}} \cdot i_{\mathrm{DAB1}}(t) + st_{\mathrm{SR}}^2 \cdot \omega_{\mathrm{L}} C_{\mathrm{DM1}} \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t) \\ &= st_{\mathrm{SR}} \cdot i_{\mathrm{DAB1}}(t) + \omega_{\mathrm{L}} C_{\mathrm{DM1}} \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t). \end{aligned} \tag{3.8}$$

The resulting AC line current $i_{\mathrm{AC}}(t)$ is then calculated with:

$$\begin{aligned} i_{\mathrm{AC}}(t) &= i_{\mathrm{R,i}}(t) + i_{\mathrm{C_{DM2}}}(t) = i_{\mathrm{R,i}}(t) + C_{\mathrm{DM2}} \cdot \frac{\mathrm{d}v_{\mathrm{AC}}(t)}{\mathrm{d}t} \\ &= st_{\mathrm{SR}} \cdot i_{\mathrm{DAB1}}(t) + \omega_{\mathrm{L}} C_{\mathrm{DM1}} \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t) + \omega_{\mathrm{L}} C_{\mathrm{DM2}} \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t) \\ &= st_{\mathrm{SR}} \cdot i_{\mathrm{DAB1}}(t) + \underbrace{\omega_{\mathrm{L}}(C_{\mathrm{DM1}} + C_{\mathrm{DM2}}) \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t)}_{\text{Capacitive DM EMC filter current}}. \end{aligned} \tag{3.9}$$

The second term in equation (3.9) is the capacitive differential mode (DM) EMC filter current, indicating a certain reactive power consumption by the DM EMC input filter capacitors C_{DM1} and C_{DM2}. As will be shown below, this capacitive power needs to be (partly) compensated in order to meet the PFC requirement given in Table 1.1 of Section 1.3. This can be achieved by controlling $i_{\mathrm{DAB1}}(t)$ slightly lagging to $v_{\mathrm{DC1}}(t)$, requiring a certain reactive (i.e. inductive) power transfer capability of the DAB.

When defining the power flow direction '*dir*' positive in the direction indicated by the arrow in Figure 3.1, i.e.:

$$dir = \begin{cases} 1 & \text{if } p(t) > 0 : \text{AC-side} \rightarrow \text{DC-side}, \\ -1 & \text{if } p(t) < 0 : \text{DC-side} \rightarrow \text{AC-side}, \end{cases} \tag{3.10}$$

then for a given amplitude of the (active) AC input current $\hat{I}_{\mathrm{AC,P}}$, a given power factor PF($=\cos(\varphi)$), and a given power flow direction *dir*, the instantaneous AC line current $i_{\mathrm{AC}}(t)$ is given by:

$$i_{\mathrm{AC}}(t) = dir \cdot \frac{\hat{I}_{\mathrm{AC,P}}}{\mathrm{PF}} \sin(\omega_{\mathrm{L}} t + dir \cdot \arccos(\mathrm{PF})). \tag{3.11}$$

Consequently, the averaged DAB input current $i_{\mathrm{DAB1}}(t)$ that is required in order to achieve this AC line current is obtained by substituting $i_{\mathrm{AC}}(t)$ in equation (3.9) by expression (3.11) and solving for $i_{\mathrm{DAB1}}(t)$, yielding:

$$\begin{aligned} i_{\mathrm{DAB1}}(t) = & st_{\mathrm{SR}} \cdot \Big[dir \cdot (\hat{I}_{\mathrm{AC,P}}/\mathrm{PF}) \sin(\omega_{\mathrm{L}} t + dir \cdot \arccos(\mathrm{PF})) - \\ & \omega_{\mathrm{L}}(C_{\mathrm{DM1}} + C_{\mathrm{DM2}}) \cdot \hat{V}_{\mathrm{AC}} \cos(\omega_{\mathrm{L}} t) \Big]. \end{aligned} \tag{3.12}$$

Note that $1/st_{\mathrm{SR}} = st_{\mathrm{SR}}$. In order to limit the required reactive power flow capability of the DAB converter[2], the total DM EMC filter capacitance value has

[2]Note that, when operated under soft-switching (i.e. by means of zero voltage switching, ZVS, see Section 3.3), the reactive power flow capability of DAB converters is limited.

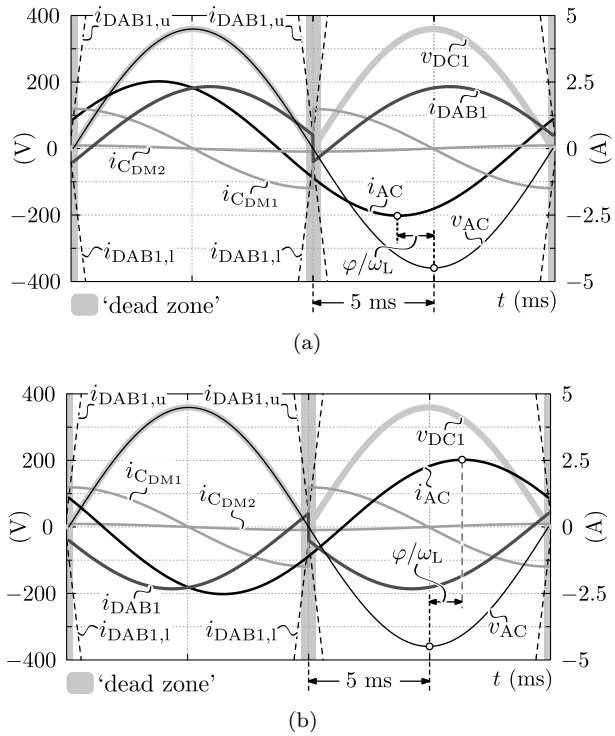


Figure 3.3: Ideal input-side quantities for the worst case PF condition: $\hat{I}_{\mathrm{AC,P}} = \sqrt{2} \cdot 0.1 \cdot I_{\mathrm{AC,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 358$ V; PF $= 0.9$. (a) Positive power flow; $dir = 1$, (b) negative power flow; $dir = -1$.

been restricted to:

$$(C_{\mathrm{DM1}} + C_{\mathrm{DM2}})_{\mathrm{max}} \leqslant 14.2\ \mu\mathrm{F}. \tag{3.13}$$

This value is a good compromise between the reactive power flow requirement of the DAB on the one hand and the size of the DM filter inductors on the other. It is the result of several DM EMC filter design iterations which were performed in the course of the development of the 1-S DAB AC–DC converter prototype system (see Section 5.4), yielding C_{DM1}=13.2 μF and C_{DM2}=1 μF.

Figure 3.3 depicts the averaged DAB input current $i_{\mathrm{DAB1}}(t)$ together with the most relevant (idealized) input side converter quantities for the worst case PF condition, i.e. $\hat{I}_{\mathrm{AC,P}} = \sqrt{2} \cdot 0.1 \cdot I_{\mathrm{AC,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 358$ V; PF $= 0.9$ (see Table 1.1). These quantities are calculated for C_{DM1}=13.2 μF and C_{DM2}=1 μF, using the aforementioned equations. In Figure 3.3(a) the power flow is positive

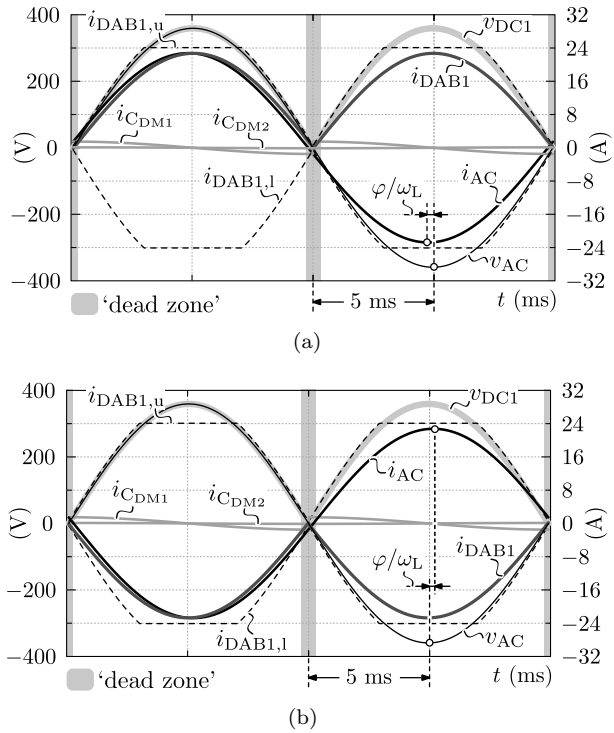


Figure 3.4: Ideal input-side quantities for nominal (active) input current $\hat{I}_{\mathrm{AC,P}} = \sqrt{2} \cdot I_{\mathrm{AC,P,nom}} = 22.6$ A; $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 358$ V; PF $= 0.999$. (a) Positive power flow; $dir = 1$, (b) negative power flow; $dir = -1$.

($dir = 1$) while in Figure 3.3(b) the power flow is negative ($dir = -1$). The same quantities are shown in Figure 3.4 regarding the nominal (active) input current $\hat{I}_{\mathrm{AC,P}} = \sqrt{2} \cdot I_{\mathrm{AC,P,nom}} = 22.6$ A, an AC line voltage $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,max}} = 358$ V, and a power factor of PF $= 0.999$. Figure 3.4(a) is obtained for positive power flow ($dir = 1$) while Figure 3.4(b)is obtained for negative power flow ($dir = -1$).

The range of the averaged DAB input current i_{DAB1} now has be defined in a way that all possible input conditions that can occur, i.e. with regard to the AC line voltage $v_{\mathrm{AC}}(t)$, the AC-line current $i_{\mathrm{AC}}(t)$, and the PF, are compassed. Thereby enough margin for component variances and dynamic controllability should be taken into account. Consequently, given the operating conditions specified in Table 1.1, an upper limit $i_{\mathrm{DAB1,u}}$ and a lower limit $i_{\mathrm{DAB1,l}}$ for i_{DAB1} are defined. Assuming PF $= 1$, $dir = 1$, and $C_{\mathrm{DM1}} = C_{\mathrm{DM2}} = 0$, the expression for $i_{\mathrm{DAB1}}(t)$ according to (3.12) becomes:

$$i_{\mathrm{DAB1}} = st_{\mathrm{SR}} \cdot \hat{I}_{\mathrm{AC,P}} \sin(\omega_{\mathrm{L}} t). \tag{3.14}$$

This means that for a certain DAB input voltage v_{DC1}, and an AC input current $\hat{I}_{\mathrm{AC,P}}$, the averaged DAB input current is highest ($i_{\mathrm{DAB1}} = i_{\mathrm{DAB1,max}}$) for $\hat{V}_{\mathrm{AC}} = \hat{V}_{\mathrm{AC,min}}$ and can be calculated as:

$$\frac{i_{\mathrm{DAB1}}}{v_{\mathrm{DC1}}} = \frac{st_{\mathrm{SR}} \cdot \hat{I}_{\mathrm{AC,P}} \sin(\omega_{\mathrm{L}} t) \;\; [\text{eq. (3.14)}]}{st_{\mathrm{SR}} \cdot \hat{V}_{\mathrm{AC}} \sin(\omega_{\mathrm{L}} t) \;\; [\text{eq. (3.2)}]} = \frac{\hat{I}_{\mathrm{AC,P}}}{\hat{V}_{\mathrm{AC}}} \tag{3.15}$$

$$\rightarrow \; i_{\mathrm{DAB1}} = \frac{v_{\mathrm{DC1}} \cdot \hat{I}_{\mathrm{AC,P}}}{\hat{V}_{\mathrm{AC}}} \tag{3.16}$$

$$\rightarrow \; i_{\mathrm{DAB1,max}} = \frac{v_{\mathrm{DC1}} \cdot \hat{I}_{\mathrm{AC,P}}}{\hat{V}_{\mathrm{AC,min}}}. \tag{3.17}$$

Using $\hat{I}_{\mathrm{AC,P}} = 24$ A ($= \sqrt{2} \cdot I_{\mathrm{AC,P,nom}} + \text{margin}$) in (3.17), adding an additional margin of 0.5 A, and clamping the result to 24 A, the upper limit $i_{\mathrm{DAB1,u}}$ is determined as:

$$\begin{aligned} i_{\mathrm{DAB1,u}}(v_{\mathrm{DC1}}) &= \min\left(\frac{v_{\mathrm{DC1}} \cdot 24}{\hat{V}_{\mathrm{AC,min}}} + 0.5, 24\right) \\ &= \min\left(0.082 \cdot v_{\mathrm{DC1}} + 0.5, 24\right), \end{aligned} \tag{3.18}$$

where $\hat{V}_{\mathrm{AC,min}} = \sqrt{2} \cdot (230 - 23) = 292.74$ V. By taking the lower limit $i_{\mathrm{DAB1,l}}(v_{\mathrm{DC1}}) = -i_{\mathrm{DAB1,u}}(v_{\mathrm{DC1}})$, the input-voltage-dependent range of the averaged DAB input current is completely defined with:

$$i_{\mathrm{DAB1,l}}(v_{\mathrm{DC1}}) \leqslant i_{\mathrm{DAB1}}(v_{\mathrm{DC1}}) \leqslant i_{\mathrm{DAB1,u}}(v_{\mathrm{DC1}}). \tag{3.19}$$

By combining (3.19) with (3.18) and (3.3), the two-quadrant (2-Q) voltage-current plane shown in Figure 3.5 is obtained, representing the complete DAB's input voltage and input current range. Note that around the zero crossing (-30 V$\leqslant v_{\mathrm{AC}} \leqslant 30$ V) the bridges of the DAB are inactive ('dead zone') as power conversion under ZVS conditions is quasi impossible within this voltage interval.

In Figure 3.5, the lines in the voltage-current plane show the relation $i_{\mathrm{DAB1}}(v_{\mathrm{DC1}})$ for different operating conditions, i.e. they represent the trajectories that are followed by i_{DAB1} during one period of the AC line voltage. In Figure 3.5(a), the lines '10% pos.', '10% neg.', '100% pos.', and '100% neg.' correspond with

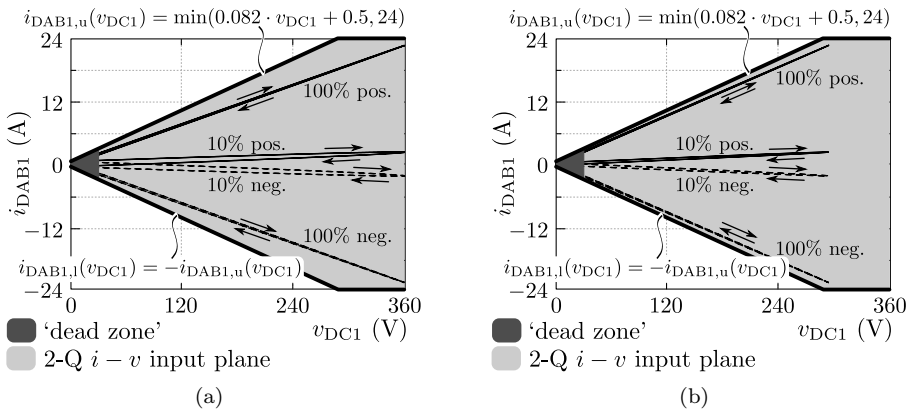


Figure 3.5: Two-quadrant (2-Q) voltage-current plane of the DAB, representing the complete DAB's input voltage and input current operating range.

the operating conditions used to respectively obtain Figures 3.3(a), 3.3(b), 3.4(a), and Figure 3.4(b), where $\hat{V}_{AC} = \hat{V}_{AC,max} = 358$ V. In Figure 3.5(b), the lines '10% pos.', '10% neg.', '100% pos.', and '100% neg.' correspond with the same operating conditions as the ones in Figure 3.5(a) with the difference that now $\hat{V}_{AC} = \hat{V}_{AC,min} = 292$ V. Due to the rectification performed by the SR, each trajectory is traversed two times during one period of the AC line voltage. It is clear that the DAB's input range is defined in a way that all possible input conditions that can occur, i.e. with regard to the AC line voltage $v_{AC}(t)$, the AC line current $i_{AC}(t)$, and the PF, are compassed since the trajectories of i_{DAB1} lie within the voltage-current plane boundaries. Furthermore, the 2-Q voltage-current plane is independent of the DAB's output voltage V_{DC2} whose range is specified in Table 1.1 as:

$$370 \text{ V} \leqslant V_{DC2} \leqslant 470 \text{ V}. \tag{3.20}$$

As a result, the complete DAB's operating range (see Figure 3.6), according to the operating conditions specified in Section 1.3 (see Table 1.1), is completely defined. As explained in Section 4.2.1 of Chapter 4, the worst case operating point regarding ZVS operation of the DAB is the one indicated by a '★'. Note that the DAB handles the double line frequency power component, which in the dual-stage AC–DC topologies is typically buffered by large (electrolytic) DC-link capacitors. Due to the absence of these DC-link capacitors in the investigated single-stage converter, electrolytic capacitors (capacitance value $C_{2,st}$) are placed at the DC output side in order to (partly) filter this 100 Hz power component. The selected value for $C_{2,st}$ is further detailed in Section 5.3 of Chapter 5.

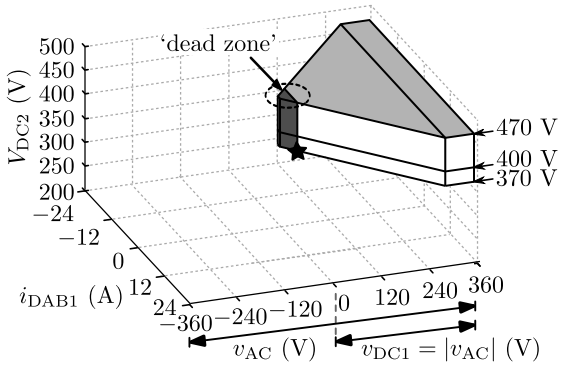


Figure 3.6: Complete operating range of the FBFB DAB DC–DC converter, which is the main building block of the investigated 1-S DAB AC–DC architecture, according to the operating conditions specified in Table 1.1 of Section 1.3.

3.2 Steady-State Operation of the DAB DC–DC Converter

In the previous section (i.e. Section 3.1) the operating range of the FBFB DAB DC–DC converter used in the investigated 1-S DAB AC–DC topology is detailed and a control equation (see equation (3.12)) for the averaged DAB input current $i_{\mathrm{DAB1}}(t)$, required in order to achieve a certain AC line current with given amplitude ($\hat{I}_{\mathrm{AC,P}}$, active component of the current), given power factor PF($=\cos(\varphi)$), and given power flow direction *dir*, is proposed. In this section the steady-state analysis of the FBFB DAB is presented, i.e. the fundamental mode equations are derived based on the lossless DAB model while referring to the general considerations regarding the traditional phase-shift modulation (PSM) given in Section 2.1. In order to tackle the disadvantages of the PSM, being a limited ZVS operating range and large RMS currents in the HF AC-link for most operating points when the DAB is operated with wide voltage ranges, here all possible degrees of freedom available for controlling the DAB's active bridges are exploited by considering dual-sided duty-cycle modulation (DSPWM) instead of PSM. This provides the highest degree of freedom regarding the search toward optimal, full-operating-range ZVS modulation schemes in Chapter 4. Furthermore, after reevaluation of the theoretical current-based (CB) ZVS conditions, commutation inductance(s) are introduced which, using a simple calculated example, are shown to be an essential HF AC-link modification in order to achieve full-operating-range ZVS operation of the DAB. The effect of commutation inductance(s) in the HF AC-link on the ZVS operating range is further investigated in Chapter 4.

Figure 3.7 shows the detailed schematic of the FBFB DAB, where connection points X_1, X_2, Y_1, and Y_2 indicate how the DAB is connected in the overall schematic of the 1-S AC–DC architecture depicted in Figure 3.1. Note that for the considered 1-S AC–DC converter the DC input port voltage of the DAB is highly variable (i.e. a folded (rectified) sine-wave voltage is applied between connection points X_1 and Y_1; see Section 3.1). The DC output port voltage, applied between connection points X_2 and Y_2, on the other hand is quasi constant (apart from some 100 Hz voltage ripple). Therefore, in the following, notations v_{DC1} and V_{DC2} are used for the respective DAB port voltages (see Figure 3.7). Furthermore, the voltage variations at both ports of the DAB induce a current in the HF filter capacitors[3], i.e. currents i_{C_1} and i_{C_2}. When disregarding the HF components of the instantaneous DAB input and output currents i_1 and i_2 that are not bypassed by the corresponding HF filter capacitance and which thus propagate to the DAB's input and output ports, the averaged (i.e. evaluated over one switching cycle T_{s}) DAB input and output port currents $i_{\mathrm{R,o}}$ and i_{DC2} (see also Figure 3.1) are composed of the averaged DAB

[3]The FBFB DAB contains a HF filter capacitance at its input and at its output port (i.e. C_1 resp. C_2, see Figure 3.7).

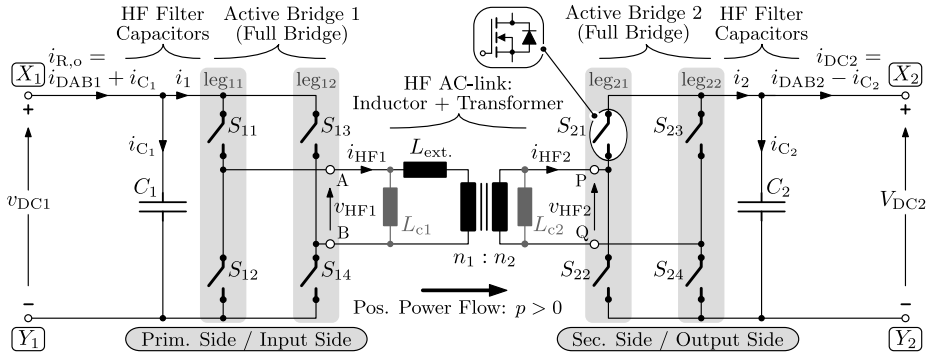


Figure 3.7: General schematic of the full bridge - full bridge (FBFB) DAB DC–DC converter used in the investigated 1-S DAB AC–DC architecture. The circuit variables L_{c1} and L_{c2} are named 'commutation inductances' and are introduced further in this section/work as an essential HF AC-link modification in order to achieve full-operating-range ZVS operation of the DAB converter.

input and output currents[4] i_{DAB1} and i_{DAB2} (see further) and the voltage-induced currents, i_{C_1} and i_{C_2}, in the HF filter capacitors:

$$i_{R,o} = i_{DAB1} + i_{C_1}, \tag{3.21}$$

$$i_{DC2} = i_{DAB2} - i_{C_2}. \tag{3.22}$$

The exact input/output port voltages/currents and the currents induced in the HF filter capacitors are derived in Section 3.1 regarding the operating conditions specified in Section 1.3.

Calculation Examples: Used Circuit Level Variables

In the following, all calculation examples and waveforms regarding the steady-state operation of the FBFB DAB converter are obtained using the circuit level variables of the final prototype converter design:

- $L = 13\ \mu$H;
- $L_{c1} = 62.1\ \mu$H;

[4]Remind that the averaged DAB input and output currents i_{DAB1} and i_{DAB2} are obtained by averaging $i_1(t)$ respectively $i_2(t)$ over one switching period T_s. The notations 'i_{DAB1}, i_{DAB2}' are preferred over the notations 'I_{DAB1}, I_{DAB2}' since, in the 1-S AC–DC architecture, their value is highly variable in time (see Section 3.1).

- $L_{c2} = 62.1\ \mu$H;
- $\frac{n_1}{n_2} = 1$.

The circuit variables L_{c1} and L_{c2} are named 'commutation inductances' and are introduced in this work as an essential HF AC-link modification in order to achieve full-operating-range ZVS operation of the DAB converter. Below, L_{c1} and L_{c2} are in the first place disregarded in the analysis, i.e. $L_{c1} = L_{c2} = \infty$, and will be introduced later in this section. Nevertheless, in order to avoid repetition they are already shown in Figure 3.7. Furthermore, for the given examples a switching frequency of $f_s = 120$ kHz is applied. The derivation of the above circuit variables is detailed in Chapter 4. For the reasons given in Section 2.2.4, in this work the HF AC-link of the designed DAB converter is implemented using an external inductance L_{ext} which is placed in series with the HF transformer (see Figure 3.7). Consequently, the equivalent inductance value L is calculated with (2.49).

3.2.1 Lossless DAB Model

For the FBFB DAB that is controlled with PSM (see Section 2.1.2), voltages $v_{HF1}(t)$ and $v_{HF2}(t)$ generated by the full bridge circuits are modulated with 50 % duty-cycle and thus alter between two voltage levels (i.e. plus and minus the corresponding DC bus voltage level; acc. to (2.5) and (2.6)). However, with PSM the bridge states where either the two top switches or the two bottom switches of an active bridge are simultaneously in the conduction state are not considered. As a result, the conditions where the voltage generated by an active bridge equals zero is overlooked, greatly limiting the degrees of freedom to modulate the AC-link voltages $v_{HF1}(t)$ and $v_{HF2}(t)$. Therefore the 'zero-voltage' states are included in the analysis given below, enabling pulse-width modulation of $v_{HF1}(t)$ and $v_{HF2}(t)$, which can now alter between three instead of two voltage levels within a switching period T_s:

$$v_{HF1}(t) = \begin{cases} +v_{DC1} & \text{for } st_{leg_{11}}{=}1,\ st_{leg_{12}}{=}0, \\ 0 & \text{for } st_{leg_{11}}{=}1,\ st_{leg_{12}}{=}1 \text{ or } st_{leg_{11}}{=}0,\ st_{leg_{12}}{=}0, \\ -v_{DC1} & \text{for } st_{leg_{11}}{=}0,\ st_{leg_{12}}{=}1, \end{cases} \tag{3.23}$$

$$v_{HF2}(t) = \begin{cases} +V_{DC2} & \text{for } st_{leg_{21}}{=}1,\ st_{leg_{22}}{=}0, \\ 0 & \text{for } st_{leg_{21}}{=}1,\ st_{leg_{22}}{=}1 \text{ or } st_{leg_{21}}{=}0,\ st_{leg_{22}}{=}0, \\ -V_{DC2} & \text{for } st_{leg_{21}}{=}0,\ st_{leg_{22}}{=}1, \end{cases} \tag{3.24}$$

where $st_{leg_{11}}$, $st_{leg_{12}}$, $st_{leg_{21}}$, and $st_{leg_{22}}$ are respectively described by (2.3), (2.4), (2.7), and (2.8). The expressions given in Section 2.1.2 for the determination of

$v_{\mathrm{HF1}}(t)$, $v_{\mathrm{HF2}}(t)$, and $v'_{\mathrm{HF2}}(t)$ still hold, now using v_{DC1} instead of V_{DC1}:

$$v_{\mathrm{HF1}}(t) = v_{\mathrm{DC1}} \cdot (st_{\mathrm{leg}_{11}} - st_{\mathrm{leg}_{12}}), \tag{3.25}$$

$$v_{\mathrm{HF2}}(t) = V_{\mathrm{DC2}} \cdot (st_{\mathrm{leg}_{21}} - st_{\mathrm{leg}_{22}}), \tag{3.26}$$

$$v'_{\mathrm{HF2}}(t) = \frac{n_1}{n_2} \cdot v_{\mathrm{HF2}}(t). \tag{3.27}$$

The resulting lossless DAB model for the FBFB DAB converter is depicted in Figure 3.8 while Figure 3.9 shows two examples of the three-level, pulse-width modulated patterns of voltages[5] $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$. It can be seen from Figure 3.9 that within one switching period T_{s} there are now eight time intervals (numbered with index counter i; $m = 8$) with constant voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, and thus with constant inductor voltage[6] $v_{\mathrm{L}}(t)$:

$$\begin{aligned}
&\text{time interval I } (i = 1): && t_0 < t \leqslant t_1,\\
&\text{time interval II } (i = 2): && t_1 < t \leqslant t_2,\\
& && \vdots\\
&\text{final time interval } (i = m): && t_{\mathrm{m}-1} < t \leqslant t_{\mathrm{m}} = t_0 + T_{\mathrm{s}}.
\end{aligned} \tag{3.28}$$

This implies that eight switching instances[7] (e.g. $t_0 \ldots t_7$) take place within one switching cycle T_{s}. As, besides the phase-shift angle ϕ between both HF AC-link voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, also the duty-cycles τ_1 and τ_2 of $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$ can be adjusted, this modulation technique is referred to as dual-sided duty-cycle modulation (DSPWM). Consequently, the number of modulation parameters has increased from one for the PSM described in Section 2.1.2 to three for the DSPWM described in this section:

- the phase-shift angle ϕ (rad.) between $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$;
- the pulse-width modulation angle τ_1 (rad.) of $v_{\mathrm{HF1}}(t)$;
- the pulse-width modulation angle τ_2 (rad.) of $v_{\mathrm{HF2}}(t)$.

[5] It should be reminded that, in any case, the average values of $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$ (and thus of $v'_{\mathrm{HF2}}(t)$), evaluated over one switching period during steady-state converter operation (i.e. the DC components of $v_{\mathrm{HF1}}(t)$, $v_{\mathrm{HF2}}(t)$, and $v'_{\mathrm{HF2}}(t)$), should be zero in order to avoid saturation of the HF transformer.

[6] Remind that $v_{\mathrm{L}}(t)$ is calculated with (2.15).

[7] Note that the boundaries $t_{\mathrm{i}-1}$ and t_{i} of a time interval i correspond with a change of voltage $v_{\mathrm{HF1}}(t)$ or voltage $v_{\mathrm{HF2}}(t)$ which is equal to the associated DC bus voltage and which, according to (3.23) and (3.24), is initiated by a state change of one of the two legs of the particular active bridge. Remind that for PSM the voltage change is equal to two times the associated DC bus voltage since the voltage change is initiated by a simultaneous state change of both legs of the particular active bridge.

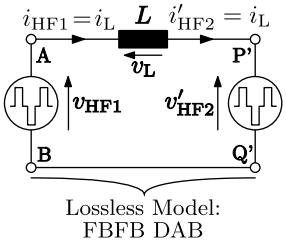


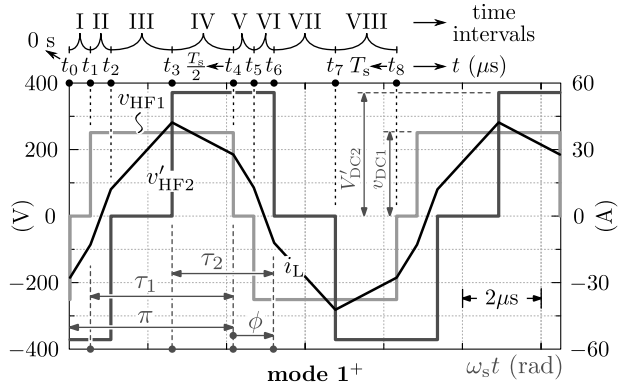
Figure 3.8: Lossless model of the full bridge - full bridge (FBFB) DAB DC–DC converter regarding dual-sided duty-cycle modulation (DSPWM).

ϕ, τ_1, τ_2 are depicted in Figure 3.9 and are defined as angles ($\Delta t \cdot \omega_s$) in the unit radians (angular axes; i.e. normalized with respect to the switching period T_s), with $\omega_s = 2\pi f_s$ and f_s the switching frequency ($f_s = 1/T_s$). ϕ is the angle between the positive falling edge of $v_{HF1}(t)$ and the positive falling edge of $v'_{HF2}(t)$. A last parameter that can be freely controlled (within a reasonable range) is the switching frequency f_s, resulting in a total of four modulation parameters:

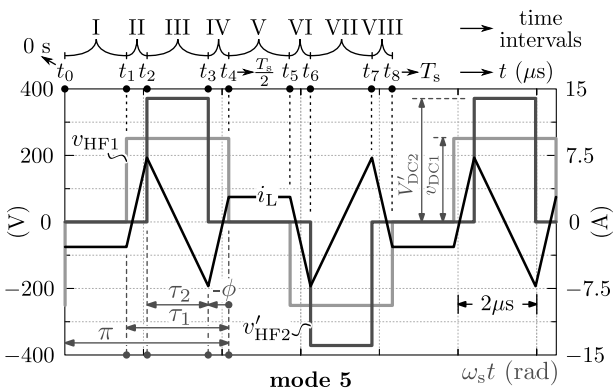
$$\rightarrow \ \mathbf{x} = (\phi, \tau_1, \tau_2, f_s). \tag{3.29}$$

The DSPWM provides the highest possible flexibility for controlling the DAB's active bridges and thus the highest degree of freedom regarding the search toward optimal ZVS modulation schemes. However, the complexity of the analysis greatly increases since now not two (i.e. for PSM) but twelve unique sequences of the eight time intervals i, within a switching cycle T_s, with constant AC-link voltages, can be identified, resulting in twelve possible switching modes. Figure A.1 of Appendix A depicts examples for all of these twelve modes. The modulation parameter relations describing the boundary conditions of the respective switching modes are given in Table A.1 of Appendix A.

As indicated by Table A.1 and conform Figure A.1, the total of twelve switching modes contains four unique modes for each power flow direction and four modes that are usable for both power flow directions (the power flow direction *dir* is defined by (2.13) in accordance with Figure 3.7). It is shown in Chapter 4 that for each power flow direction only two out of the twelve possible modes are feasible for efficient ZVS operation. For positive power flow ($dir = 1$) these are mode 1^+ (high power mode; see Figure 3.9(a) and Figure A.1(a)) and mode 5 (low power mode; see Figure 3.9(b) and Figure A.1(i)). For negative power flow ($dir = -1$) these are, very similarly, mode 1^- (high power mode; see Figure A.1(b)) and once more mode 5 (low power mode). Mode 1^+ (high power mode for positive power flow) and mode 1^- (high power mode for negative power flow) show highly similar HF AC-link voltage patterns and are generally referred to as mode 1. In fact, the modulation parameters for mode 1^- can be directly calculated from those of



(a) Example: $\phi = \pi/4$ rad., $\tau_1 = 7\pi/8$ rad., $\tau_2 = 5\pi/8$ rad.



(b) Example: $\phi = -\pi/8$ rad., $\tau_1 = 5\pi/8$ rad., $\tau_2 = 3\pi/8$ rad.

Figure 3.9: Examples of the primary side referred AC-link terminal voltages and inductor currents for dual-sided duty-cycle modulation (DSPWM) of the FBFB DAB. (a) Mode 1^+: high power mode, usable for positive power flow ($dir = 1$). (b) Mode 5: low power mode, usable for positive and negative power flow ($dir = 1$ and $dir = -1$). The waveforms are derived using $v_{DC1} = 250$ V, $V_{DC2} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{c1} = L_{c2} = \infty$, and $f_s = 120$ kHz.

mode 1^+ as is shown further in this section. Mode 1 (high power mode) and mode 5 (low power mode) form the basis of the final DAB modulation schemes presented in Chapter 4. For the reason of clarity, below the derivation of the steady-state mode equations is detailed for mode 1^+ and mode 5 only[8], which correspond with the voltage patterns depicted in respectively Figure 3.9(a) and Figure 3.9(b) and which are obtained under the conditions:

[8]The equations for mode 1^- (negative power flow; $dir = -1$) are similar to those of mode 1^+ (positive power flow; $dir = 1$).

$$\text{mode } 1^+: \qquad -\tau_1 + \pi \leqslant \phi \leqslant \tau_2, \tag{3.30}$$

$$\text{mode } 5: \qquad \tau_2 - \tau_1 \leqslant \phi \leqslant 0, \tag{3.31}$$

i.e. the mode boundary conditions, see also Table A.1 of Appendix A. Nevertheless, in the scope of the search toward optimal modulation schemes in Chapter 4, the steady-state expressions for all twelve modes were derived and evaluated in Section 4.1. For the sake of brevity they are given in Appendix A and referred to in the following explanations.

3.2.2 Dual-Sided Duty-Cycle Modulation (DSPWM): Mode Equations

Under the assumption that the modulation parameters $\mathbf{x}$ (see (3.29)) and the supply voltages v_{DC1} and V_{DC2} remain constant during a switching cycle T_s, the expressions for the inductor current at the different switching instances, $i_\mathrm{L}(t_\mathrm{i})$, are obtained by establishing equation (2.17) in the first half cycle of the switching period T_s (voltage intervals I…IV, within $0 < t \leqslant T_\mathrm{s}/2$) while applying (2.18). Choosing the negative rising edge of $v_{\mathrm{HF1}}(t)$ as the time reference t_0 (= 0 s; see Figure 3.9), the expressions for the switching instances $t_0 \ldots t_4$ required to establish the systems of equations for mode 1^+ and mode 5 are as listed in the left inset of Table 3.1[9], resulting in:

mode 1^+:

$$\begin{aligned}
i_\mathrm{L}(t_1) &= i_\mathrm{L}(t_0) + \frac{(\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(\pi - \tau_1)}{\omega_\mathrm{s}} && : \text{interval I},\\
i_\mathrm{L}(t_2) &= i_\mathrm{L}(t_1) + \frac{(v_{\mathrm{DC1}} + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(-\pi + \phi + \tau_1)}{\omega_\mathrm{s}} && : \text{interval II},\\
i_\mathrm{L}(t_3) &= i_\mathrm{L}(t_2) + \frac{v_{\mathrm{DC1}}}{L} \cdot \frac{(\pi - \tau_2)}{\omega_\mathrm{s}} && : \text{interval III},\\
i_\mathrm{L}(t_4) &= i_\mathrm{L}(t_3) + \frac{(v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(-\phi + \tau_2)}{\omega_\mathrm{s}} && : \text{interval IV},\\
i_\mathrm{L}(t_4) &= -i_\mathrm{L}(t_0).
\end{aligned} \tag{3.32}$$

[9] $t_0 \ldots t_4$ for all possible switching modes are listed in Table A.2 of Appendix A. Note also that for all modes, $t_5 \ldots t_8$ can be directly calculated from $t_1 \ldots t_4$ according to the right inset of Table 3.1.

	mode 1^+	mode 5
t_0	0	0
t_1	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_2	$\frac{\phi}{\omega_s}$	$\frac{\pi + \phi - \tau_2}{\omega_s}$
t_3	$\frac{\pi + \phi - \tau_2}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$
$\vdots$	$\vdots$	$\vdots$

	all modes	
$\vdots$	$\vdots$	$\vdots$
t_5	$t_1 + \frac{T_s}{2}$	$t_1 + \frac{T_s}{2}$
t_6	$t_2 + \frac{T_s}{2}$	$t_2 + \frac{T_s}{2}$
t_7	$t_3 + \frac{T_s}{2}$	$t_3 + \frac{T_s}{2}$
t_8	$t_4 + \frac{T_s}{2} = T_s$	$t_4 + \frac{T_s}{2} = T_s$

Table 3.1: Left table inset: switching instances $t_0 \dots t_4$ for mode 1^+ and mode 5, choosing the negative rising edge of $v_{HF1}(t)$ as the time reference t_0 (= 0 s). Right table inset: for all modes $t_5 \dots t_8$ can be directly calculated from $t_1 \dots t_4$.

mode 5:

$$
\begin{aligned}
&i_L(t_1) = i_L(t_0) && \text{: interval I,}\\
&i_L(t_2) = i_L(t_1) + \frac{v_{DC1}}{L} \cdot \frac{(\phi + \tau_1 - \tau_2)}{\omega_s} && \text{: interval II,}\\
&i_L(t_3) = i_L(t_2) + \frac{(v_{DC1} - \frac{n_1}{n_2} \cdot V_{DC2})}{L} \cdot \frac{\tau_2}{\omega_s} && \text{: interval III,}\\
&i_L(t_4) = i_L(t_3) + \frac{v_{DC1}}{L} \cdot \frac{-\phi}{\omega_s} && \text{: interval IV,}\\
&i_L(t_4) = -i_L(t_0). &&
\end{aligned}
\tag{3.33}
$$

Solving these systems of equations[10] gives the expressions in Table 3.2 for the inductor current $i_L(t)$ at the switching instances $t_0 \dots t_4$ within $0 < t \leqslant T_s/2$ for both mode 1^+ and mode 5. d is the primary side referred voltage conversion ratio according to (2.21). The solutions for $i_L(t_i)$ regarding all possible switching modes are given in Table A.3 of Appendix A. Conform Figures 3.7 and 3.8, and disregarding commutation inductances L_{c1} and L_{c2} (i.e. $L_{c1} = L_{c2} = \infty$), the respective HF AC-link currents (bridge currents) $i_{HF1}(t)$ and $i_{HF2}(t)$ are calculated with (2.22) and (2.23). $i_{HF1}(t)$ and $i_{HF2}(t)$ for the example in Figure 3.9(a) (i.e. for mode 1^+) are respectively shown in Figure 3.10(a), depicting the primary side bridge quantities, and in Figure 3.10(b), depicting the secondary side bridge quantities. $i_{HF1}(t)$ and $i_{HF2}(t)$ for the example in Figure 3.9(b) (i.e. for mode 5) are shown in Figure A.2 of Appendix A. The states of the different bridge legs

[10]The systems of equations for the calculation of $i_L(t_i)$ regarding all possible switching modes are listed in Appendix A, equation systems (A.1)-(A.12).

	$i_{\mathrm{L}}(t_{\mathrm{i}})$ for mode 1^{+}	$i_{\mathrm{L}}(t_{\mathrm{i}})$ for mode 5
$i_{\mathrm{L}}(t_0)$	$\frac{-v_{\mathrm{DC1}} \cdot \left(d \cdot (\frac{-\tau_2}{2} + \phi) + \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$	$\frac{-v_{\mathrm{DC1}} \left(-d\frac{\tau_2}{2} + \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_1)$	$\frac{v_{\mathrm{DC1}} \cdot \left(d \cdot (-\tau_1 + \frac{\tau_2}{2} - \phi + \pi) - \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$	$\frac{v_{\mathrm{DC1}} \cdot \left(d\frac{\tau_2}{2} - \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_2)$	$\frac{-v_{\mathrm{DC1}} \cdot \left(-d\frac{\tau_2}{2} - \frac{\tau_1}{2} - \phi + \pi\right)}{\omega_{\mathrm{s}} L}$	$\frac{v_{\mathrm{DC1}} \cdot \left(d\frac{\tau_2}{2} + \frac{\tau_1}{2} - \tau_2 + \phi\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_3)$	$\frac{v_{\mathrm{DC1}} \cdot \left(d\frac{\tau_2}{2} + \frac{\tau_1}{2} - \tau_2 + \phi\right)}{\omega_{\mathrm{s}} L}$	$\frac{v_{\mathrm{DC1}} \cdot \left(-d\frac{\tau_2}{2} + \tau_1 + \phi\right)}{\omega_{\mathrm{s}} L}$
$i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0)$	$\frac{v_{\mathrm{DC1}} \cdot \left(d \cdot (\frac{-\tau_2}{2} + \phi) + \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$	$\frac{v_{\mathrm{DC1}} \cdot \left(-d\frac{\tau_2}{2} + \frac{\tau_1}{2}\right)}{\omega_{\mathrm{s}} L}$

Table 3.2: Expressions for the inductor current $i_{\mathrm{L}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_{\mathrm{s}}/2$ for mode 1^{+} and mode 5 operation.

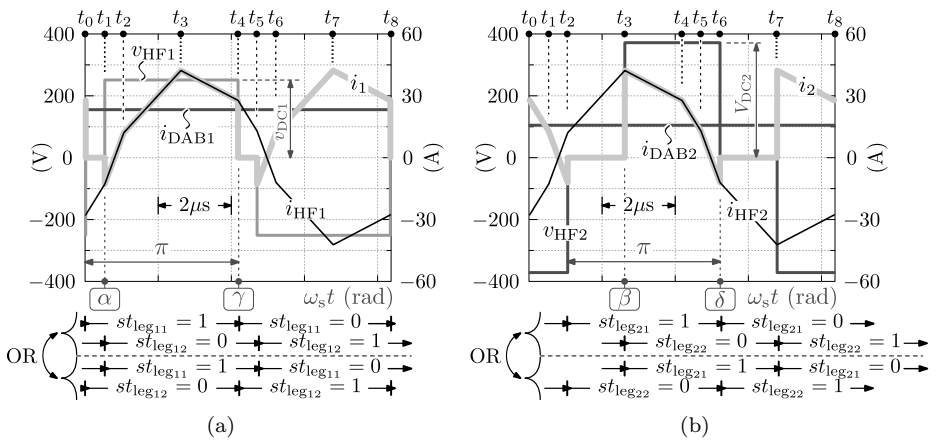


Figure 3.10: (a) Primary side and (b) secondary side bridge quantities (voltages and currents) that correspond with the example in Figure 3.9(a) (i.e. mode 1^{+}).

that need to be applied during the switching cycle in order to obtain the depicted voltages patterns ($v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$) are also indicated in the figures.

By analyzing the bridge leg states $st_{\mathrm{leg_{xx}}}$ and the associated switching devices that are conducting, it can be seen that the instantaneous DAB input and output currents $i_1(t)$ and $i_2(t)$ (also shown in Figures 3.10 and A.2) can once more be calculated from respectively $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ using (2.24) and (2.25). Lastly, the averaged DAB input current i_{DAB1} is obtained by evaluating (2.26), yielding[11]:

[11] Expressions for i_{DAB1} regarding all possible switching modes: see Table A.4 of Appendix A.

mode 1^+:

$$i_{\mathrm{DAB1},1^+} = \frac{-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{2\omega_{\mathrm{s}}L\pi}\cdot\big((\phi-\tau_2)^2+(\phi+\tau_1)^2-\tau_1\tau_2 \\ +\pi(\pi-2(\tau_1+\phi))\big) \qquad \forall\ -\tau_1+\pi\leqslant\phi\leqslant\tau_2, \tag{3.34}$$

mode 5:

$$i_{\mathrm{DAB1},5} = \frac{-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{2\omega_{\mathrm{s}}L\pi}\cdot\big(\tau_2^2-\tau_1\tau_2-2\tau_2\phi\big) \qquad \forall\ \tau_2-\tau_1\leqslant\phi\leqslant 0. \tag{3.35}$$

The averaged DAB input power p_1, evaluated one switching cycle T_{s}, can now be calculated with:

$$p_1 = i_{\mathrm{DAB1}}\cdot v_{\mathrm{DC1}}. \tag{3.36}$$

The expressions for the averaged DAB output current i_{DAB2} and output power p_2 can be derived in a similar way, or can be obtained by evaluating the DAB's power balance according to (2.31). It can be shown that the maximum and minimum achievable averaged DAB input currents $i_{\mathrm{DAB1,max}}$ and $i_{\mathrm{DAB1,min}}$ for DSPWM of the FBFB DAB occur for mode 1 operation and for $\tau_1=\tau_2=\pi$ rad., and are thus identical to (2.32) and (2.33) for PSM:

$$i_{\mathrm{DAB1,max}} = \frac{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{8f_{\mathrm{s}}L} \qquad \text{for } \phi=\pi/2;\tau_1=\tau_2=\pi;\ \text{mode } 1^+, \tag{3.37}$$

$$i_{\mathrm{DAB1,min}} = -\frac{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}{8f_{\mathrm{s}}L} \qquad \text{for } \phi=-\pi/2;\tau_1=\tau_2=\pi;\ \text{mode } 1^-, \tag{3.38}$$

presenting an upper limit to the employed equivalent inductance value L with respect to the desirable averaged DAB input current i_{DAB1}. The expressions for the phase-shift angle ϕ, required to achieve a given i_{DAB1}, with given pulse-width modulation angles τ_1 and τ_2, are obtained by rearranging (3.34) and (3.35):

$$\text{mode } 1^+: \qquad \phi_{1^+} = \frac{-\tau_1+\tau_2+\pi}{2} \\ \pm\sqrt{\frac{-(\tau_2-\pi)^2+\tau_1(2\pi-\tau_1)}{4}-\frac{i_{\mathrm{DAB1}}\cdot\omega_{\mathrm{s}}L\pi}{\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}}, \tag{3.39}$$

$$\text{mode } 5: \qquad \phi_5 = \frac{\tau_2-\tau_1}{2}+\frac{i_{\mathrm{DAB1}}\cdot\omega_{\mathrm{s}}L\pi}{\tau_2\cdot\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}}. \tag{3.40}$$

As mentioned above, a strong similarity exists between the voltage and current waveforms for operation of the DAB in mode 1^+ (positive power flow; $dir = 1$; Figure A.1(a)) and in mode 1^- (negative power flow; $dir = -1$; Figure A.1(b)). It can easily be seen from the mode 1^+ and mode 1^- voltage patterns that in mode 1^- operation the phase-shift angle ϕ_{1^-}, required to achieve a given negative averaged DAB input current $i_{\mathrm{DAB1,1^-}} \leqslant 0$, with given pulse-width modulation angles τ_1 and τ_2, can be directly calculated from the expression for ϕ_{1^+} (i.e. equation (3.39), mode 1^+ operation) by inputting $i_{\mathrm{DAB1}} = |i_{\mathrm{DAB1,1^-}}|$ into (3.39) and calculating ϕ_{1^-} with:

$$\text{mode } 1^- : \qquad \phi_{1^-} = -(\tau_1 + \phi_{1^+} - \tau_2), \tag{3.41}$$

where ϕ_{1^+} is calculated with (3.39) using $i_{\mathrm{DAB1}} = |i_{\mathrm{DAB1,1^-}}|$.

Similar as for PSM (see Section 2.1.2), the expression for the phase-shift angle ϕ_{1^+} (i.e. equation (3.39)) provides two solutions, dividing the mode 1^+ operating region, which is defined by (3.30), into a 'high RMS' and a 'low RMS' region[12]. The same goes for the mode 1^- operating region since ϕ_{1^-} is directly related to ϕ_{1^+} via (3.41). The value for ϕ_{1^+} at the boundary between the 'high RMS' and the 'low RMS' region, regarding mode 1^+ operation, is defined by the first term of (3.39). It can be shown in a similar way as was done for PSM that, in order to achieve efficient DAB operation in mode 1^+, ϕ_{1^+} should be calculated with the '$-\sqrt{}$' solution of (3.39). Taking into account the mode boundary condition (3.30), efficient DAB operation (i.e. regarding the RMS value of the HF AC-link currents) for mode 1^+ is thus obtained when:

$$-\tau_1 + \pi \leqslant \phi_{1^+} \leqslant \frac{-\tau_1 + \tau_2 + \pi}{2} \tag{3.42}$$

$\rightarrow$ assuring mode 1^+ operation with low AC-link circulating currents.

Referring to (3.41) for the indirect calculation of ϕ_{1^-} and to the mode 1^- boundary condition given in Table A.1, efficient mode 1^- DAB operation is consequently obtained when:

$$\frac{-\tau_1 + \tau_2 - \pi}{2} \leqslant \phi_{1^-} \leqslant \tau_2 - \pi \tag{3.43}$$

$\rightarrow$ assuring mode 1^- operation with low AC-link circulating currents.

[12] It is shown in Figure 2.5(a) of Section 2.1.2 that the RMS value I_{L} of the inductor current $i_{\mathrm{L}}(t)$ is significantly lower in the 'low-RMS' operating region compared to the 'high-RMS' operating region.

3.2.3 Current-Based Zero Voltage Switching (CB ZVS) Conditions

According to Section 2.1.3, theoretical 'current-based' zero voltage switching (CB ZVS) of a bridge leg is achieved when the drain to source current $i_{\mathrm{DS,S_{xx}}}$ of the switch S_{xx} which initiates the commutation, i.e. the switch which is turned off and causes a state change of the leg, is positive at the switching instant, $i_{\mathrm{DS,S_{xx}}}(t = t_{\mathrm{turn-off}}) \geqslant 0$. For the FBFB DAB, $i_{\mathrm{DS,S_{xx}}}$ of the individual switches can be calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$, using expressions (2.38)-(2.41) for the switches $S_{1\mathrm{x}}$ of the primary side active bridge and using expressions (2.42)-(2.45) for the switches $S_{2\mathrm{x}}$ of the secondary side active bridge. The drain to source currents $i_{\mathrm{DS,S_{xx}}}$ and corresponding drain to source voltages $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} of the FBFB DAB, regarding mode 1^+ operation according to the example in Figure 3.9(a), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure 3.10, are shown in Figures 3.11(a)-3.11(b) (switches $S_{1\mathrm{x}}$ of the primary side active bridge) and Figures 3.11(c)-3.11(d) (switches $S_{2\mathrm{x}}$ of the secondary side active bridge). $i_{\mathrm{DS,S_{xx}}}$ and $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} regarding mode 5 operation according to the example in Figure 3.9(b), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure A.2, are shown in Figures A.3(a)-A.3(b) (Appendix A, switches $S_{1\mathrm{x}}$ of the primary side active bridge) and Figures A.3(c)-A.3(d) (Appendix A, switches $S_{2\mathrm{x}}$ of the secondary side active bridge). For both the current patterns in Figure 3.11 (mode 1^+) and Figure A.3 (mode 5) the turn-off currents of the individual switches are indicated by a '★' and are clearly positive, confirming that for these examples CB ZVS is achieved.

By analyzing the current and voltage patterns for the different switching modes and when defining:

- t_α: switching instant that corresponds with the positive rising edge of $v_{\mathrm{HF1}}(t)$,
- t_β: switching instant that corresponds with the positive rising edge of $v_{\mathrm{HF2}}(t)$,
- t_γ: switching instant that corresponds with the positive falling edge of $v_{\mathrm{HF1}}(t)$,
- t_δ: switching instant that corresponds with the positive falling edge of $v_{\mathrm{HF2}}(t)$,

the generalized set of CB ZVS constraints defined by (2.46) still holds, i.e.

$$\begin{aligned} s^{\pm} \cdot i_{\mathrm{HF1}}(t_\alpha) &\geqslant 0, & s^{\pm} \cdot i_{\mathrm{HF2}}(t_\beta) &\geqslant 0, \\ s^{\pm} \cdot i_{\mathrm{HF1}}(t_\gamma) &\geqslant 0, & s^{\pm} \cdot i_{\mathrm{HF2}}(t_\delta) &\geqslant 0. \end{aligned} \tag{3.44}$$

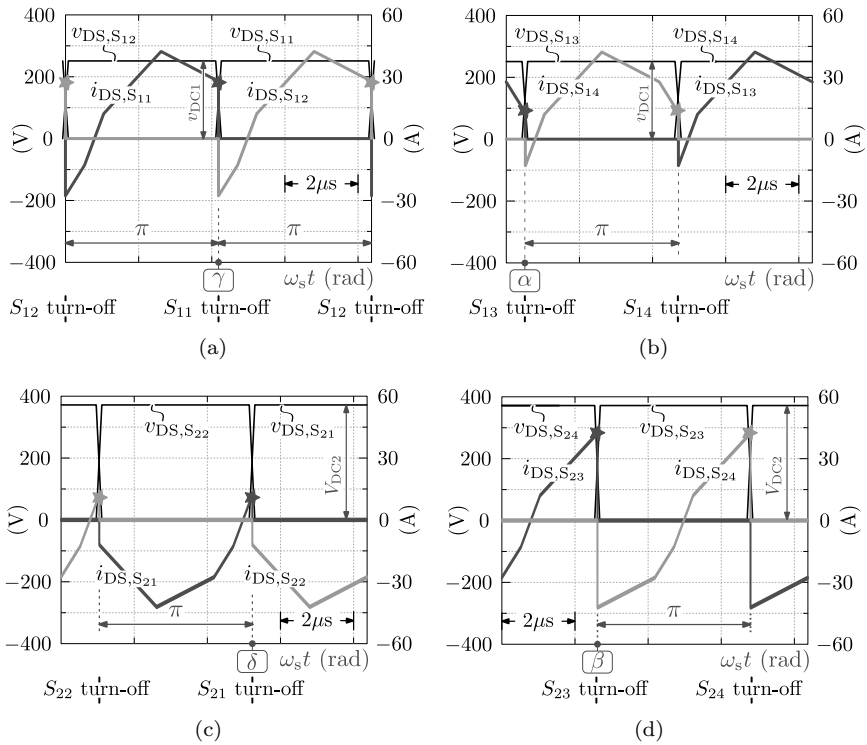


Figure 3.11: Drain to source currents $i_{\mathrm{DS,S_{xx}}}$ and corresponding drain to source voltages $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} of the FBFB DAB regarding mode 1^+ operation according to the example in Figure 3.9(a), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure 3.10. (a)-(b) Switches $S_{1\mathrm{x}}$ of the primary side active bridge: (a) bridge leg_{11}, (b) bridge leg_{12}. (c)-(d) Switches $S_{2\mathrm{x}}$ of the secondary side active bridge: (c) bridge leg_{21}, (d) bridge leg_{22}.

Consequently, CB ZVS is achieved in the primary side active bridge when conditions $s^{\pm} \cdot i_{\mathrm{HF1}}(t_\alpha) \geqslant 0$ and $s^{\pm} \cdot i_{\mathrm{HF1}}(t_\gamma) \geqslant 0$ are satisfied while CB ZVS is achieved in the secondary side active bridge when conditions $s^{\pm} \cdot i_{\mathrm{HF2}}(t_\beta) \geqslant 0$ and $s^{\pm} \cdot i_{\mathrm{HF2}}(t_\delta) \geqslant 0$ are satisfied. Switching instances $t_{\theta_{\mathrm{i}}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ and bridge currents $i_{\mathrm{HF1}}(t_{\theta_{\mathrm{i}}})$ and $i_{\mathrm{HF2}}(t_{\theta_{\mathrm{i}}})$, required to evaluate (3.44), are listed in Table 3.3 for mode 1^+ and mode 5 operation, and in Table A.5 of Appendix A for all possible switching modes of the FBFB DAB. Remind that multiplier $s^{\pm}$ is introduced in Section 2.1.3 of Chapter 2 in order to bring generality to the DAB's ZVS conditions/equations:

	mode 1^+		mode 5	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$
β	$t_\beta = t_3$	$i_{\mathrm{HF}2}(t_3)$	$t_\beta = t_2$	$i_{\mathrm{HF}2}(t_2)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_6$	$i_{\mathrm{HF}2}(t_6) = -i_{\mathrm{HF}2}(t_2)$	$t_\delta = t_3$	$i_{\mathrm{HF}2}(t_3)$

Table 3.3: Switching instances $t_{\theta_\mathrm{i}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ and bridge currents $i_{\mathrm{HF}1}(t_{\theta_\mathrm{i}})$ and $i_{\mathrm{HF}2}(t_{\theta_\mathrm{i}})$ required to evaluate (3.44) for mode 1^+ and mode 5 operation.

$$s^{\pm} = \begin{cases} 1 & \text{for switching instances } t_{\theta_\mathrm{i}} = \{t_\beta, t_\gamma\}, \\ -1 & \text{for switching instances } t_{\theta_\mathrm{i}} = \{t_\alpha, t_\delta\}. \end{cases} \tag{3.45}$$

Angles $\theta_\mathrm{i} = \{\alpha, \beta, \gamma, \delta\}$ defined by $\theta = \omega_\mathrm{s} t$, e.g. $\alpha = \omega_\mathrm{s} \cdot t_\alpha$, are shown in Figures 3.10 and 3.11 (mode 1^+) and in Figures A.2 and A.3 (mode 5) of Appendix A.

3.2.4 Commutation Inductances

It is mentioned in Section 2.2.2 that when considering CB ZVS, substantial parts of the calculated (i.e. using (3.44)) ZVS regions involve incomplete bridge commutations due to the presence of (parasitic) switch capacitances [96]. It is shown in Section 4.1 that this effect is most pronounced in the regions where the primary side referred voltage conversion ratio defined by (2.21) substantially differs from one, i.e. $d >> 1$ and $d << 1$, as well as along the boundary between the low power switching mode (i.e. mode 5) and the high power switching mode (i.e. mode 1). Consequently, the prediction of ZVS using the CB ZVS conditions defined by (3.44) and the derivation of corresponding modulation schemes will, in reality, inevitably lead to hard-switching operation, reduced conversion efficiency, and, in all probability, destruction of the semiconductor switching devices. In order to deal with this deficiency, in Section 3.3 a novel current-dependent charge-based (CDCB) ZVS analysis and corresponding CDCB ZVS verification method is proposed in which the parasitic output capacitances of the switches are taken into account. This enables to accurately describe the DAB's ZVS conditions, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions. However, as the CB ZVS conditions according to (3.44) serve as absolute minimum constraints in the CDCB ZVS verification method, the calculated CDCB ZVS operating regions (reality) are even more restricted than the calculated CB ZVS regions (theoretical). It is shown in Section 4.1 that when applying the proposed CDCB ZVS verification method and when thus including the switch output capacitances in the analysis, full-operating-range ZVS modulation

which involves smooth transitions[13] between the low power switching mode (i.e. mode 5) and the high power switching mode (i.e. mode 1) cannot be achieved with the traditional implementation of the DAB's HF AC-link, i.e. a transformer and optionally an external series inductor L_{ext} (cf. Figure 3.7). As steps in the modulation parameter trajectories are highly undesirable, a solution to overcome this problem is absolutely required. This solution is proposed below by means of 'commutation inductances' which in Section 4.1 are identified as an essential HF AC-link modification[14] for achieving full-operating-range ZVS modulation that involves smooth trajectories of the modulation parameters $\mathbf{x}$.

Commutation inductances are defined as inductances that are placed in parallel with active bridge 1 (L_{c1}, between nodes A and B) and/or with active bridge 2 (L_{c2}, between nodes P and Q), as shown in Figure 3.7. The new lossless DAB model for the FBFB DAB converter with commutation inductances is shown in Figure 3.12, where

$$L'_{\text{c2}} = \left(\frac{n_1}{n_2}\right)^2 \cdot L_{\text{c2}}. \tag{3.46}$$

It is shown below that the bridge-paralleled commutations inductances always have a beneficial contribution to the ZVS conditions due to the injection of a small reactive current in the respective active bridge. Commutation current $i_{\text{L}_{\text{c1}}}(t)$ is induced in L_{c1} by voltage $v_{\text{HF1}}(t)$ while commutation current $i'_{\text{L}_{\text{c2}}}(t)$ is induced in L'_{c2} by voltage $v'_{\text{HF2}}(t)$ (see Figure 3.12), affecting the primary and secondary side bridge currents $i_{\text{HF1}}(t)$ and $i_{\text{HF2}}(t)$ according to:

$$i_{\text{HF1}}(t) = i_{\text{L}}(t) + i_{\text{L}_{\text{c1}}}(t), \tag{3.47}$$

$$i_{\text{HF2}}(t) = i'_{\text{HF2}}(t) \cdot \frac{n_1}{n_2} = \left(i_{\text{L}}(t) - i'_{\text{L}_{\text{c2}}}(t)\right) \cdot \frac{n_1}{n_2}, \tag{3.48}$$

where the dynamics of $i_{\text{L}_{\text{c1}}}(t)$ and $i'_{\text{L}_{\text{c2}}}(t)$ are described by:

$$\frac{\mathrm{d}i_{\text{L}_{\text{c1}}}(t)}{\mathrm{d}t} = \frac{v_{\text{HF1}}(t)}{L_{\text{c1}}}, \tag{3.49}$$

$$\frac{\mathrm{d}i'_{\text{L}_{\text{c2}}}(t)}{\mathrm{d}t} = \frac{v'_{\text{HF2}}(t)}{L'_{\text{c2}}}. \tag{3.50}$$

The expressions for the commutation currents at the different switching instances, $i_{\text{L}_{\text{c1}}}(t_{\text{i}})$ and $i'_{\text{L}_{\text{c2}}}(t_{\text{i}})$, are obtained by rewriting (3.49) and (3.50) as:

[13] A smooth mode transition is a transition from the one switching mode to the other without steps in the modulation parameters $\mathbf{x}$.

[14] Is has been mentioned in inter alia [83, 84, 96] that the magnetizing inductance of the transformer can be used to provide additional commutation charge in the switches. However no detailed investigation (and subsequent modulation scheme) concerning EB or CDCB ZVS is given.

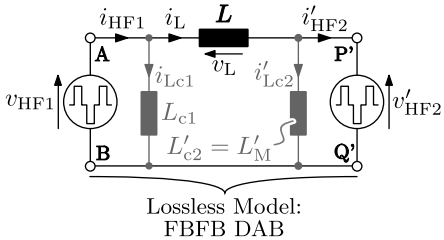


Figure 3.12: Lossless model of the full bridge - full bridge (FBFB) DAB DC–DC converter regarding dual-sided duty-cycle modulation (DSPWM), with the inclusion of HF AC-link commutation inductances.

$$i_{\mathrm{L_{c1}}}(t_{\mathrm{i}}) = i_{\mathrm{L_{c1}}}(t_{\mathrm{i-1}}) + \frac{1}{L_{\mathrm{c1}}} \int_{t_{\mathrm{i-1}}}^{t_{\mathrm{i}}} v_{\mathrm{HF1}} \mathrm{d}t \quad \forall \quad t_{\mathrm{i-1}} < t_{\mathrm{i}}, \tag{3.51}$$

$$i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}}) = i'_{\mathrm{L_{c2}}}(t_{\mathrm{i-1}}) + \frac{1}{L'_{\mathrm{c2}}} \int_{t_{\mathrm{i-1}}}^{t_{\mathrm{i}}} v'_{\mathrm{HF2}} \mathrm{d}t \quad \forall \quad t_{\mathrm{i-1}} < t_{\mathrm{i}}, \tag{3.52}$$

and establishing these expressions in the first half cycle of the switching period T_{s} (voltage intervals I...IV, within $0 < t \leqslant T_{\mathrm{s}}/2$). The resulting systems of equations regarding mode 1^+ and mode 5 are given in Appendix A, equation systems (A.13)-(A.16). The equation systems for the other switching modes are not given for the sake of brevity. By applying[15]:

$$i_{\mathrm{L_{c1}}}(t + T_{\mathrm{s}}/2) = -i_{\mathrm{L_{c1}}}(t), \tag{3.53}$$

$$i'_{\mathrm{L_{c2}}}(t + T_{\mathrm{s}}/2) = -i'_{\mathrm{L_{c2}}}(t), \tag{3.54}$$

solutions for $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$ and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}})$ are obtained which are given in Table 3.4[16] regarding mode 1^+ and mode 5, and in Table A.6 of Appendix A regarding all possible switching modes.

Figure 3.13 (mode 1^+), showing the primary side and secondary side bridge quantities (voltages and currents), is a repetition of Figure 3.10 with the difference that now commutation inductances L_{c1} and L_{c2} are added in the HF AC-link. I.e. the same conditions regarding voltages v_{DC1} and V_{DC2}, transformer ratio n_1/n_2, equivalent inductance value L, and modulation parameters $\mathbf{x}$ as in Figure 3.10 are

[15] In steady-state operation, the voltages $v_{\mathrm{HF1}}(t)$ and $v'_{\mathrm{HF2}}(t)$, and thus also the currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ repeat every half-cycle with reversed signs.

[16] Note that $V'_{\mathrm{DC2}} = \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}$.

	mode 1^+		mode 5	
t_i	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{V'_{\mathrm{DC2}}\left(\frac{\tau_2}{2}-\phi\right)}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$	$-\frac{v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$\frac{-v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{DC2}}\left(\tau_1-\frac{\tau_2}{2}+\phi-\pi\right)}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$	$\frac{-v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$\frac{v_{\mathrm{DC1}}\left(\frac{\tau_1}{2}+\phi-\pi\right)}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$	$\frac{v_{\mathrm{DC1}}\left(\frac{\tau_1}{2}-\tau_2+\phi\right)}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\left(\frac{\tau_1}{2}-\tau_2+\phi\right)}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$	$\frac{v_{\mathrm{DC1}}\left(\frac{\tau_1}{2}+\phi\right)}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{DC2}}\left(\frac{\tau_2}{2}-\phi\right)}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$	$\frac{v_{\mathrm{DC1}}\frac{\tau_1}{2}}{\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{DC2}}\frac{\tau_2}{2}}{\omega_\mathrm{s}L'_{\mathrm{c2}}}$

Table 3.4: Expressions for the commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for mode 1^+ and mode 5 operation.

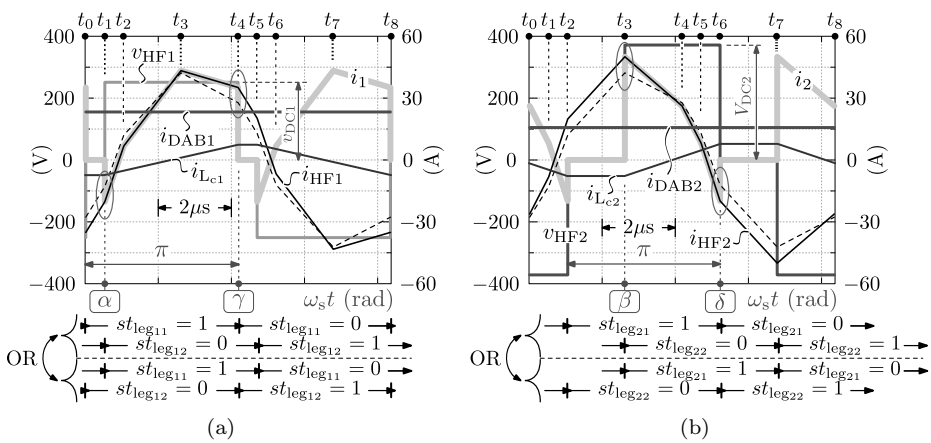


Figure 3.13: Repetition of Figure 3.10 (mode 1^+) with the difference that now commutation inductances L_{c1} and L_{c2} are added in the HF AC-link, i.e. $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1\ \mu\mathrm{H}$ in this figure compared to $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$ for Figure 3.10. (a) Primary side and (b) secondary side bridge quantities (voltages and currents).

used but now $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1\ \mu\mathrm{H}$ instead of $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$. Due to the injection of small reactive 'commutation' currents $i_{\mathrm{L_{c1}}}(t)$ and $i_{\mathrm{L_{c2}}}(t)$ into the respective active bridges, the total bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ are beneficially influenced regarding the ZVS conditions given by (3.44). In Figure 3.13 the previous (i.e. conform Figure 3.10) bridge currents are shown as dashed lines. It can be seen

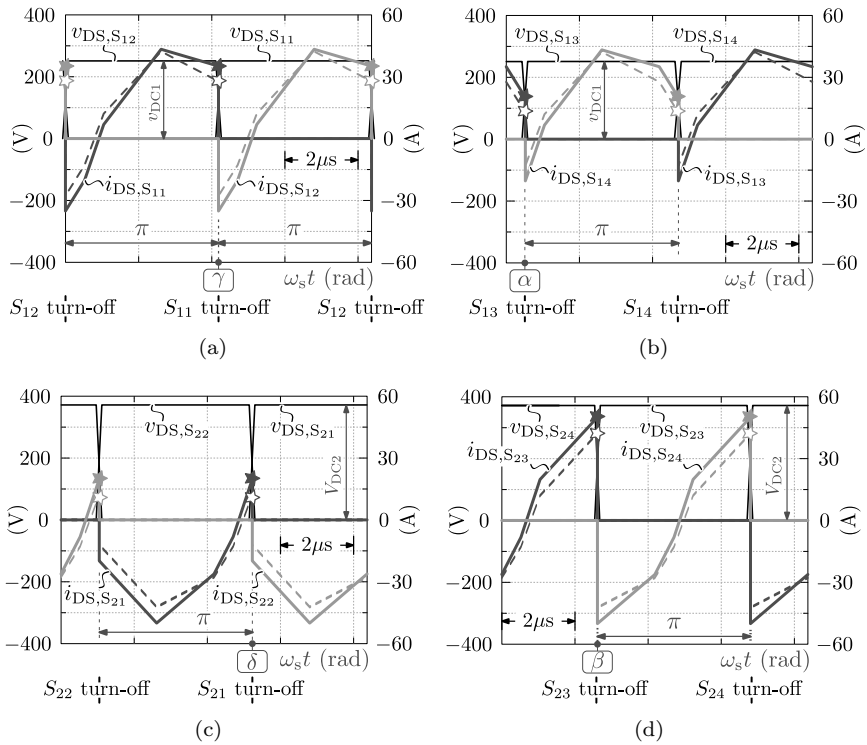


Figure 3.14: Repetition of Figure 3.11 (mode 1^+) with the difference that now commutation inductances L_{c1} and L_{c2} are added in the HF AC-link, i.e. $L_{c1} = L_{c2} = 62.1$ μH in this figure compared to $L_{c1} = L_{c2} = \infty$ for Figure 3.11. (a)-(b) Drain to source currents $i_{DS,S_{1x}}$ in switches S_{1x} of the primary side active bridge: (a) bridge leg_{11}, (b) bridge leg_{12}. (c)-(d) Drain to source currents $i_{DS,S_{2x}}$ in switches S_{2x} of the secondary side active bridge: (c) bridge leg_{21}, (d) bridge leg_{22}.

that for the primary side active bridge (see Figure 3.13(a)) both $s^{\pm} \cdot i_{HF1}(t_\alpha)$ and $s^{\pm} \cdot i_{HF1}(\gamma)$ have increased, which is also the case for $s^{\pm} \cdot i_{HF1}(t_\beta)$ and $s^{\pm} \cdot i_{HF1}(\delta)$ regarding the secondary side active bridge (see Figure 3.13(b)). Figure A.4 of Appendix A is a similar repetition of Figure A.2 for mode 5 operation, showing the same benefit regarding the ZVS conditions.

Figure 3.14 (mode 1^+), showing drain to source currents $i_{DS,S_{xx}}$ and corresponding drain to source voltages $v_{DS,S_{xx}}$ of all the switches S_{xx} of the DAB, is a repetition of Figure 3.11, again using the same conditions except for the commutation inductances which are now $L_{c1} = L_{c2} = 62.1$ μH instead of $L_{c1} = L_{c2} = \infty$ for Figure 3.11. It can be seen that the turn-off current $i_{DS,S_{xx}}(t = t_{turn-off})$ of all switches (primary and secondary side) has increased. The previous turn-off

currents (i.e. conform Figure 3.11) are indicated by a '☆' while the new ones (i.e. commutation inductance included) are indicated with a '★'. Figure A.5 of Appendix A is a similar repetition of Figure A.3 for mode 5 operation, showing the same benefit regarding the ZVS conditions (i.e. an increased turn-off current $i_{\mathrm{DS,S_{xx}}}(t = t_{\mathrm{turn-off}})$ for all the switches S_{xx} of the DAB.

It is clear from Figures 3.13 and A.4 that commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i_{\mathrm{L_{c2}}}(t)$ have an impact on the bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$. This impact is always beneficial regarding the ZVS conditions of the active bridges. Nevertheless, due to their reactive nature, $i_{\mathrm{L_{c1}}}(t)$ and $i_{\mathrm{L_{c2}}}(t)$ do not contribute to the DAB's power transfer and are therefore not present in any of the expressions for i_{DAB1}, i_{DAB2}, p_1, or p_2. Although here only shown for mode 1^+ and mode 5, commutation inductances L_{c1} and L_{c2} benefit the ZVS conditions for all twelve switching modes, being an inherent result of the reactive power injection into the bridges. It should be noted that the addition of commutation inductance(s) does not necessarily lead to (substantially) higher overall conduction losses since the freedom to optimally control the modulation parameters $\mathbf{x}$ under ZVS conditions becomes bigger. This is exactly what was needed to meet the needs. The same remark can be made for the requirements of the HF input and output filters (evidently, commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i_{\mathrm{L_{c2}}}(t)$ also have an impact on the HF components of the instantaneous DAB input and output currents $i_1(t)$ and $i_2(t)$) which, for the same reason, do not necessarily have to be made substantially larger. The effect of commutation inductances in the HF AC-link on the ZVS operating range is further investigated in Chapter 4 where different scenarios are extensively discussed. Note also that in this work L_{c2} is implemented by the magnetizing inductance of the HF AC-link transformer ($L_{\mathrm{c2}} = L_{\mathrm{M}}$), avoiding increased volume and costs, while for L_{c1} and external inductor is used (see Section 5.2). The subject of further investigation/optimization might be to consider a T-type instead of a Pi-type equivalent circuit model for the HF AC-link which allows the use of the transformer's leakage inductances in order to obtain the same behavior.

In order to illustrate the absolute necessity of commutation inductance(s), Figure 3.15 shows an example of the primary side and secondary side bridge quantities (voltages and currents) at the boundary between mode 5 (low power mode) and mode 1^+ (high power mode) operation. When goaling for continuous modulation parameter trajectories, this boundary always needs to be crossed when going from low to high power operation or vice versa. It can be seen from Figure 3.15 that at this boundary condition the falling edges of $v_{\mathrm{HF1}}(t)$ and $v_{\mathrm{HF2}}(t)$ fall together (i.e. $\phi = 0$, $t_\gamma = t_\delta$). Without commutation inductances, the CB ZVS conditions $s^{\pm} \cdot i_{\mathrm{HF1}}(t_\gamma) \geqslant 0$ and $s^{\pm} \cdot i_{\mathrm{HF2}}(t_\delta) \geqslant 0$ can now only be simultaneously satisfied when $i_{\mathrm{HF1}}(t_\gamma) = i_{\mathrm{HF2}}(t_\delta) = 0$, as illustrated in the example (dashed lines). This is, according to the CDCB ZVS constraints in Section 3.3, far from sufficient to achieve ZVS in reality (i.e. due to the presence of parasitic switch capacitances). As shown in the figure, the addition of commutation inductances

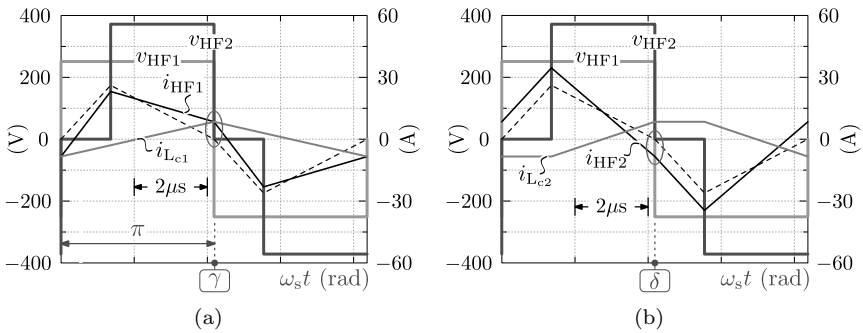


Figure 3.15: Example of the primary side and secondary side bridge quantities (voltages and currents) at the boundary between mode 5 (low power mode) and mode 1^+ (high power mode) operation. The waveforms are derived using $v_{DC1} = 250$ V, $V_{DC2} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{c1} = L_{c2} = 62.1$ μH, $\phi = 0$ rad., $\tau_1 = \pi$ rad., $\tau_2 = 2.12$ rad. and $f_s = 120$ kHz.

has an advantageous impact on the bridge currents (see solid lines), making it easier to satisfy (3.44) and thus providing a solution for the above problem.

3.3 Zero Voltage Switching (ZVS)

Given a set of input parameters (v_{DC1}, V_{DC2}, L, L_{c1}, L_{c2}, and n_1/n_2) and modulation parameters $\mathbf{x}$, it can be verified if theoretical current-based (CB) ZVS is achieved for all semiconductor switching devices S_{xx} of the DAB by evaluating (3.44). The bridge currents $i_{\mathrm{HF1}}(t_{\theta_{\mathrm{i}}})$ and $i_{\mathrm{HF2}}(t_{\theta_{\mathrm{i}}})$ at the different switching instances $t_{\theta_{\mathrm{i}}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ required to evaluate (3.44) are given in Table A.5 for all possible switching modes. The bridge currents $i_{\mathrm{HF1}}(t_{\mathrm{i}})$ and $i_{\mathrm{HF2}}(t_{\mathrm{i}})$ required in Table A.5 are calculated using (3.47) and (3.48), which include commutation inductances L_{c1} and L_{c2}, and using the expressions for respectively $i_{\mathrm{L}}(t_{\mathrm{i}})$, $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$, and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}})$ listed in:

- $i_{\mathrm{L}}(t_{\mathrm{i}}) \rightarrow$ Table A.3;
- $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$ and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}}) \rightarrow$ Table A.6.

The time instances t_{i} required in Table A.5 are calculated using the expressions in Table A.2. In case a particular t_{i} lies in the second half cycle of the switching period (i.e. $t_{\mathrm{i}} > T_{\mathrm{s}}/2$), these expressions should be combined with the expressions given in the right inset of Table 3.1. Remind that for a given set of modulation parameters $\mathbf{x}$, the switching mode can be determined based on the mode boundary conditions listed in Table A.1.

It has been mentioned in the previous sections that when the DAB is operated using modulation schemes that rely on the theoretical CB ZVS conditions (i.e. when ZVS is verified using the steps described above), in reality hard-switching operation with reduced conversion efficiency and, in all probability, destruction of the semiconductor switching devices occurs in the 'critical parts' of the calculated (CB) ZVS regions. The reason is that the CB ZVS constraints defined by (3.44) do not take into account the resetting of the parasitic output capacitances of the switching devices. In order to deal with this deficiency, in this section a novel current-dependent charge-based (CDCB) ZVS verification method is proposed [86, 87] whereby the charge that is required to reset the parasitic output capacitances of the switches during commutation of the bridge legs, as well as the time dependency of the commutation currents, are taken into account. This results in a more accurate description of the DAB's ZVS conditions, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions. Below, for better understanding, firstly the ZVS principle is described in detail. Thereafter, the CDCB ZVS verification method is outlined.

3.3.1 Zero Voltage Switching (ZVS) Principle

As shown in Figure 3.16(a), each switch S_{xx} of the DAB can be represented by a power transistor T_{xx}, an anti-parallel (body) diode D_{xx}, and a parasitic capacitance C_{xx}. Regarding commutation of a bridge leg it is the output capacitance C_{oss}, which is composed of the gate to drain capacitance C_{GD} and the drain to source capacitance C_{DS} ($C_{oss} = C_{DS} + C_{GD}$), of the switch that needs to be considered[17]: $C_{xx} = C_{oss}$. It can be seen from Figures 3.16(b) (logarithmic x and y axis) and 3.16(c) (logarithmic y axis only) that C_{oss} shows a highly nonlinear dependency[18]

[17]The gate to source capacitance C_{GS} is only relevant regarding the design of the gate drive units.

[18]Remind that in this work only Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are considered. In Section 5.1.1 the FAIRCHILD FCH76N60NF SupreMOS® high-voltage super-junction MOSFETs are selected for the active bridges of the DAB due to their excellent soft-switching performance, inter alia the nonlinear output capacitance and low reverse recovery charge, in combination with a low on-resistance. The capacitance characteristics shown in Figures 3.16(b) and 3.16(c) are those of the FAIRCHILD FCH76N60NF.

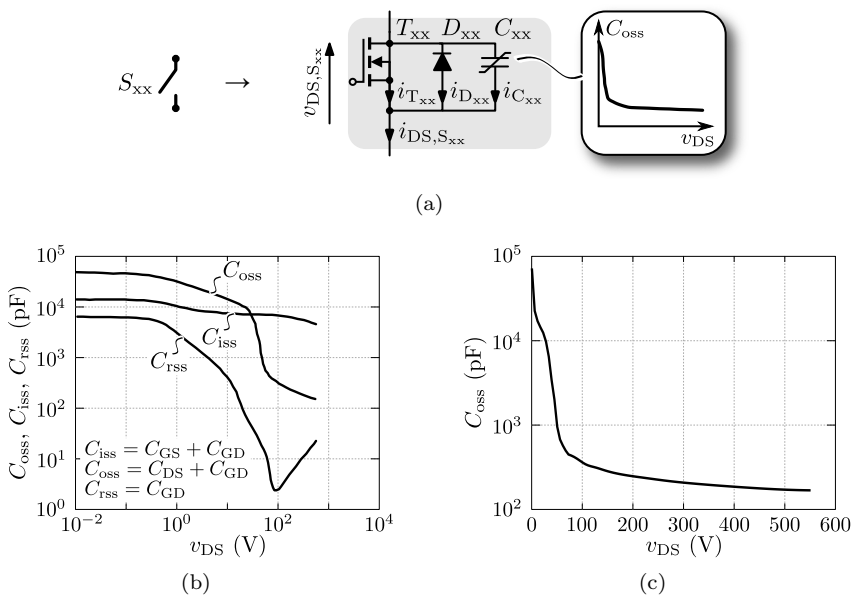


Figure 3.16: (a) Representation of the HF high-voltage switches S_{xx} (MOSFETs) of the DAB. (b)-(c) Capacitance characteristics (measured at a gate to source voltage of $V_{GS} = 0$ V) of the selected FAIRCHILD FCH76N60NF SupreMOS® high-voltage super-junction MOSFETs; (b) $C_{oss}(v_{DS})$, $C_{iss}(v_{DS})$, and $C_{rss}(v_{DS})$ shown on a logarithmic x and y axis, (c) $C_{oss}(v_{DS})$ shown on a arithmetic x axis and logarithmic y axis.

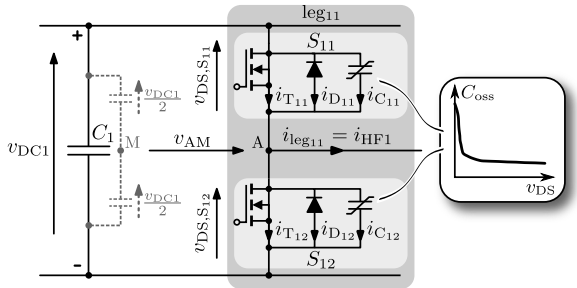


Figure 3.17: Bridge leg of the DAB converter.

on the drain to source voltage v_{DS}. The zero voltage switching (ZVS) principle is explained using Figure 3.17, considering the commutation of leg current $i_{\mathrm{leg_{11}}} = i_{\mathrm{HF1}}$ from the bottom switch S_{12} to the top switch S_{11} of bridge $\mathrm{leg_{11}}$, and using Figure 3.18 which depicts an example of the currents and voltages related to such a commutation. Note that the same ZVS principle applies for a commutation from the top to the bottom switch of $\mathrm{leg_{11}}$. The top inset of Figure 3.18 depicts measured gate voltages $v_{\mathrm{GS,S_{11}}}$ and $v_{\mathrm{GS,S_{12}}}$ of the two leg switches S_{11} and S_{12}, while the middle inset shows the measured leg current $i_{\mathrm{leg_{11}}} (= i_{\mathrm{HF1}})$ as well as the measured drain to source voltage $v_{\mathrm{DS,S_{12}}}$ of the bottom switch S_{12}. The bottom inset of Figure 3.18 shows the waveforms obtained from a simulation which is performed under the same conditions as for the measurements. The bottom inset (simulation) is a zoomed image (finer time scale) of the middle figure inset, enabling discussion of the currents (according to Figure 3.17) that flow in the individual switch components (i.e. T_{xx}, D_{xx}, and C_{xx}). Note that $i_{\mathrm{leg_{11}}}$ is negative at the switching instant t_{sw}.

The total parasitic leg capacitance to be considered for the commutation, $C_{\mathrm{leg_{11}}}$, is highly nonlinear and is calculated with:

$$C_{\mathrm{leg_{11}}}(v_{\mathrm{AM}}) = C_{12}(v_{\mathrm{DS,S_{12}}}) + C_{11}(v_{\mathrm{DS,S_{11}}}), \tag{3.55}$$

since during the commutation DC-bus capacitor C_1 acts as a short and C_{11} and C_{12} are thus effectively connected in parallel. Voltage $v_{\mathrm{AM}}(t)$ is the voltage between the (fictitious) DC-bus midpoint and connection point A (see Figure 3.17):

$$v_{\mathrm{AM}}(t) = v_{\mathrm{DS,S_{12}}}(t) - \frac{v_{\mathrm{DC1}}}{2}, \tag{3.56}$$

where

$$v_{\mathrm{DC1}} = v_{\mathrm{DS,S_{11}}}(t) + v_{\mathrm{DS,S_{12}}}(t). \tag{3.57}$$

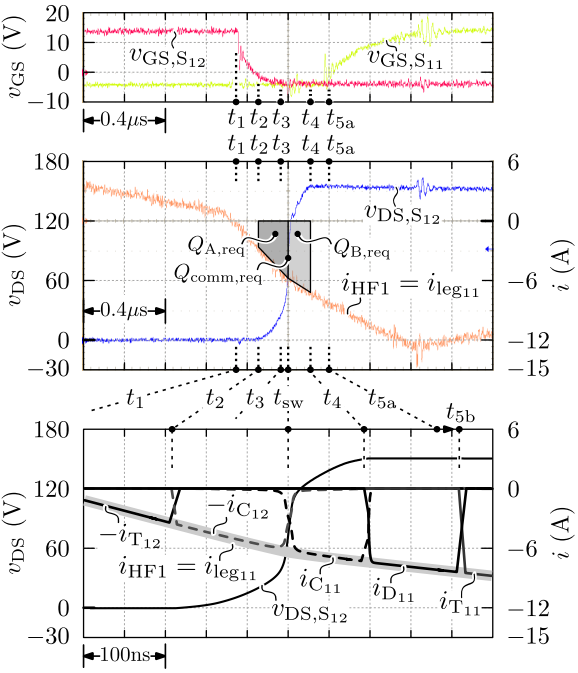


Figure 3.18: Example of a commutation of current $i_{leg_{11}} = i_{HF1}$ from the bottom switch S_{12} to the top switch S_{11} of bridge leg$_{11}$ (cf. Figure 3.17). The DC-bus voltage of the bridge, v_{DC1}, is 150 V for this example.

$C_{leg_{11}}$ for the FAIRCHILD FCH76N60NF MOSFETs is depicted in Figure 3.19. The capacitance trajectories (arrowed lines[19]) that are followed during a bridge commutation depend on the DC-bus voltage v_{DC1}, as three-dimensionally shown in Figure 3.19(a) and two-dimensionally shown in Figure 3.19(b). Note that the 150 V line corresponds with the example in Figure 3.18.

Quasi lossless ZVS turn-off— At time instant t_1 (see Figure 3.18) the gate of switch S_{12}, carrying a positive drain to source current, $i_{DS,S_{12}}(t = t_1) > 0$, is turned off. At the moment of turn-off the current is flowing through transistor T_{12} of switch S_{12}: $i_{T_{12}}(t = t_1) = i_{DS,S_{12}}(t = t_1) = -i_{leg_{11}}(t = t_1)$. After a small time delay ($= t_2 - t_1$) the gate threshold voltage is reached and the channel resistance $R_{DS,S_{12}}$ of T_{12} starts to increase rapidly. This causes the leg current $i_{leg_{11}}$ to start flowing through the total parasitic leg capacitance $C_{leg_{11}}$ (current divider network consisting of $R_{DS,S_{12}}$ and $C_{leg_{11}}$). It can be seen from Figure 3.19 that $C_{leg_{11}}$ is big at the moment when the conductive channel of T_{12} starts to open (i.e. at time

[19]For commutation from the top switch to the bottom switch of the bridge leg, the arrows are pointing in the opposite direction.

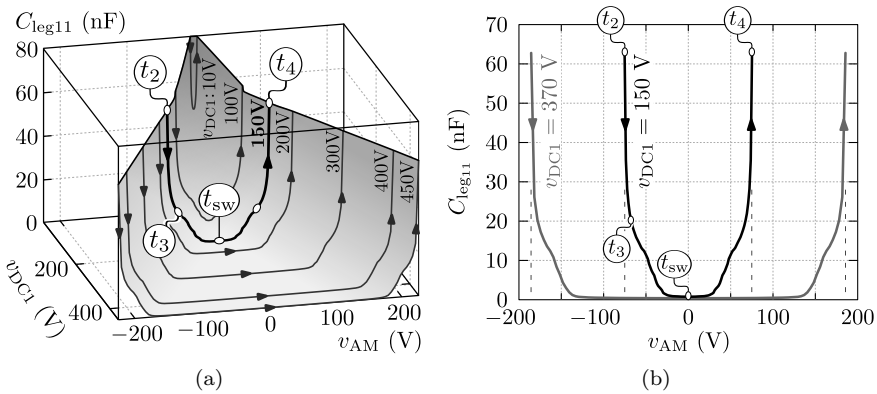


Figure 3.19: Total parasitic bridge leg capacitance $C_{\text{leg}_{11}}(v_{\text{AM}})$ for the FAIRCHILD FCH76N60NF MOSFETs used in the active bridges of the DAB. (a) 3-D representation, (b) 2-D representation. The arrowed lines indicate the capacitance trajectory that is followed during commutation of a bridge leg. The 150 V line corresponds with the example in Figure 3.18.

instant t_2). As $v_{\text{DS,S}_{12}}$ is low at this moment, the increase of $R_{\text{DS,S}_{12}}$ causes $i_{\text{leg}_{11}}$ to mainly start flowing through C_{12} ($i_{\text{C}_{12}} \approx -i_{\text{leg}_{11}}$; see Figure 3.18, bottom inset). This is because C_{12} is big and C_{11} small at low $v_{\text{DS,S}_{12}}$ (i.e. conform Figure 3.16). Quasi lossless turn-off of switch S_{12} is achieved if the drain-source channel of T_{12} is completely opened before $i_{\text{leg}_{11}}$ has provided enough charge to $C_{\text{leg}_{11}}$ for causing a significant rise of drain to source voltage $v_{\text{DS,S}_{12}}$ (quasi zero voltage turn-off of switch S_{12}). This can be seen in Figure 3.18 where at time instant t_3 the gate of S_{12} is completely off while $v_{\text{DS,S}_{12}}$ is still low (C_{12} is bypassing $i_{\text{leg}_{11}}$, keeping $v_{\text{DS,S}_{12}}$ low at turn-off).

Quasi lossless ZVS turn-on— After time instant t_2 (see Figure 3.18), a resonance occurs between $C_{\text{leg}_{11}}$ and the HF AC-link inductances. During this resonance $C_{\text{leg}_{11}}$ is charged by $i_{\text{leg}_{11}}$ (t_2–t_4). Due to the resulting increase of $v_{\text{DS,S}_{12}}$, the value of C_{12} drops while that of C_{11} rises, causing the leg current $i_{\text{leg}_{11}}$ to transfer from C_{12} to C_{11}. This current transfer occurs around t_{sw} as can be seen from the bottom inset of Figure 3.18. At t_4 the resonant transition completes ($v_{\text{DS,S}_{12}}$ has reached the DC-bus voltage level v_{DC1}), putting diode D_{11} into conduction. Now, transistor T_{11} can be turned on under (quasi) zero voltage. At time instant $t_{5\text{a}}$, when the anti-parallel diode D_{11} of switch S_{11} is conducting, the gate of S_{11} is turned on. After a small time delay ($= t_{5\text{b}} - t_{5\text{a}}$), $v_{\text{GS,S}_{11}}$ reaches the gate threshold voltage and transistor T_{11} effectively takes over the leg current from D_{11} ($i_{\text{T}_{11}}(t \geqslant t_{5\text{b}}) = i_{\text{leg}_{11}}(t \geqslant t_{5\text{b}})$). ZVS turn-on of switch S_{11} is thus achieved when the resonant transition (t_2–t_4) of drain to source voltage $v_{\text{DS,S}_{12}}$ from ≈ 0 V to v_{DC1} completes before transistor T_{11} is turned on. For the commutation from the bottom switch S_{12} to the top switch

S_{11} of the bridge leg, the absolute minimum requirement to achieve this is that the leg current is flowing into the leg, charging $C_{\mathrm{leg}_{11}}$ during time interval t_2-t_4 until voltage $v_{\mathrm{DS,S}_{12}}$ reaches v_{DC1}. This requirement corresponds with the theoretical CB ZVS verification according to (3.44).

3.3.2 Current-Dependent Charge-Based (CDCB) ZVS Verification Method

Based on above considerations a general procedure is introduced in order, for a given set of input parameters (v_{DC1}, V_{DC2}, L, L_{c1}, L_{c2}, and n_1/n_2) and modulation parameters $\mathbf{x}$, to ascertain whether quasi lossless ZVS commutation is achieved in all semiconductor switching devices S_{xx} of the DAB. Figure 3.20 summarizes the complete procedure which relies on a current-dependent charge-based (CDCB) ZVS analysis.

Step 1: Starting from the given set of input parameters and keeping in mind that for the commutation from the bottom switch to the top switch of a bridge leg the current needs to flow into the leg (charging of C_{leg}) and out of the leg (discharging of C_{leg}) when commutation from the top switch to the bottom switch is considered, in a first step the CB ZVS constraints given by (3.44) need to be verified[20]. Therefore the bridge currents $i_{\mathrm{HF1}}(t_{\theta_{\mathrm{i}}})$ and $i_{\mathrm{HF2}}(t_{\theta_{\mathrm{i}}})$ at the different switching instances $t_{\theta_{\mathrm{i}}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ need to be calculated by following the different steps outlined at the beginning of this section (i.e. Section 3.3).

Step 2: The total charge $Q_{\mathrm{comm,req}}(v_{\mathrm{DC}})$ needed to complete the commutation of a bridge leg (i.e. charging/discharging of C_{leg}), can be calculated as:

$$Q_{\mathrm{comm,req}}(v_{\mathrm{DC}}) = \int_0^{v_{\mathrm{DC}}} (C_{11}(v_{\mathrm{C}}) + C_{12}(v_{\mathrm{C}}))\mathrm{d}v_{\mathrm{C}} = \int_0^{v_{\mathrm{DC}}} 2 \cdot C_{\mathrm{oss}}(v_{\mathrm{C}})\mathrm{d}v_{\mathrm{C}}, \quad (3.58)$$

with v_{DC} the corresponding DC-bus voltage. $Q_{\mathrm{comm,req}}(v_{\mathrm{DC}})$ can be subdivided into charges $Q_{\mathrm{A,req}}(v_{\mathrm{DC}})$ and $Q_{\mathrm{B,req}}(v_{\mathrm{DC}})$, each required to achieve a voltage change of half the DC-bus voltage ($v_{\mathrm{DC}}/2$):

$$Q_{\mathrm{A,req}}(v_{\mathrm{DC}}) = Q_{\mathrm{B,req}}(v_{\mathrm{DC}}) = \frac{Q_{\mathrm{comm,req}}(v_{\mathrm{DC}})}{2}. \quad (3.59)$$

In the following, $Q_{\mathrm{A,req}}(v_{\mathrm{DC}})$ and $Q_{\mathrm{B,req}}(v_{\mathrm{DC}})$ ($= Q_{\mathrm{A,req}}(v_{\mathrm{DC}})$) are referred to as $Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}})$. $Q_{\mathrm{comm,req}}(v_{\mathrm{DC}})$ and $Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}})$ for the used MOSFETs (i.e. the FAIRCHILD FCH76N60NF) are depicted in Figure 3.21 (left inset) which

[20] The theoretical CB ZVS conditions according to (3.44) serve as absolute minimum constraints in the CDCB ZVS verification method.

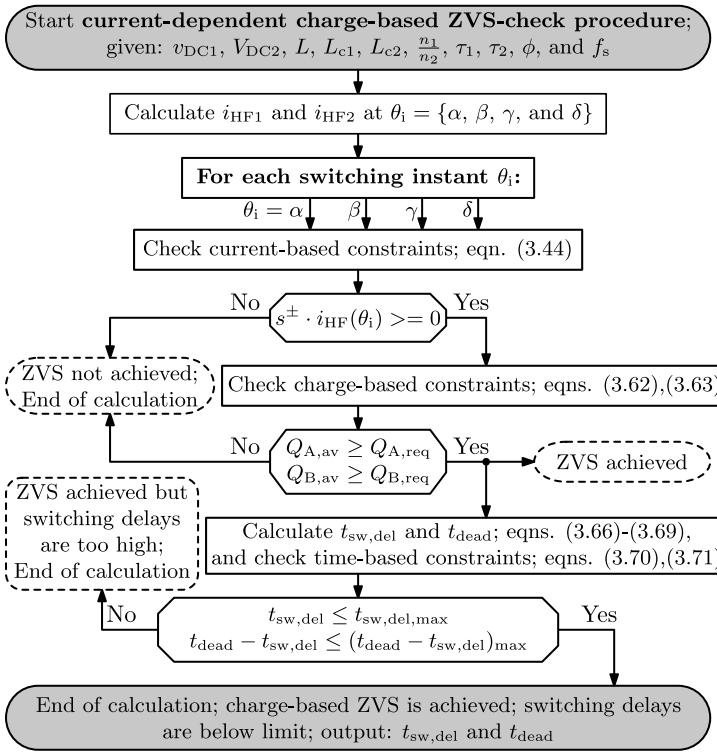


Figure 3.20: Procedure to verify if current-dependent charge-based (CDCB) ZVS is achieved in all switching devices of the DAB, and if the switching delays are below an upper limit.

is obtained using the circuit simulator GeckoCIRCUITS^{TM} [105] in which the capacitor model given by (3.58) is applied and in which a nonlinear capacitor $C(u)$ that is based on small-signal measurements (such as in Figures 3.16(b) and 3.16(c)) can be directly employed [101]. Note that $Q_{comm,req}$ and $Q_{A/B,req}$ do not only depend on the DC-bus voltage v_{DC} but also slightly on the leg current as can be seen from Figure 3.21 (right inset). Therefore they are derived based on an average leg current, $i_{leg,AVG}$, applying a margin (0.05 μC and 0.1 μC) for component variances and circuit imperfections:

$$Q_{comm,req}(v_{DC}) = Q_{comm}(v_{DC}, i_{leg,AVG}) + 0.1\ \mu C, \tag{3.60}$$

$$Q_{A/B,req}(v_{DC}) = Q_{A/B}(v_{DC}, i_{leg,AVG}) + 0.05\ \mu C. \tag{3.61}$$

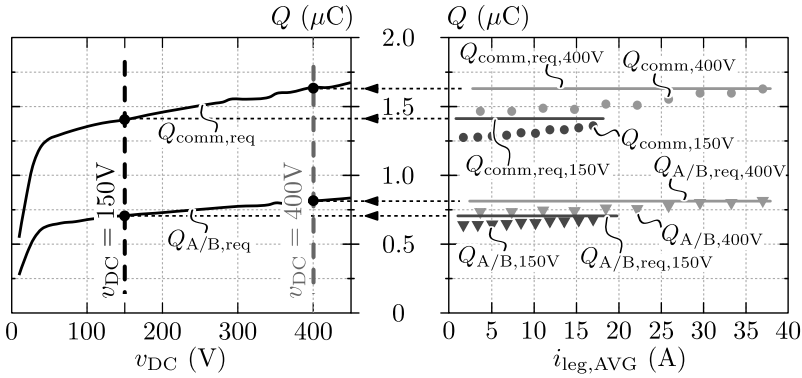


Figure 3.21: Charges required to achieve a voltage change of the full DC-bus voltage (v_{DC}) and of half the DC-bus voltage ($v_{\text{DC}}/2$) during commutation of a bridge leg (i.e. charging/discharging of the parasitic leg capacitance C_{leg}).

(Quasi) lossless ZVS commutation of a bridge leg occurs when the charges $Q_{\text{A,av}}$ and $Q_{\text{B,av}}$, which are available in the current i_{HF} of the bridge leg before (i.e. $Q_{\text{A,av}}$) and after (i.e. $Q_{\text{B,av}}$) the considered switching instant $t_{\theta_{\text{i}}} = \{t_\alpha, t_\beta, t_\gamma, \text{ or } t_\delta\}$, are higher than or equal to $Q_{\text{A/B,req}}(v_{\text{DC}})$. $Q_{\text{A,av}}$ and $Q_{\text{B,av}}$ are calculated using respectively a backward and a forward integration of leg current i_{HF}, starting at the considered switching instant θ_{i} ($= \omega_{\text{s}} \cdot t_{\theta_{\text{i}}}$):

$$Q_{\text{A,av}} = s^{\pm} \cdot \left[\left(\sum_{j=1}^{n_{\text{B}}} \int_{\theta_{i-j+1}}^{\theta_{i-j}} \frac{-i_{\text{HF}}}{\omega_{\text{s}}} \text{d}\theta \right) + \int_{\theta_{i-n_{\text{B}}}}^{\theta_x} \frac{-i_{\text{HF}}}{\omega_{\text{s}}} \text{d}\theta \right] \geqslant Q_{\text{A/B,req}}(v_{\text{DC}}), \tag{3.62}$$

$$Q_{\text{B,av}} = s^{\pm} \cdot \left[\left(\sum_{j=1}^{m_{\text{F}}} \int_{\theta_{i+j-1}}^{\theta_{i+j}} \frac{i_{\text{HF}}}{\omega_{\text{s}}} \text{d}\theta \right) + \int_{\theta_{i+m_{\text{F}}}}^{\theta_y} \frac{i_{\text{HF}}}{\omega_{\text{s}}} \text{d}\theta \right] \geqslant Q_{\text{A/B,req}}(v_{\text{DC}}), \tag{3.63}$$

with,

- θ_{x}: first instant prior to θ_{i} where i_{HF} crosses zero;
- θ_{y}: first instant after θ_{i} where i_{HF} crosses zero;
- $\theta_{\text{i}-\text{j}}$ and $\theta_{\text{i}+\text{j}}$: switching instances of the three remaining bridges;
- n_{B}: number of switching instances between θ_{x} and θ_{i}; $0 \leqslant n_{\text{B}} \leqslant 3$;

- m_{F}: number of switching instances between θ_{i} and θ_{y}; $0 \leqslant m_{\mathrm{F}} \leqslant 3$;
- $s^{\pm}$: multiplier, defined by (3.45);
- $i_{\mathrm{HF}} = i_{\mathrm{HF1}}$ for $\theta_{\mathrm{i}} = \{\alpha, \gamma\}$, $i_{\mathrm{HF}} = i_{\mathrm{HF2}}$ for $\theta_{\mathrm{i}} = \{\beta, \delta\}$.

These current-dependent charge-based (CDCB) constraints need to be verified at each switching instant $\theta_{\mathrm{i}} = \{\alpha, \beta, \gamma, \text{ and } \delta\}$. θ_{x}, θ_{y}, n_{B}, and m_{F} are calculated using the given set of input parameters which determine the bridge currents i_{HF1} and i_{HF2}. It can be shown that, independent from the applied switching mode, $0 \leqslant n_{\mathrm{B}} + m_{\mathrm{F}} \leqslant 3$. Summarizing, for each switching instant $\theta_{\mathrm{i}} = \{\alpha, \beta, \gamma, \text{ and } \delta\}$, $Q_{\mathrm{A,av}}$, $Q_{\mathrm{B,av}}$, and $Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}})$ are determined as:

- Switching instant $\theta_{\mathrm{i}} = \alpha$:
  - $Q_{\mathrm{A,av},\alpha}$ is calculated with (3.62), using $i_{\mathrm{HF}} = i_{\mathrm{HF1}}$;
  - $Q_{\mathrm{B,av},\alpha}$ is calculated with (3.63), using $i_{\mathrm{HF}} = i_{\mathrm{HF1}}$;
  - $Q_{\mathrm{A/B,req},\alpha}$ $(=Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}{=}v_{\mathrm{DC1}}))$ is determined by using the primary side DC-link voltage v_{DC1} in the left inset of Figure 3.21.
- Switching instant $\theta_{\mathrm{i}} = \beta$:
  - $Q_{\mathrm{A,av},\beta}$ is calculated with (3.62), using $i_{\mathrm{HF}} = i_{\mathrm{HF2}}$;
  - $Q_{\mathrm{B,av},\beta}$ is calculated with (3.63), using $i_{\mathrm{HF}} = i_{\mathrm{HF2}}$;
  - $Q_{\mathrm{A/B,req},\beta}$ $(=Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}{=}V_{\mathrm{DC2}}))$ is determined by using the secondary side DC-link voltage V_{DC2} in the left inset of Figure 3.21.
- Switching instant $\theta_{\mathrm{i}} = \gamma$:
  - $Q_{\mathrm{A,av},\gamma}$ is calculated with (3.62), using $i_{\mathrm{HF}} = i_{\mathrm{HF1}}$;
  - $Q_{\mathrm{B,av},\gamma}$ is calculated with (3.63), using $i_{\mathrm{HF}} = i_{\mathrm{HF1}}$;
  - $Q_{\mathrm{A/B,req},\gamma}$ $(=Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}{=}v_{\mathrm{DC1}}))$ is determined by using the primary side DC-link voltage v_{DC1} in the left inset of Figure 3.21.
- Switching instant $\theta_{\mathrm{i}} = \delta$:
  - $Q_{\mathrm{A,av},\delta}$ is calculated with (3.62), using $i_{\mathrm{HF}} = i_{\mathrm{HF2}}$;
  - $Q_{\mathrm{B,av},\delta}$ is calculated with (3.63), using $i_{\mathrm{HF}} = i_{\mathrm{HF2}}$;
  - $Q_{\mathrm{A/B,req},\delta}$ $(=Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}{=}V_{\mathrm{DC2}}))$ is determined by using the secondary side DC-link voltage V_{DC2} in the left inset of Figure 3.21.

$Q_{\mathrm{A/B,req}}(v_{\mathrm{DC1}})$ is the minimum required commutation charge for the primary side active bridge of the DAB and is further referred to as $Q_{\mathrm{A/B,req,p}}$, while $Q_{\mathrm{A/B,req}}(V_{\mathrm{DC2}})$ is the minimum required commutation charge for the secondary side active bridge of the DAB and is further referred to as $Q_{\mathrm{A/B,req,s}}$, where:

$$Q_{\mathrm{A/B,req,p}} = Q_{\mathrm{A/B,req},\alpha} = Q_{\mathrm{A/B,req},\gamma}, \tag{3.64}$$

$$Q_{\mathrm{A/B,req,s}} = Q_{\mathrm{A/B,req},\beta} = Q_{\mathrm{A/B,req},\delta}. \tag{3.65}$$

Step 3: In order to achieve switching at the predicted moment, the switching delay $t_{\mathrm{sw,del}}$ ($= t_{\mathrm{sw}} - t_2$, see Figure 3.18) has to be dynamically compensated in the controller. Moreover, a dynamic dead-time (t_{dead}) adaptation is required for each bridge leg, avoiding back commutation and hard turn on (i.e. a switch should be turned on after its anti-parallel (body) diode is put into conduction). At each switching instant θ_{i}, $t_{\mathrm{sw,del}}$ and t_{dead} are respectively calculated with:

$$t_{\mathrm{sw,del}} = \frac{\theta_{\mathrm{i}} - \theta_{\mathrm{A}}}{\omega_{\mathrm{s}}}, \tag{3.66}$$

$$t_{\mathrm{dead}} = \frac{\theta_{\mathrm{B}} - \theta_{\mathrm{A}}}{\omega_{\mathrm{s}}}, \tag{3.67}$$

where θ_{A} and θ_{B} are the instances where respectively the backward and the forward integration (equations (3.62) and (3.63); starting point θ_{i}) of the corresponding leg current equal the charge $Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}})$ needed to achieve a voltage change of half the DC-bus voltage. θ_{A} and θ_{B} are thus found by solving:

$$s^{\pm} \cdot \int_{\theta_{\mathrm{i}}}^{\theta_{\mathrm{A}}} \frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta = Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}), \tag{3.68}$$

$$s^{\pm} \cdot \int_{\theta_{\mathrm{i}}}^{\theta_{\mathrm{B}}} \frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}} \mathrm{d}\theta = Q_{\mathrm{A/B,req}}(v_{\mathrm{DC}}). \tag{3.69}$$

Step 4: Lastly it is verified if $t_{\mathrm{sw,del}}$ and $(t_{\mathrm{dead}} - t_{\mathrm{sw,del}})$ are smaller than an upper limit, avoiding too long commutation delays. This yields a set of time-based constraints:

$$t_{\mathrm{sw,del}} \leqslant t_{\mathrm{sw,del,max}}, \tag{3.70}$$

$$t_{\mathrm{dead}} - t_{\mathrm{sw,del}} \leqslant (t_{\mathrm{dead}} - t_{\mathrm{sw,del}})_{\mathrm{max}}. \tag{3.71}$$

A reasonable value for these maximum limits is 500 ns (for the considered FAIRCHILD FCH76N60NF MOSFETs).

Examples

For convenience, all quantities involved in the CDCB ZVS verification method outlined above are depicted in Figure 3.22, considering fictitious patterns of the bridge currents i_{HF1} and i_{HF2}. Each sub-figure represents one of the four switching instances $\theta_{\mathrm{i}} = \{\alpha,\ \beta,\ \gamma,\ \text{and}\ \delta\}$, i.e. Figure 3.22(a) corresponds with switching instance $\theta_{\mathrm{i}} = \alpha$, Figure 3.22(b) with switching instance $\theta_{\mathrm{i}} = \beta$, Figure 3.22(c) with switching instance $\theta_{\mathrm{i}} = \gamma$, and Figure 3.22(d) with switching instance $\theta_{\mathrm{i}} = \delta$.

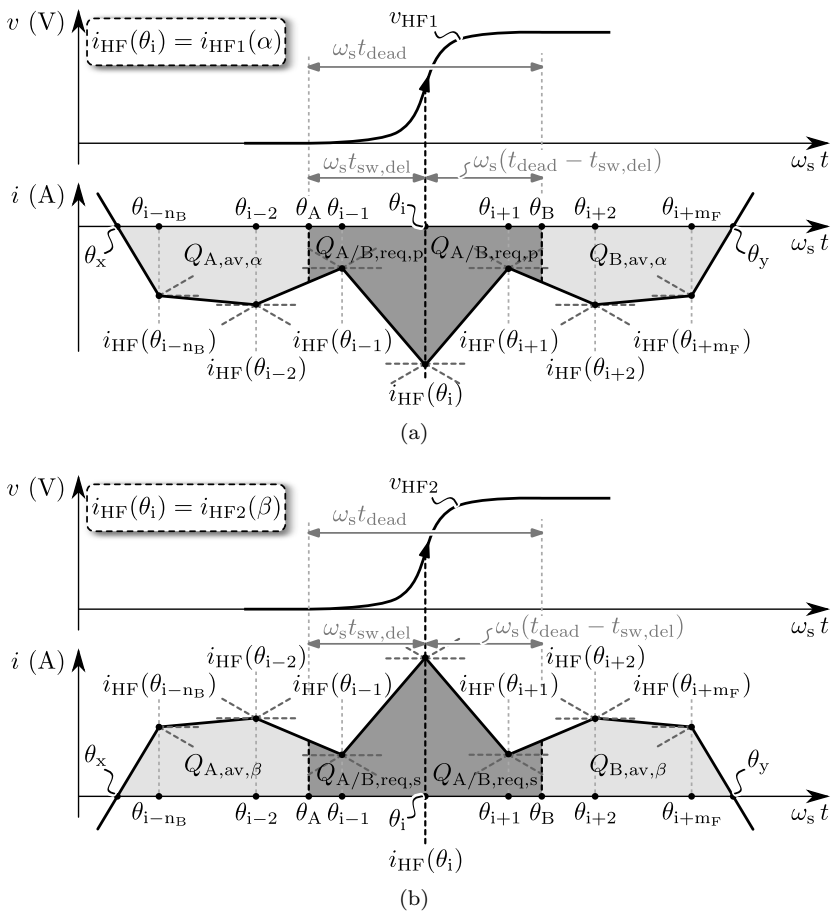
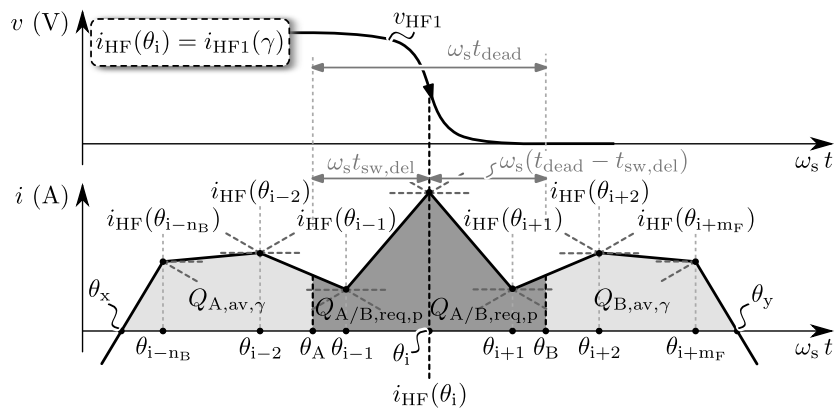
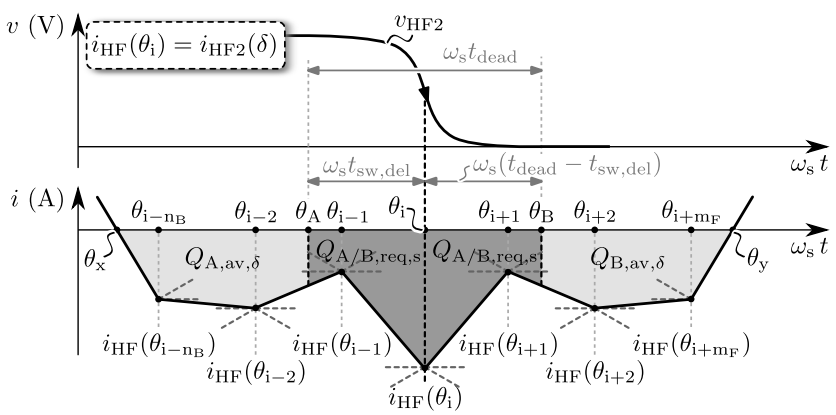


Figure 3.22: Fictitious illustration of the different quantities involved in the CDCB ZVS verification method, regarding (a) switching instant $\theta_{\mathrm{i}} = \alpha$, (b) switching instant $\theta_{\mathrm{i}} = \beta$, (c) switching instant $\theta_{\mathrm{i}} = \gamma$, and (d) switching instant $\theta_{\mathrm{i}} = \delta$ (continued on the next page).

For each switching instant, $Q_{\mathrm{A,av}}$, $Q_{\mathrm{B,av}}$, $Q_{\mathrm{A/B,req,p}}$, and $Q_{\mathrm{A/B,req,s}}$, which need to satisfy (3.62) and (3.63) in order to achieve CDCB ZVS, are visualized. The switching delays $t_{\mathrm{sw,del}}$ and the dead times t_{dead} (see equations (3.66)-(3.69)) are also shown in the figures. Note that the different current patterns are meant for illustration only and are therefore drawn in 'a most general way', i.e. they are physically not possible to achieve in steady state operation of the DAB. In particular the number of switching instances n_{B} between θ_{x} and θ_{i}, and the number of switching instances m_{F} between θ_{i} and θ_{y} cannot be both equal to three as is



(c)



(d)

Cont. Figure 3.22: Fictitious illustration of the different quantities involved in the CDCB ZVS verification method, regarding (a) switching instant $\theta_{\mathrm{i}} = \alpha$, (b) switching instant $\theta_{\mathrm{i}} = \beta$, (c) switching instant $\theta_{\mathrm{i}} = \gamma$, and (d) switching instant $\theta_{\mathrm{i}} = \delta$.

the case in the figures (remind that independent from the applied switching mode, $0 \leqslant n_{\mathrm{B}} + m_{\mathrm{F}} \leqslant 3$, see above).

A 'real world' example for demonstrating the CDCB ZVS verification method is given below (see Figures 3.23 - 3.25), regarding a random mode 5 operating point of the DAB. This example is used in Section 4.2 in order to derive a directly employable analytical solution for the calculation of the modulation parameters $\mathbf{x}$ which lead to full-operating-range CDCB ZVS operation. Figure 3.23 depicts the primary side referred AC-link terminal voltages v_{HF1} and v'_{HF2}, and inductor current i_{L} for the considered operating point, which is obtained using $v_{\mathrm{DC1}} = 250$ V, $V_{\mathrm{DC2}} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH, $f_{\mathrm{s}} = 120$ kHz, $\phi = -0.12$ rad., $\tau_1 = 1.53$ rad., and $\tau_2 = 0.94$ rad. The switching instances $\theta_{\mathrm{i}} = \{\alpha,\ \beta,\ \gamma,$ and $\delta\}$ at which the CDCB ZVS constraints need to be evaluated are also indicated in Figure 3.23. The primary side bridge quantities (i.e. v_{HF1} and i_{HF1}) that correspond to this operating point are shown in Figure 3.24 while Figure 3.25 depicts the corresponding secondary side bridge quantities (i.e. v_{HF2} and i_{HF2}). Remind that i_{HF1} is required in order to evaluate the CDCB ZVS constraint functions at switching instances $\theta_{\mathrm{i}} = \{\alpha$ and $\gamma\}$ while i_{HF2} is required for performing the evaluation at switching instances $\theta_{\mathrm{i}} = \{\beta$ and $\delta\}$. For both Figures 3.24 and 3.25, sub-figures '(b)' are a repetition of sub-figures '(a)', each putting the focus on a different switching instant. Sub-figure '(a)' of Figure 3.24 highlights switching instant $\theta_{\mathrm{i}} = \alpha$ while sub-figure '(b)' highlights switching instant $\theta_{\mathrm{i}} = \gamma$. Sub-figure '(a)' of Figure 3.25 highlights switching instant $\theta_{\mathrm{i}} = \beta$ while sub-figure '(b)' highlights switching instant $\theta_{\mathrm{i}} = \delta$. Sub-figures '(c)' are a zoomed image of the areas indicated in sub-figures '(a)' while sub-figures '(d)' are a zoomed image of the areas indicated in sub-figures '(b)'. For each switching instant $\theta_{\mathrm{i}} = \{\alpha,\ \beta,\ \gamma,$ and

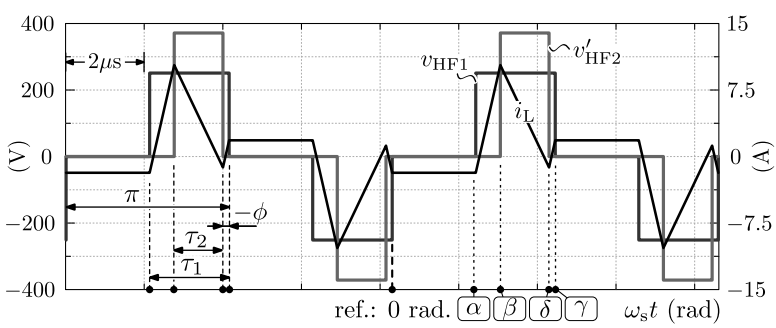


Figure 3.23: 'Real world' example used to demonstrate the CDCB ZVS verification method, regarding a random mode 5 operating point of the DAB. The considered operating point is derived using $v_{\mathrm{DC1}} = 250$ V, $V_{\mathrm{DC2}} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{\mathrm{c1}} = L_{\mathrm{c2}} = 62.1$ μH, $f_{\mathrm{s}} = 120$ kHz, $\phi = -0.12$ rad., $\tau_1 = 1.53$ rad., and $\tau_2 = 0.94$ rad.

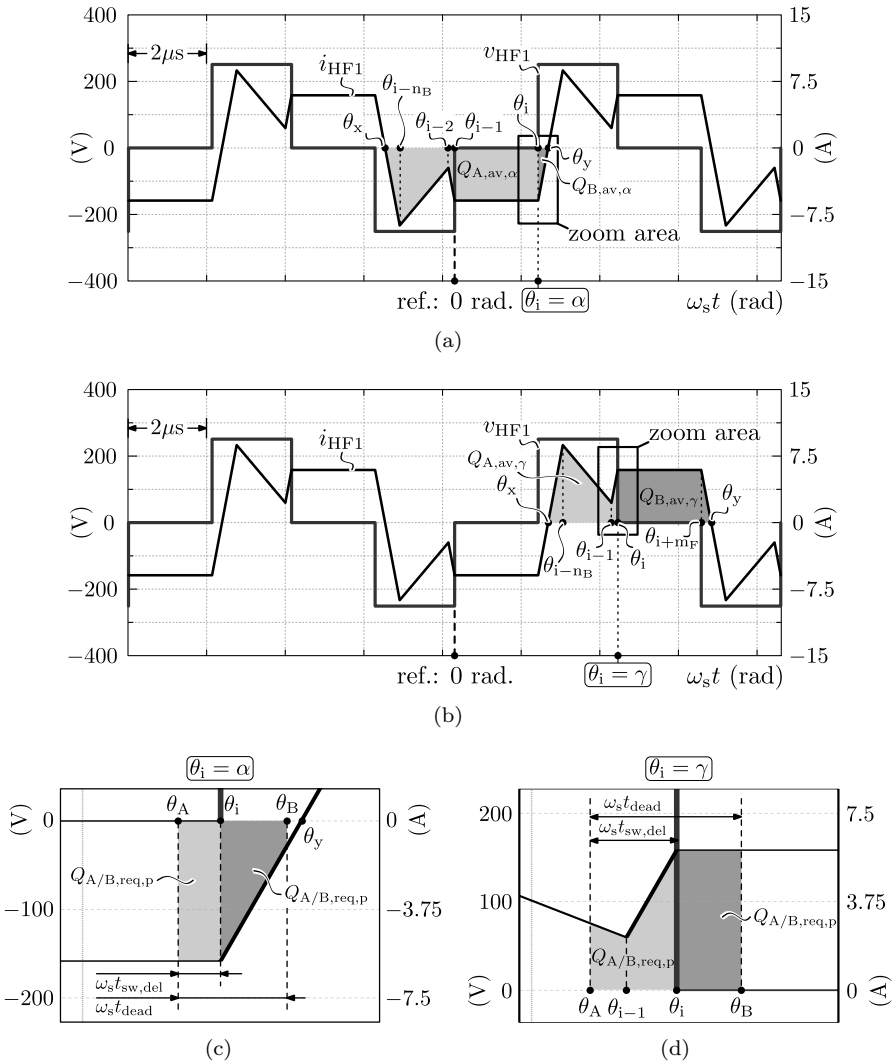


Figure 3.24: Primary side bridge quantities (i.e. v_{HF1} and i_{HF1}) and the corresponding quantities that are involved in the proposed CDCB ZVS verification method, regarding the operating point depicted in Figure 3.23.

$\delta\}$, all quantities involved in the CDCB ZVS verification method outlined above are shown in the figures:

- Switching instant $\theta_i = \alpha$:

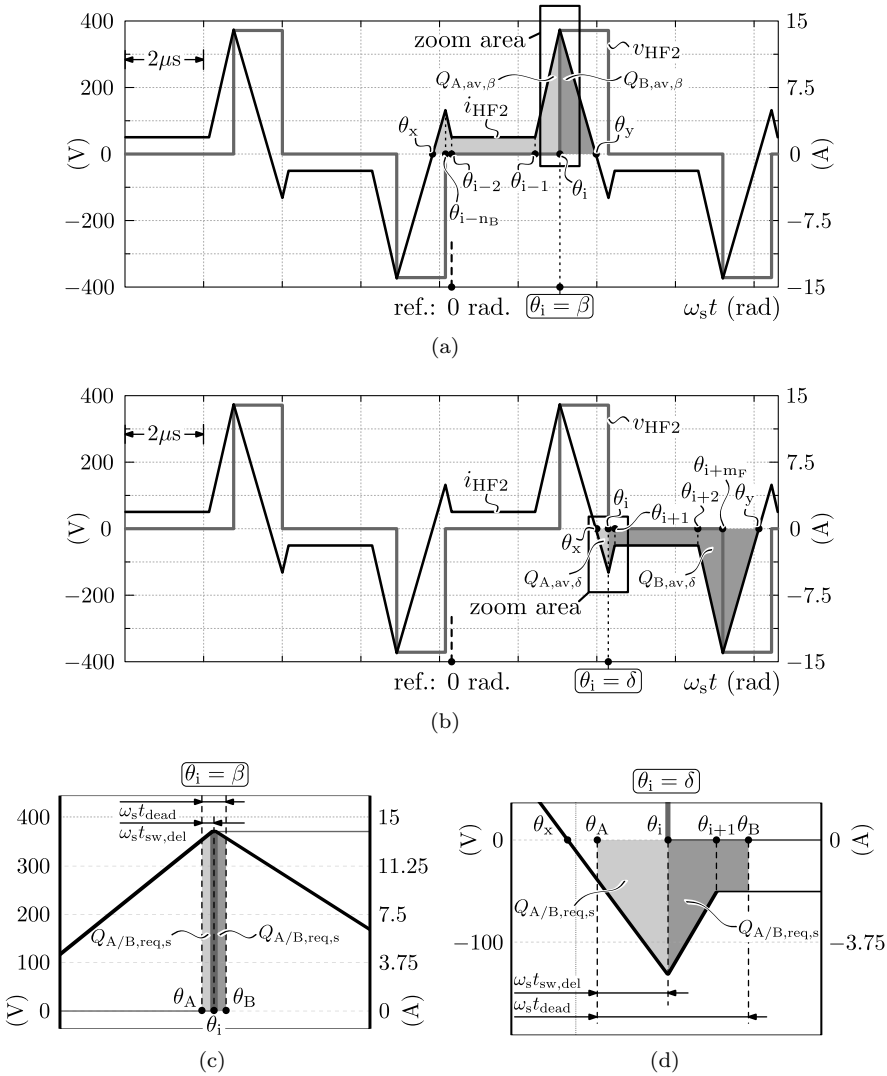


Figure 3.25: Secondary side bridge quantities (i.e. v_{HF2} and i_{HF2}) and the corresponding quantities that are involved in the proposed CDCB ZVS verification method, regarding the operating point depicted in Figure 3.23.

- $Q_{A,av,\alpha}$ and $Q_{B,av,\alpha}$: sub-figure 3.24(a);
- $Q_{A/B,req,p}$ (=$Q_{A/B,req}(v_{DC}{=}v_{DC1})$): sub-figure 3.24(c) (zoomed image);
- $n_B = 3$, $m_F = 0$.

- Switching instant $\theta_\mathrm{i} = \beta$:
  - $Q_{\mathrm{A,av},\beta}$ and $Q_{\mathrm{B,av},\beta}$: sub-figure 3.25(a);
  - $Q_{\mathrm{A/B,req,s}}$ (=$Q_{\mathrm{A/B,req}}(v_\mathrm{DC}{=}V_\mathrm{DC2})$): sub-figure 3.25(c) (zoomed image);
  - $n_\mathrm{B} = 3$, $m_\mathrm{F} = 0$.
- Switching instant $\theta_\mathrm{i} = \gamma$:
  - $Q_{\mathrm{A,av},\gamma}$ and $Q_{\mathrm{B,av},\gamma}$: sub-figure 3.24(b);
  - $Q_{\mathrm{A/B,req,p}}$ (=$Q_{\mathrm{A/B,req}}(v_\mathrm{DC}{=}v_\mathrm{DC1})$): sub-figure 3.24(d) (zoomed image);
  - $n_\mathrm{B} = 2$, $m_\mathrm{F} = 1$.
- Switching instant $\theta_\mathrm{i} = \delta$:
  - $Q_{\mathrm{A,av},\delta}$ and $Q_{\mathrm{B,av},\delta}$: sub-figure 3.25(b);
  - $Q_{\mathrm{A/B,req,s}}$ (=$Q_{\mathrm{A/B,req}}(v_\mathrm{DC}{=}V_\mathrm{DC2})$): sub-figure 3.25(d) (zoomed image);
  - $n_\mathrm{B} = 0$, $m_\mathrm{F} = 3$.

Furthermore also the switching delays and dead times, $t_{\mathrm{sw,del}}$ and t_dead, are shown for each switching instant.

Further Remarks

The implementation of the CDCB ZVS verification method outlined above relies on a capacitor model that reduces the expression for the voltage that appears across the parallel connected output capacitances (i.e. during the resonant transition, time interval t_2-t_4, cf. Figure 3.18) of the bridge leg switches to the most simple form. For example regarding bridge leg_{11} shown in Figure 3.17, the voltage v_C across $C_{\mathrm{leg}_{11}} = C_{11}||C_{12}$ during t_2-t_4 can be written as:

$$v_\mathrm{C}(q_\mathrm{C}) = \begin{cases} v_\mathrm{DC1} & \text{for } q_\mathrm{C} \geqslant (Q_{\mathrm{A/B,req,p}} = Q_{\mathrm{A/B,req}}(v_\mathrm{DC} = v_\mathrm{DC1})), \\ 0 & \text{for } q_\mathrm{C} < (Q_{\mathrm{A/B,req,p}} = Q_{\mathrm{A/B,req}}(v_\mathrm{DC} = v_\mathrm{DC1})). \end{cases} \tag{3.72}$$

Consequently, the HF AC-link currents are modeled as piecewise linear functions. Nevertheless, the error due to this linear approximation is small as, due to the strong nonlinearity of the leg capacitances, the energy transfer to and from the capacitances during commutation is almost fully concentrated in the time intervals where v_C remains quasi constant (i.e. at the beginning and at the end of the resonant interval t_2-t_4). Therefore, the momentaneous resonant transition has a negligible influence on the linear shape of the HF AC-link currents (see Figure 3.18) and the expressions to calculated the bridge currents (i_HF1 and i_HF2) are still valid. Quasi simultaneously with this work, a similar charge-based ZVS analysis for a triangular current mode (TCM) PFC rectifier has been proposed in [68], strengthening the validity.

3.4 Conclusion

This chapter discusses the steady-state operation of the single-stage (1-S) DAB AC–DC converter investigated in this work.

In the **first part** of this chapter, i.e. Section 3.1, the general operating principle of the 1-S DAB AC–DC converter is discussed. Based on the equivalent circuit model of the converter's AC input side, the operating range (i.e. with regard to the operating conditions specified in Table 1.1 of Section 1.3) of the full bridge - full bridge (FBFB) DAB DC–DC converter, which is the main building block of the DAB AC–DC converter, is derived. Furthermore, a control equation (i.e. equation (3.11)) for the (averaged) DAB input current $i_{\mathrm{DAB1}}(t)$ that is required in order to achieve a certain requested AC line current with given amplitude, power factor, and power flow direction, is presented. Both the DAB's operating range and the control equation for $i_{\mathrm{DAB1}}(t)$ include the reactive (capacitive) power consumption of the EMC input filter, requiring a certain reactive power transfer capability of the DAB. The obtained operating range is the starting point for the calculation procedures outlined in Chapter 4, regarding the derivation of full-operating-range ZVS modulation schemes for the DAB, and regarding the determination of the DAB's circuit level variables such as the transformer's turns ratio, the inductances values, and the applied switching frequency.

In the **second part** of this chapter, i.e. Section 3.2, the steady-state analysis of the FBFB DAB is presented, i.e. the fundamental mode equations are derived based on the lossless DAB model while referring to the general considerations regarding the traditional phase-shift modulation (PSM) given in Section 2.1. In order to tackle the disadvantages of the PSM, being a limited ZVS operating range and large RMS currents in the HF AC-link for most operating points when the DAB is operated with wide voltage ranges, here all possible degrees of freedom available for controlling the DAB's active bridges are exploited by considering dual-sided duty-cycle modulation (DSPWM) instead of PSM and by including all twelve switching modes that are possible with the (FBFB) DAB converter. This provides the highest possible degree of freedom regarding the search toward optimal, full-operating-range ZVS modulation schemes in Chapter 4. Furthermore, after reevaluation of the theoretical current-based (CB) ZVS conditions, 'commutation inductance(s)' are introduced which, using a simple calculation example, are shown to be an essential HF AC-link modification in order to achieve full-operating-range ZVS. The implication on the DAB model and on the mode equations of commutation inductance(s) is also detailed, while their effect on the ZVS operating range is further investigated in Chapter 4.

DAB's that are operated using modulation schemes which rely on the theoretical current-based (CB) ZVS conditions, in reality lead to hard-switching operation within the 'critical parts' of the calculated CB ZVS regions. This results in a

reduced conversion efficiency and, in all probability, leads to destruction of the semiconductor switching devices. In order to deal with this deficiency, in the **third part** of this chapter, i.e. Section 3.3, the ZVS behavior of the DAB is studied in detail and a novel current-dependent charge-based (CDCB) ZVS verification method is proposed. Thereby, the charge that is required to reset the parasitic output capacitances of the switches during commutation of the bridge legs, as well as the time dependency of the commutation currents, are taken into account. This results in a more accurate description of the DAB's ZVS conditions, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions. The presented CDCB ZVS verification method is experimentally verified and is translated into a set of constraints which are further used in Chapter 4 in order to derive full-operating-range CDCB ZVS modulation schemes for the DAB converter.

4

ZVS Modulation Schemes

For the determination of full-operating-range ZVS modulation schemes for the FBFB DAB DC–DC converter used in the investigated 1-S AC–DC architecture, in a first step an optimization procedure is proposed [86], which is based on a constrained numerical minimum search (i.e. a constrained nonlinear optimization). Closed-form solutions, such as presented in [92], for the optimal modulation parameters (i.e. $\mathbf{x_{opt}} = (\phi_{\mathrm{opt}}, \tau_{1,\mathrm{opt}}, \tau_{2,\mathrm{opt}}, f_{\mathrm{s,opt}})$) are not directly feasible because of the three following reasons:

1. *User definability of the cost function $f_{\mathrm{cost}}(\mathbf{x})$:* using a numerical optimization algorithm users can, according to their needs, predefine a cost function to be minimized. This allows to include all converter related losses, but also requirements concerning system volume, weight, control, EMC,... A closed-form solution for $\mathbf{x_{opt}}$ would require a fixed cost function.

2. *Discontinuity of the ZVS conditions:* the CDCB ZVS criterion proposed in Section 3.3 introduces discontinuities in the constraints functions for ZVS since the number of terms to be calculated in expressions (3.62)-(3.63) can vary, i.e. $0 \leqslant n_{\mathrm{B}}, m_{\mathrm{F}} \leqslant 3$. Moreover, additional boundaries conditions emerge as a result of the time-based constraints given by expressions (3.70)-(3.71).

3. *Increased complexity:* due the inclusion of commutation inductances L_{c1} and L_{c2} in the HF AC-link of the DAB (see Section 3.2.4), additional terms appear in the expressions for the primary and secondary side bridge currents i_{HF1} and i_{HF2}. Expressions (3.47) and (3.48) contain commutation currents $i_{L_{c1}}(t)$ and $i'_{L_{c2}}(t)$ which are not present in (2.22)-(2.23) when considering a traditional HF AC-link implementation (i.e. without commutation inductances). These terms substantially complicate the DAB mode equations. Moreover, the possible usage of a variable switching frequency adds a degree of freedom to modulate the active bridges of the DAB.

Below (i.e. Section 4.1), the numerical optimization procedure is outlined and demonstrated for several scenarios regarding the commutation inductances L_{c1} and L_{c2}, and regarding the applied ZVS conditions (i.e. the commonly used (theoretical) current-based (CB) ZVS conditions versus the current-dependent charge-based (CDCB) ZVS conditions proposed in Section 3.3.2 of this work), resulting in an optimal, full-operating-range CDCB ZVS modulation scheme for the DAB converter. Based on the results acquired from the numerical approach, in Section 4.2 a general, directly employable closed-form analytical solution for the calculation of the modulation parameters $\mathbf{x}$ which lead to full-operating-range CDCB ZVS operation is proposed, facilitating the direct application to a given (FBFB) DAB converter, provided that commutation inductors with appropriate inductance values are present in the HF AC-link. Additionally, in Section 4.3 a semi-analytical approach is presented as an alternative method to derive a full-operating-range CDCB ZVS modulation scheme for the DAB. Lastly, in Section 4.4 the three approaches are briefly compared while their impact on the losses in the different converter components and on the EMC input filter requirements is further investigated in Chapter 5. Furthermore, this chapter also provides guidelines for the effective selection of the circuit level variables $\mathbf{h} = (L, L_{c1}, L_{c2},$ and $n_1/n_2)$, and for the switching frequency pattern to be applied.

4.1 Numerical Approach

4.1.1 Constrained Nonlinear Optimization Procedure

Figure 4.1 summarizes the optimization procedure which starts from an initial set of circuit level variables $\mathbf{h} = \mathbf{h_{init}} = (L_{\text{init}}, L_{\text{c1,init}}, L_{\text{c2,init}},$ and $n_{1,\text{init}}/n_{2,\text{init}})$. Then it iterates through the complete DAB's operating range shown in Figure 3.6, passing variables $i_{\text{DAB1}}(\text{i},\text{j},\text{k})$, $v_{\text{DC1}}(\text{i},\text{j},\text{k})$, $V_{\text{DC2}}(\text{i},\text{j},\text{k})$, and circuit variables $\mathbf{h}$ to the core algorithm. Here, for each switching mode an optimizer is applied to find the minimum of a cost function $f_{\text{cost}}(\mathbf{x})$, while satisfying the constraint functions for that mode. The results ($\mathbf{x_{opt}}$, f_{cost}, and exit flag EF) from each mode optimizer are inputted to a selector for detecting which mode satisfies the constraint functions[1] and has the 'best value' for the cost function, outputting $\mathbf{x_{opt}}(\text{i},\text{j},\text{k})$, mode$(\text{i},\text{j},\text{k})$, and EF$(\text{i},\text{j},\text{k})$. After the complete operating range has been evaluated, the circuit level variables $\mathbf{h} = (L, L_{\text{c1}}, L_{\text{c2}},$ and $n_1/n_2)$ are varied in a top level iteration loop until full-operating-range CDCB ZVS is achieved, i.e. all exit flags EF$(\text{i},\text{j},\text{k})$ should be equal to one, and until the resulting modulation parameter trajectories are continuous (discontinuous steps in $\mathbf{x_{opt}}$ are highly undesirable), yielding the final, optimal CDCB ZVS modulation scheme.

Below, the information required for the implementation of the optimization algorithm depicted in Figure 4.1 is summarized, starting with the constraint functions and the cost function ($f_{\text{cost}}(\mathbf{x})$) to be minimized, followed by the considered switching frequency range and the initial values $\mathbf{h_{init}}$ of the circuit level variables $\mathbf{h}$. The expressions for the constraint functions and the cost function are mode dependent and are determined by the DAB's steady-state mode equations presented in Chapter 3 and Appendix A.

Constraint Functions— The constraint functions can be subdivided into,

- Functions describing the relation $i_{\text{DAB1}} = f(\mathbf{x})$. These are nonlinear and can be rewritten to subject the optimizer to the nonlinear equality $c_{\text{eq}}(\mathbf{x}) = 0$. The relations $i_{\text{DAB1}} = f(\mathbf{x})$ for all possible switching modes are given in Table A.4 of Appendix A;

- Functions describing the physical limitations on $\mathbf{x}$ (e.g. $0 \leqslant \tau_1 \leqslant \pi$ and $f_{\text{s,min}} \leqslant f_{\text{s}} \leqslant f_{\text{s,max}}$). This yields a set of lower bounds $\mathbf{l_b}$ and upper bounds $\mathbf{u_b}$ so that the solution of the optimization is always in the range $\mathbf{l_b} \leqslant \mathbf{x} \leqslant \mathbf{u_b}$;

- Functions describing the mode boundary conditions, assuring that the resulting modulation parameters $\mathbf{x_{opt}}$ for a certain switching mode do not result in a different mode of operation. The mode boundary conditions are

[1] The mode optimizer outputs an exit flag EF = 1 when the constraint functions for that mode are satisfied, and an exit flag EF = 0 when one or more constraints are violated.

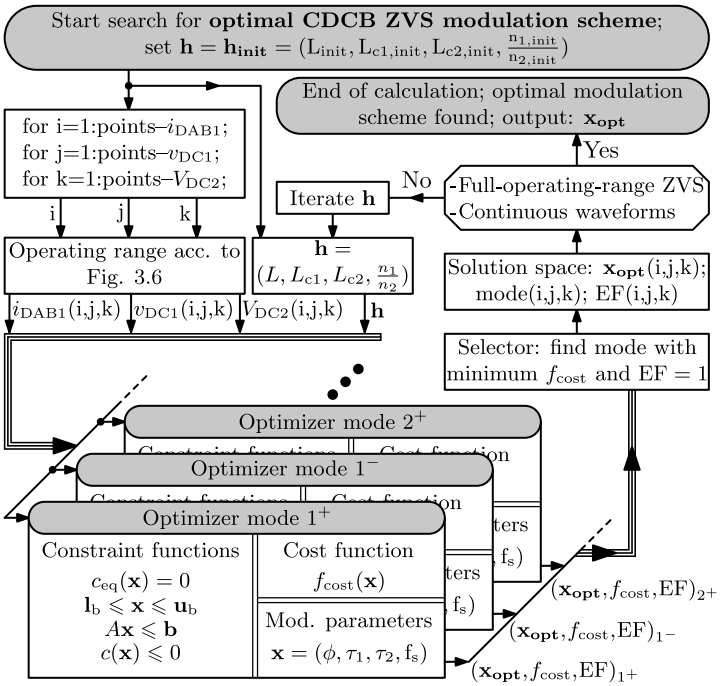


Figure 4.1: Procedure to determine an optimal CDCB ZVS modulation scheme and corresponding modulation parameters $\mathbf{x_{opt}} = (\phi_{\text{opt}}, \tau_{1,\text{opt}}, \tau_{2,\text{opt}}, f_{\text{s,opt}})$, using a constrained nonlinear (numerical) optimization algorithm.

given in Table A.1 of Appendix A and can be written as a set of linear inequalities, $A\mathbf{x} \leqslant \mathbf{b}$;

- Functions describing the ZVS boundaries according to the CDCB ZVS verification method proposed in Section 3.3, i.e. conform equations (3.62)-(3.71) and conform the calculation procedure depicted in Figure 3.20. These can be written as nonlinear inequalities $c(\mathbf{x}) \leqslant 0$. Note that the operation of the DAB is assumed/recommended to be, but not limited to ZVS. Alternatively hard-switching operation could be allowed and the corresponding switching losses could be included in the cost function.

The final numerical optimization procedure/algorithm is implemented in MATLAB$^{\text{TM}}$ using the 'fmincon'-function of the Optimization Toolbox$^{\text{TM}}$, and is verified using a Genetic Algorithm of the Global Optimization Toolbox$^{\text{TM}}$.

Cost Function $f_{\text{cost}}(\mathbf{x})$— For investigations of the DAB topology, most often converter losses are chosen for $f_{\text{cost}}(\mathbf{x})$, and the impact of HF losses caused by

current harmonics is neglected in a first design phase [92, 95]. According to [74, 92], under ZVS operation, the conduction losses of the semiconductor switching devices (MOSFETs) account for the biggest part ($> 50\%$) of the total converter losses, being verified in Chapter 5. For this reason, and similar to [92], only the conduction losses of the DAB's MOSFETs are considered for illustrating the proposed algorithm. These losses are proportional to $(I_{\mathrm{HF1}}^2 + I_{\mathrm{HF2}}^2)$ as the active bridges of the final DAB design consist of the same type of MOSFETs (see Section 5.1.1), yielding:

$$f_{\mathrm{cost}}(\mathbf{x}) = (I_{\mathrm{HF1}}^2 + I_{\mathrm{HF2}}^2), \tag{4.1}$$

where I_{HF1} and I_{HF2} are the local RMS values of the primary and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$:

$$I_{\mathrm{HF1,k}} = \sqrt{\frac{1}{T_{\mathrm{s}}} \int_{kT_{\mathrm{s}}}^{(k+1)T_{\mathrm{s}}} \left(i_{\mathrm{HF1}}(t)\right)^2 \mathrm{d}t}, \tag{4.2}$$

$$I_{\mathrm{HF2,k}} = \sqrt{\frac{1}{T_{\mathrm{s}}} \int_{kT_{\mathrm{s}}}^{(k+1)T_{\mathrm{s}}} \left(i_{\mathrm{HF2}}(t)\right)^2 \mathrm{d}t}. \tag{4.3}$$

For each switching mode of the DAB, analytical expressions for I_{HF1} and I_{HF2} can be derived by evaluating (4.2) and (4.3) using (3.47) and (3.48) in combination with the expressions for $i_{\mathrm{L}}(t_{\mathrm{i}})$, $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$, and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}})$ given in Tables A.3 and A.6, and in combination with the expressions for time instances t_{i} in Table A.2. This yields very large equations which are not given for the reason of brevity.

From the numerical optimization examples performed and discussed below (see Section 4.1.2), it is concluded that the DAB's ZVS constraint functions are the determining factor for the final values of the calculated modulation parameters $\mathbf{x_{opt}}$. Consequently, the cost function is of less importance in the determination of a ZVS modulation scheme. Moreover, the loss of ZVS operation would cause a tremendous increase of the switching losses and thus of the overall converter losses, overshadowing the discrepancy due to simplification of the cost function and justifying the selection of (4.1). Although not considered here, in Chapter 5 detailed loss (and volume) models are used in order to design and optimize the main converter components such as the inductors, the transformer, the heat sinks, the EMC filter, ... There HF losses caused by current harmonics, temperature dependencies, etc., are taken into account.

Switching Frequency Range— An upper switching frequency limit of $f_{\mathrm{s,max}} = 120$ kHz is selected to accommodate a compact converter design without causing excessive switching frequency related losses such as conduction losses due to high-frequency effects, core losses and switching losses. Moreover, thermal limitations apply at high switching frequencies, resulting in an increased total converter volume

[16]. $f_{\mathrm{s,max}}$ is chosen to stay well below these thermal limits. The choice of the lower switching frequency limit $f_{\mathrm{s,min}}$ is based on design considerations related to the differential-mode (DM) EMC input filter which is designed according to the procedure outlined in [106], and conform the guidelines given in [107] regarding filter damping, in order to comply with the CISPR 22 Class B standard [56] in the frequency range of 150 kHz – 30 MHz. A two-stage DM EMC filter topology with optimized (passive) damping (cf. Figure 3.2) is selected[2]. $f_{\mathrm{s,min}} = 75$ kHz, which is doubled towards the input port of the DAB converter, is chosen so that $2 \cdot f_{\mathrm{s,min}}$ is well beyond the maximum cut-off frequency, $f_{\mathrm{cutoff,DM2,max}}$, of the second DM filter stage, assuring enough margin to attenuate the lower HF harmonics of the input current. This selection is based on the assumption of an absolute maximum cut-off frequency of $f_{\mathrm{cutoff,DM2,max}} = 50$ kHz for the second DM filter stage, a maximum mains inductance of $L_{\mathrm{mains,max}} = 300$ μH, a cut-off frequency selection according[3] to $f_{\mathrm{cutoff,DM1}} = 0.05 \ldots 0.2 \cdot f_{\mathrm{cutoff,DM2}}$, and a minimum control bandwidth of $B_{w,\mathrm{min}} = 1.5$ kHz [106, 107]. Nevertheless, for an optimal DM filter design it might be advantageous to select $f_{\mathrm{s,min}}$ higher than 75 kHz, enabling higher filter cut-off frequencies and thus a lower filter volume [108]. Regarding the required filter attenuation, 150 kHz ($= 2 \cdot 75 = 2 \cdot f_{\mathrm{s,min}}$ kHz) is the worst possible choice for converters operated with constant switching frequency [106, 108]. However, this is not the case for the final switching frequency modulation applied for the DAB (see following sections), for which frequencies close to $f_{\mathrm{s,min}}$ mainly occur in the low current intervals of the AC line current $i_{\mathrm{AC}}(t)$. In these intervals the harmonic power of the instantaneous, HF switched, DAB input current i_1 is very low (the highest harmonic power occurs in the high current intervals of $i_{\mathrm{AC}}(t)$, and thus at higher switching frequencies). Moreover, modulation of the switching frequency results in a broader spectral distribution of the harmonic power and/or reduction of the amplitudes of individual harmonics. These effects lead to a lower required attenuation of the DM EMC filter and thus increased filter cut-off frequencies and decreased filter volume compared to converter operation with constant switching frequency. Furthermore, the allowance of a variable switching frequency in the optimization algorithm has the same effect as changing the inductance values. Therefore, investigations with other inductances are implicitly covered. The selected switching frequency range applied in the optimization algorithm depicted in Figure 4.1 is thus:

$$(f_{\mathrm{s,min}} = 75 \text{ kHz}) \leqslant f_{\mathrm{s}} \leqslant (f_{\mathrm{s,max}} = 120 \text{ kHz}). \tag{4.4}$$

Circuit Level Variables h— The following paragraphs provide general guidelines which can be used in order to select the initial values $\mathbf{h_{init}}$ of the circuit level variables $\mathbf{h}$ that are used in the optimization procedure depicted in Figure 4.1.

[2]The DM EMC input filter design is discussed in Section 5.4.

[3]Note that $f_{\mathrm{cutoff,DM1}}$ is the cut-off frequency of the first DM filter stage.

Transformer's turns ratio:
The turns ratio n_1/n_2 of the HF transformer needs to be determined such that $V'_{\mathrm{DC2,min}} > (\hat{v}_{\mathrm{DC1,max}} + 10\ \mathrm{V})$, with $V'_{\mathrm{DC2,min}} = n_1/n_2 \cdot V_{\mathrm{DC2,min}}$, is satisfied. Given the input voltage and output voltage range of the DAB converter, where $\hat{v}_{\mathrm{DC1,max}} = 358$ V (maximum DAB input voltage, see (3.3)) and $V_{\mathrm{DC2,min}} = 370$ V (minimum DAB output voltage, see (3.20)), this results in:

$$\frac{n_1}{n_2} > \left(\frac{\hat{v}_{\mathrm{DC1,max}} + 10}{V_{\mathrm{DC2,min}}} = 0.9946 \right). \tag{4.5}$$

The FBFB DAB can also be operated with other settings, e.g. allowing $V'_{\mathrm{DC2,min}} \leqslant \hat{v}_{\mathrm{DC1,max}}$ [92]. However, when being used in a 1-S AC–DC architecture, this would imply the occurrence of $d = 1$, since in this case the DAB is operated with variable input voltage v_{DC1} and thus with highly variable voltage conversion ratio d (remind that d is defined by (2.21)). This is a problem since in the vicinity of $d = 1$ it is quasi impossible to obtain ZVS in mode 5 operation (i.e. low power operation). The reason is that when d is close to one and when the DAB is operated with switching mode 5, the inductor volt-seconds product that is available to achieve the required zero crossing of the secondary side bridge current $i_{\mathrm{HF2}}(t)$ in time interval $t_\beta - t_\delta$ is too small[4]. Low inductance values for L_{c1} and/or L_{c2} would be required, leading to substantially increased RMS values of the HF AC-link currents. On the other hand, when n_1/n_2 is taken much higher than the result of (4.5), d becomes too high in the low voltage intervals of $v_{\mathrm{AC}}(t)$, again impeding ZVS as is illustrated in Section 4.1.2. The 10 V margin in (4.5) is based on the analysis of several optimization runs and turned out to be a good design guideline[5]. Based on this discussion, the recommended initial transformer turns ratio $n_{1,\mathrm{init}}/n_{2,\mathrm{init}}$ to be used in the optimization procedure is:

$$\frac{n_{1,\mathrm{init}}}{n_{2,\mathrm{init}}} = \left(\frac{\hat{v}_{\mathrm{DC1,max}} + 10}{V_{\mathrm{DC2,min}}} = 0.9946 \right), \tag{4.6}$$

which needs to be top-level iterated in the upward direction.

Equivalent inductance L:
According to (3.37), the maximum positive averaged input current[6] $i_{\mathrm{DAB1,max}}$ achievable with the FBFB DAB is obtained at $\tau_1 = \tau_2 = \pi$, $\phi = \pi/2$, mode 1^+, and needs to be higher than the maximum required averaged DAB input current according to (3.18):

[4]Note that according to the CDCB ZVS constraints given in Section 3.3, $i_{\mathrm{HF2}}(t_\beta)$ needs to be (at least) positive while $i_{\mathrm{HF2}}(t_\delta)$ needs to be (at least) negative.

[5]Note that the valley in V'_{DC2} due to the 100 Hz power component occurs 45° out of phase with $\hat{v}_{\mathrm{DC1}}$, inherently introducing an additional margin to the condition (4.5).

[6]The minimum negative averaged DAB input current $i_{\mathrm{DAB1}} = i_{\mathrm{DAB1,min}}$ is obtained at $\tau_1 = \tau_2 = \pi$, $\phi = -\pi/2$, mode 1^-, according to (3.38).

$$\left(i_{\mathrm{DAB1,max}} = \frac{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}{8 f_{\mathrm{s}} L} \right) \geqslant (\max(i_{\mathrm{DAB1,u}}) = 24 \text{ A}) \,. \tag{4.7}$$

An upper limit to the employed equivalent inductance value L can be calculated with (4.7) by setting: $f_{\mathrm{s}} = f_{\mathrm{s,max}} = 120$ kHz, $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V, and $n_1/n_2 = n_{1,\mathrm{init}}/n_{2,\mathrm{init}} = 0.9946$, yielding a recommended initial equivalent inductance value of

$$L_{\mathrm{init}} = L_{\mathrm{max}} = \frac{\frac{n_{1,\mathrm{init}}}{n_{2,\mathrm{init}}} \cdot V_{\mathrm{DC2,min}}}{8 f_{\mathrm{s,max}} i_{\mathrm{DAB1,max}}} = 15.97 \ \mu\mathrm{H}, \tag{4.8}$$

which needs to be top-level iterated in the downward direction. A good design guideline is to choose the final equivalent inductance value L in the range $L \approx (0.75 \ \ldots \ 0.85) \cdot L_{\mathrm{init}}$, i.e. leaving some margin to optimally modulate $\mathbf{x}$.

4.1.2 Results of the Numerical Approach

The search towards optimal modulation parameters $\mathbf{x_{opt}}$ and thus an optimal modulation scheme for the FBFB DAB using the optimization procedure outlined above is illustrated for different scenarios regarding commutation inductances L_{c1} and L_{c2}, and regarding the applied ZVS conditions (i.e. CB versus CDCB ZVS). In order to allow a clear comparison of the results for the different simulation examples, the values of the circuit variables L and n_1/n_2 are taken the same for each example. It are the final design values which are the result of an iteration performed during the design phase of the converter prototype system:

- $L = 13 \ \mu$H;
- $\frac{n_1}{n_2} = 1$.

The transformer turns ratio of $n_1/n_2 = 1$ is especially selected to enable efficient transformer construction with an equal number of primary and secondary side turns. For each scenario discussed below, $\mathbf{x_{opt}}$ is calculated for the whole DAB operating range according to Figure 3.6, applying 75 kHz $\leqslant f_{\mathrm{s}} \leqslant$ 120 kHz, $n_1/n_2 = 1$, and $L = 13 \ \mu$H. Remind that the optimization algorithm outputs the optimal modulation parameters $\mathbf{x_{opt}}$, i.e. optimal regarding minimization of the cost function $f_{\mathrm{cost}}(\mathbf{x})$ defined by (4.1), yielding the optimal ZVS modulation scheme. The other quantities shown in the graphs are calculated by applying $\mathbf{x_{opt}}$ in the analytical steady-state equations for the DAB given in Chapter 3 and Appendix A.

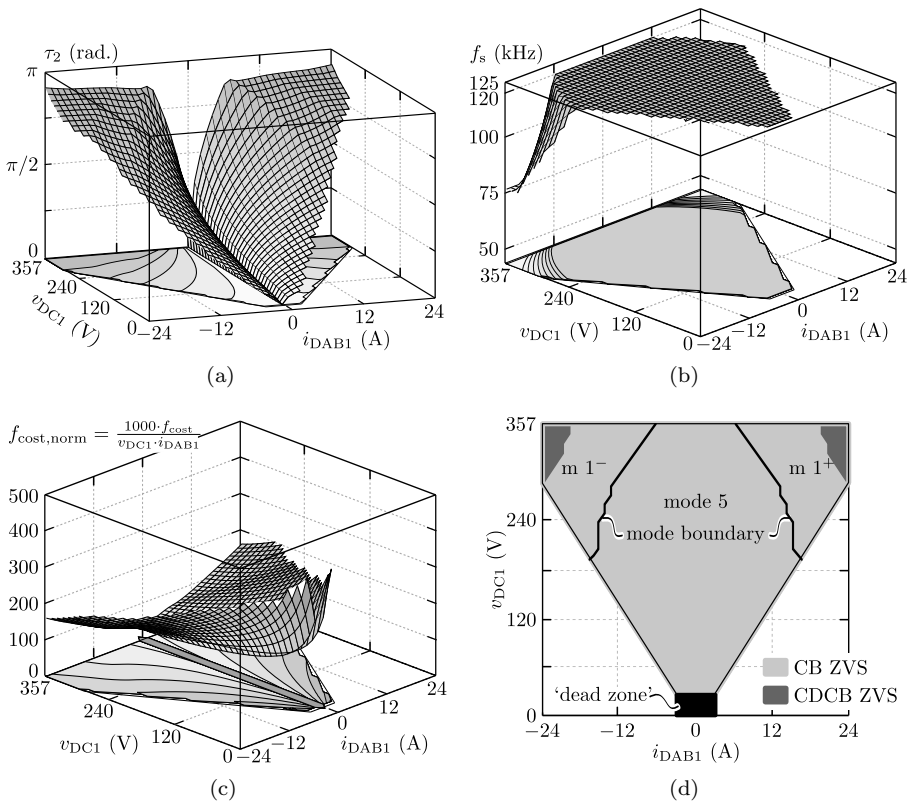


Figure 4.2: Results of the numerical search for optimal modulation schemes according to simulation example 1 (1st run): no use of commutation inductances ($L_{c1} = L_{c2} = \infty$). The optimizer is subjected to the CB ZVS conditions, using all possible switching modes. The output voltage for this example is $V_{DC2} = V_{DC2,nom} = 400$ V.

Simulation example 1, no commutation inductances (infinite L_{c1}, infinite L_{c2}):

This is the way the HF AC-link of the DAB converter is traditionally implemented: $L_{c1} = L_{c2} = \infty$, $i_{L_{c1}}(t) = i_{L_{c2}}(t) = 0$, $i_{HF1}(t) = i_L(t)$ (according to (3.47)), and $i_{HF2}(t) = n_1/n_2 \cdot i_L(t)$ (according to (3.48)). Consequently, no additional reactive currents are injected into the active bridges of the DAB in order to enhance ZVS.

1st run— Illustratively the optimization is performed a first time applying the generalized theoretical CB ZVS constraints defined by (3.44). Figure 4.2 depicts the results of the optimization (i.e. the resulting, optimal, modulation scheme),

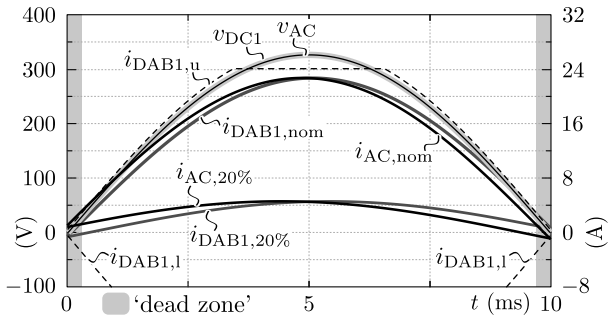


Figure 4.3: Averaged DAB input currents i_{DAB1}, required to achieve $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$; PF = 0.999 ($i_{\mathrm{DAB1,nom}}$-line) respectively $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$; PF = 0.983 ($i_{\mathrm{DAB1,20\%}}$-line). The nominal AC input voltage is applied: $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$.

calculated in the complete DAB's input voltage and input current operating range[7], and for an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. The optimal modulation parameters $\tau_{2,\mathrm{opt}}$ and $f_{\mathrm{s,opt}}$ are respectively shown in Figures 4.2(a) and 4.2(b) while, for brevity, $\tau_{1,\mathrm{opt}}$ and ϕ_{opt} are respectively shown in Figures B.1(a) and B.1(b) of Appendix B. Figure 4.2(d) depicts the calculated ZVS areas in the v_{DC1}-i_{DAB1} plane. It can be seen that the CB ZVS conditions are satisfied within the whole operating range but, however, the CDCB ZVS conditions that are calculated using the CDCB ZVS verification method proposed in Section 3.3.2 are mostly violated. This is a clear indication that modulation schemes which rely on the theoretical CB ZVS constraints, which do not take into account the resetting of the parasitic output capacitances of the switches during commutation, in reality lead to hard-switching operation within large regions of the DAB's operating range. Although all possible switching modes are included in the optimizer, switching mode 1 (applied in the high power regions of the v_{DC1}-i_{DAB1} plane) and switching mode 5 (applied in the low power regions of the v_{DC1}-i_{DAB1} plane) turn out to be most efficient (i.e. regarding the RMS value of the HF AC-link currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$) and are the only modes used to operate the DAB (see Figure 4.2(d)). The resulting, normalized, cost function is shown in Figure 4.2(c) while Figure 4.2(b) depicts the applied switching frequency pattern. From the latter it can be seen that the optimization algorithm keeps the switching frequency fixed at $f_{\mathrm{s}} = f_{\mathrm{s,max}} = 120$ kHz during the major part of the v_{DC1}-i_{DAB1} plane while only applying frequency modulation at high power levels. There a lowered f_{s} leads to the lowest cost function.

Figure 4.4 depicts the value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal

[7]Remind that the DAB's input voltage and input current operating range is defined by the two-quadrant (2-Q) voltage-current (i.e. v_{DC1}-i_{DAB1}) plane shown in Figure 3.5.

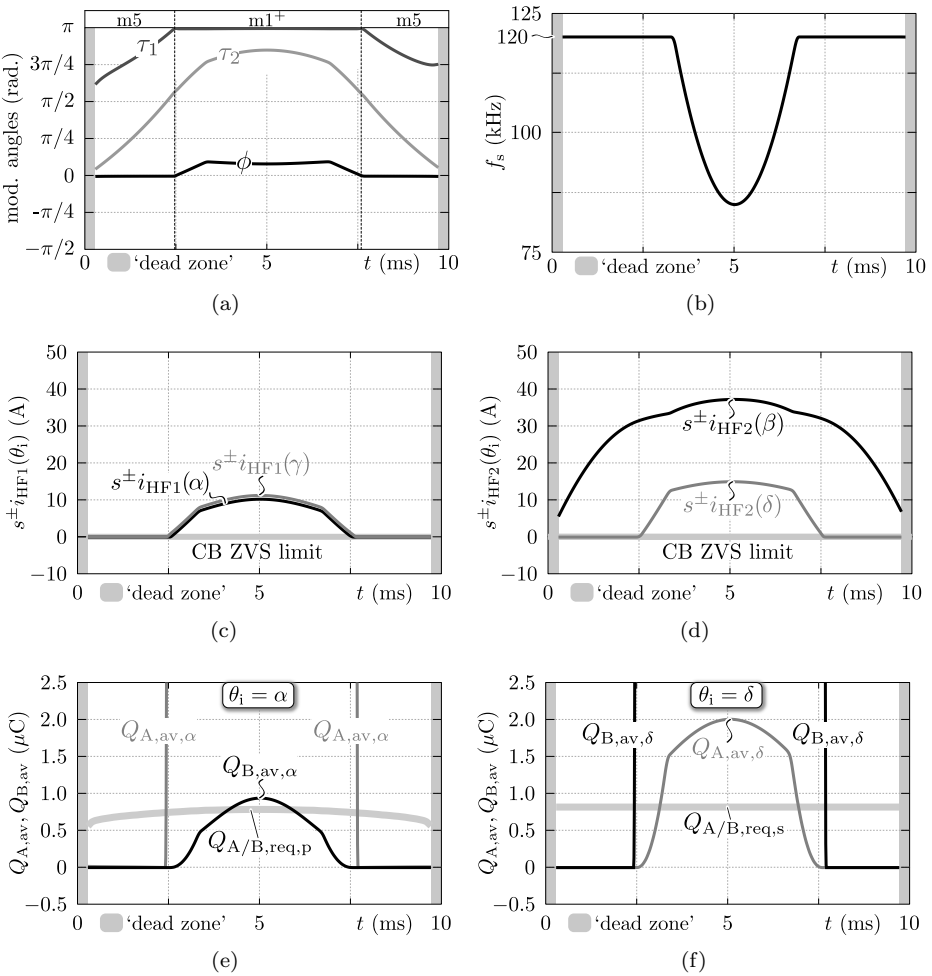


Figure 4.4: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V. The applied conditions are conform simulation example 1, 1st run (all switching modes included in the optimizer).

input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999, and an output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V. The values for i_{DAB1} (see Figure 4.3, $i_{DAB1,nom}$-line) that are applied during the half cycle in order to achieve the requested AC line current and PF are calculated using control equation (3.12).

The resulting trajectories of the modulation angles (i.e. $\tau_{1,\text{opt}}$, $\tau_{2,\text{opt}}$, and ϕ_{opt}) and the switching frequency $f_{\text{s,opt}}$ are respectively shown in Figures 4.4(a) and 4.4(b). Figures 4.4(c) and 4.4(d) show the values for $s^{\pm} \cdot i_{\text{HF1}}(\alpha)$ and $s^{\pm} \cdot i_{\text{HF1}}(\gamma)$, respectively $s^{\pm} \cdot i_{\text{HF2}}(\beta)$ and $s^{\pm} \cdot i_{\text{HF2}}(\delta)$. It can be seen that these values are bigger than zero during the complete half cycle which means that the generalized CB ZVS constraints defined by (3.44) are satisfied in the whole range. This, together with the fact that the solution for $\mathbf{x_{opt}}$ is similar to the one presented in [92], validates the proposed optimization algorithm. Also here it can be seen that only switching mode 1 (high power mode) and switching mode 5 (low power mode) are used to operate the DAB (see Figure 4.4(a)). Switching mode 5 is used at the beginning and at the end of the half cycle (low power intervals) while mode 1^+ is used in the middle of the half cycle (high power interval). Note that, in this simulation example, phase-shift angle ϕ equals zero during mode 5 operation. This is actually the boundary condition between mode 5 and mode 1^+. Moreover, the resulting modulation parameter trajectories are continuous, being highly desirable. Furthermore, from Figure 4.4(b) the frequency modulation at high power levels can be noticed.

Although CB ZVS is achieved, it can be seen from Figures 4.4(e) and 4.4(f) that, during the major part of the half cycle, the available commutation charges $Q_{\text{A,av},\alpha}$ and $Q_{\text{B,av},\alpha}$ for switching instant $\theta_{\text{i}} = \alpha$ (see Figure 4.4(e)) as well as the available commutation charges $Q_{\text{A,av},\delta}$ and $Q_{\text{B,av},\delta}$ for switching instant $\theta_{\text{i}} = \delta$ (see Figure 4.4(f)) are lower than respectively the minimum required commutation charge $Q_{\text{A/B,req,p}}$ (cf. (3.64), ZVS of the primary side active bridge) and the minimum required commutation charge $Q_{\text{A/B,req,s}}$ (cf. (3.65), ZVS of the secondary side active bridge). This once more confirms that modulation schemes that rely on the CB ZVS constraints, which do not take into account the resetting of the parasitic output capacitances of the switching devices, in reality lead to hard-switching operation. Note that for convenience only $Q_{\text{A,av}}$ and $Q_{\text{B,av}}$ for switching instances $\theta_{\text{i}} = \{\alpha \text{ and } \delta\}$ are shown, turning out to be the most critical for ZVS operation. $Q_{\text{A,av}}$ and $Q_{\text{B,av}}$ for switching instances $\theta_{\text{i}} = \{\beta \text{ and } \gamma\}$ are respectively shown in Figures B.2(a) and B.2(b) of Appendix B. There, during the major part of the half cycle, the available commutation charges $Q_{\text{A,av},\gamma}$ and $Q_{\text{B,av},\gamma}$ for switching instant $\theta_{\text{i}} = \gamma$ (see Figure B.2(b)) are lower than the minimum required commutation charge $Q_{\text{A/B,req,p}}$ (cf. (3.64), ZVS of the primary side active bridge). The available commutation charges $Q_{\text{A,av},\beta}$ and $Q_{\text{B,av},\beta}$ for switching instant $\theta_{\text{i}} = \beta$ (see Figure B.2(a)) on the other hand are higher than the minimum required commutation charge $Q_{\text{A/B,req,s}}$ (cf. (3.65), ZVS of the secondary side active bridge).

2^{nd} run— A second optimization is performed using the same conditions as in the first run, with the difference that now the optimizer is subjected to the CDCB ZVS constraints proposed in Section 3.3.2. These constraints take into account the resetting of the parasitic output capacitances of the switching devices.

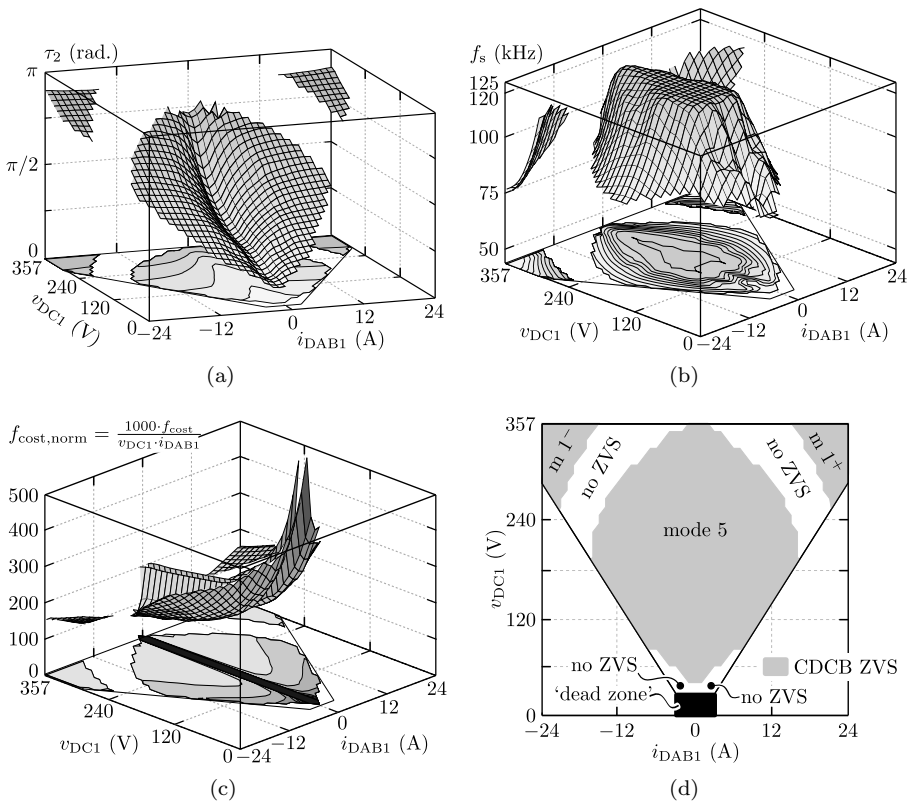


Figure 4.5: Results of the numerical search for optimal modulation schemes according to simulation example 1 (2^{nd} run): no use of commutation inductances ($L_{c1} = L_{c2} = \infty$). The optimizer is subjected to the CDCB ZVS conditions, using mode 1 and mode 5 (efficient switching modes) only. The output voltage for this example is $V_{DC2} = V_{DC2,nom} = 400$ V.

Figure 4.5 depicts the results of the optimization (i.e. the resulting, optimal, modulation scheme), calculated in the complete DAB's input voltage and input current operating range (i.e. the v_{DC1}-i_{DAB1}-plane shown in Figure 3.5) and for an output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V. Note that for the results shown in Figure 4.5 only the efficient switching modes 1 and 5 are applied in the optimizer. The optimal modulation parameters $\tau_{2,opt}$ and $f_{s,opt}$ are respectively shown in Figures 4.5(a) and 4.5(b) while, for brevity, $\tau_{1,opt}$ and ϕ_{opt} are respectively shown in Figures B.3(a) and B.3(b) of Appendix B. Figure 4.5(d) depicts the calculated ZVS areas in the v_{DC1}-i_{DAB1} plane. It can be seen that there are regions in the operating range (especially along the mode boundary and at low DAB input

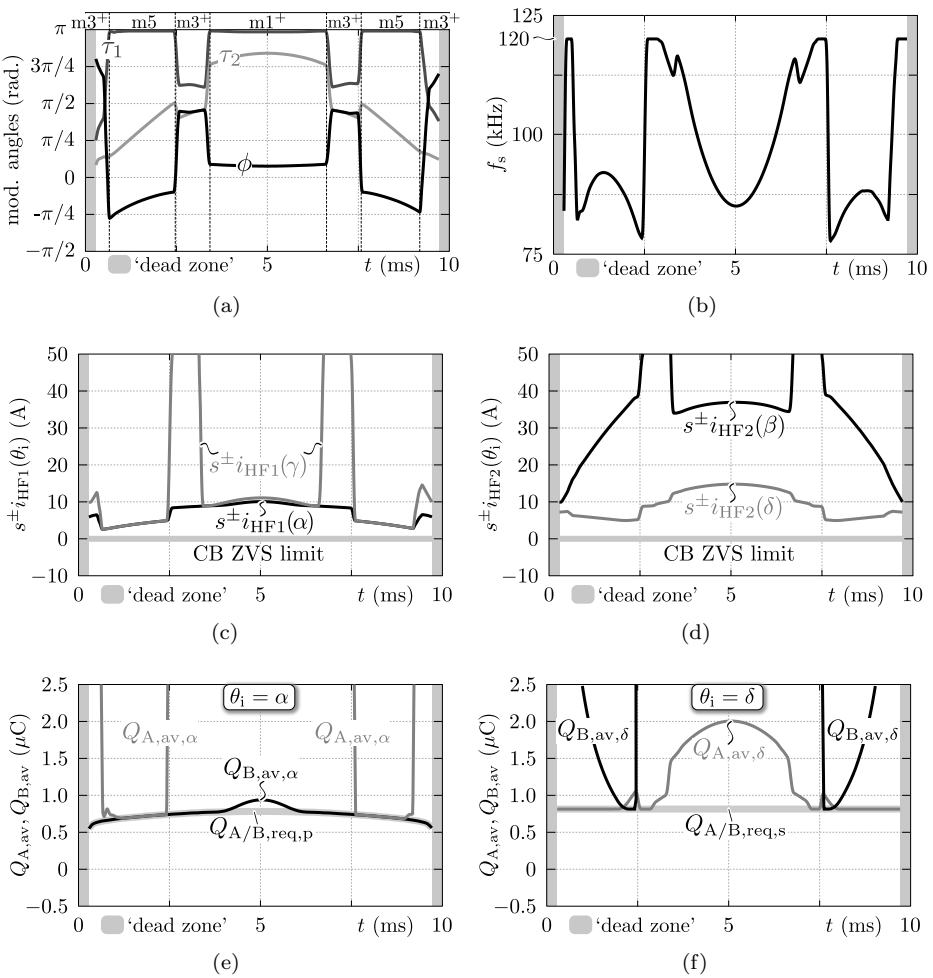


Figure 4.6: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$ (cf. Figure 4.3, $i_{\mathrm{DAB1,nom}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. The applied conditions are conform simulation example 1, 2^{st} run (all switching modes included in the optimizer).

voltage v_{DC1}) where the CDCB ZVS constraints cannot be satisfied. In these regions, the optimizer unsuccessfully tries to achieve ZVS by lowering the switching frequency (see Figure 4.5(b)). It can thus be concluded that efficient DAB operation (i.e. using switching modes 1 and 5 only) under full-operating-range CDCB ZVS

cannot be obtained. Therefore, the simulation was repeated applying all possible switching modes in the optimizer. Figure 4.6 depicts the results of this new simulation by means of the value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$, and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400\ \mathrm{V}$[8]. Now the regions where CDCB ZVS could not be achieved when only applying mode 1 and mode 5 are covered by switching mode 3 (see Figure 4.6(a)). From Figures 4.6(e) and 4.6(f) it can be seen that the available commutation charges $Q_{\mathrm{A,av},\alpha}$ and $Q_{\mathrm{B,av},\alpha}$ for switching instant $\theta_{\mathrm{i}} = \alpha$ (see Figure 4.6(e)) as well as the available commutation charges $Q_{\mathrm{A,av},\delta}$ and $Q_{\mathrm{B,av},\delta}$ for switching instant $\theta_{\mathrm{i}} = \delta$ (see Figure 4.6(f)) are higher than or equal to respectively the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ (cf. (3.64), ZVS of the primary side active bridge) and the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ (cf. (3.65), ZVS of the secondary side active bridge). The same goes for the available commutation charges $Q_{\mathrm{A,av},\gamma}$ and $Q_{\mathrm{B,av},\gamma}$ regarding switching instant $\theta_{\mathrm{i}} = \gamma$ (ZVS of the primary side active bridge) and the available commutation charges $Q_{\mathrm{A,av},\beta}$ and $Q_{\mathrm{B,av},\beta}$ regarding switching instant $\theta_{\mathrm{i}} = \beta$ (ZVS of the secondary side active bridge), which are respectively shown in Figures B.4(b) and B.4(a) of Appendix B. This means that now CDCB ZVS is guaranteed. However, as can be seen from Figures 4.6(a) and 4.6(b), the resulting trajectories of the modulation angles (i.e. $\tau_{1,\mathrm{opt}}$, $\tau_{2,\mathrm{opt}}$, and ϕ_{opt}) and the switching frequency $f_{\mathrm{s,opt}}$ are discontinuous, being highly undesirable. Moreover, during mode 3 operation the HF AC-link currents i_{HF1} and i_{HF2} show strongly increased values (see Figures 4.6(c) and 4.6(d)), leading to inefficiency converter operation due to increased conduction losses (i.e. the RMS values of the HF AC-link currents and thus also of the bridge currents are unacceptably high). Therefore it can be stated that it is impossible to achieve 'efficient' (i.e. using switching modes 1 and 5 only) full-operating-range CDCB ZVS with the traditional HF AC-link implementation of the DAB (i.e. without commutation inductances L_{c1} and L_{c2}). The regions of the operating range that are most problematic are those where the primary side referred voltage conversion ratio d, defined by (2.21), is substantially higher than one, i.e. at low DAB input voltage v_{DC1}, as well as the regions along the boundary between the low power switching mode (i.e. mode 5) and the high power switching mode (i.e. mode 1).

Simulation example 2, primary and secondary side commutation inductances (finite L_{c1}, finite L_{c2}):

Commutation inductances L_{c1} and L_{c2} are introduced in Section 3.2.4 as a HF AC-link modification (cf. Figures 3.7 and 3.12) that is essential in order to overcome the limitation of the traditional HF AC-link implementation of the DAB which, as

[8]Remind that the values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{\mathrm{DAB1,nom}}$-line).

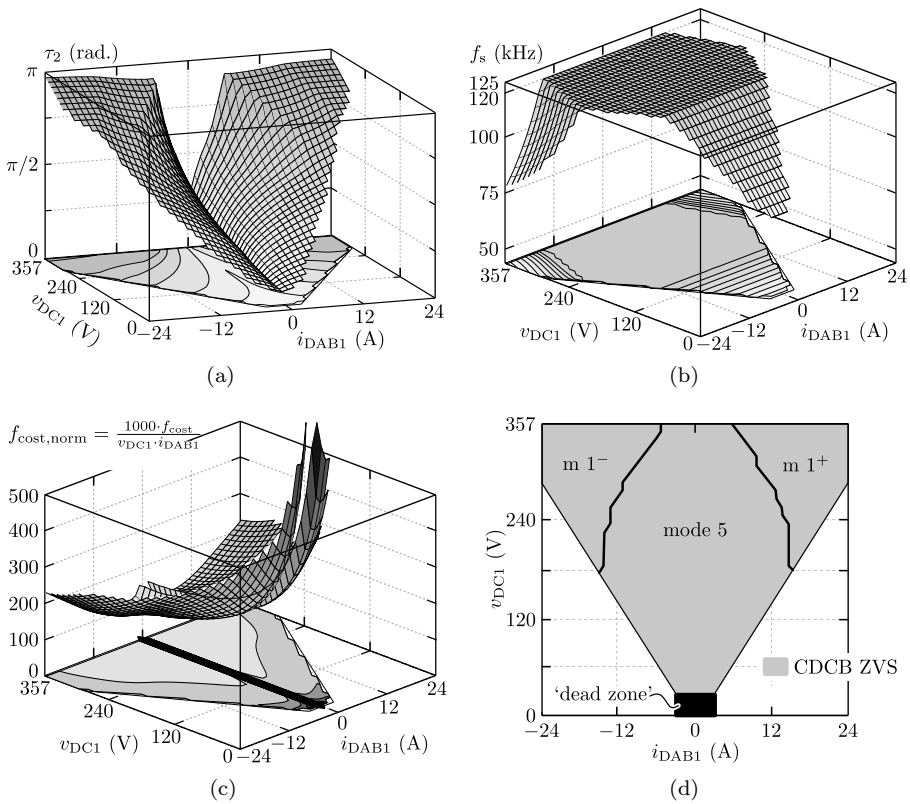


Figure 4.7: Results of the numerical search for optimal modulation schemes according to simulation example 2: primary and secondary side commutation inductances included ($L_{c1} = L_{c2} = 62.1$ μH). The optimizer is subjected to the CDCB ZVS conditions, using all possible switching modes. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V.

shown above, does not allow to achieve 'efficient' (i.e. using switching modes 1 and 5 only) full-operating-range CDCB ZVS. To prove the effectiveness of commutation inductances, in this simulation example a HF AC-link implementation with finite L_{c1} and L_{c2} is considered. Thereby small reactive currents $i_{L_{c1}}(t)$ and $i_{L_{c2}}(t)$ are injected into the respective active bridges, always having a beneficial contribution to the ZVS conditions. Now the respective bridge currents are calculated with $i_{HF1}(t) = i_L(t) + i_{L_{c1}}(t)$ (according to (3.47)), and $i_{HF2}(t) = n_1/n_2 \cdot i_L(t) - i_{L_{c2}}(t)$ (according to (3.48)).

The numerical optimization is once more performed, applying the CDCB ZVS constraints according to Section 3.3.2, including all possible switching modes, and

assuming equal commutation inductances (i.e. $L_{c1} = L_{c2}$). The values L_{c1} and L_{c2} are top-level iterated, i.e. starting from high values and iterating in the downward direction, until 'efficient' (i.e. using switching modes 1 and 5 only) full-operating-range CDCB ZVS is obtained and until the resulting modulation parameter trajectories are continuous. Figure 4.7 depicts the results of the optimization (i.e. the resulting, optimal, modulation scheme), calculated in the complete DAB's v_{DC1}-i_{DAB1}-plane shown in Figure 3.5 and regarding the worst case output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The optimal modulation parameters $\tau_{2,opt}$ and $f_{s,opt}$ are respectively shown in Figures 4.7(a) and 4.7(b) while, for brevity, $\tau_{1,opt}$ and ϕ_{opt} are respectively shown in Figures B.5(a) and B.5(b) of Appendix B. Figure 4.7(d) depicts the calculated ZVS areas in the v_{DC1}-i_{DAB1} plane. It can be seen that the CDCB ZVS conditions are satisfied within the whole operating range while only switching mode 1 (applied in the high power regions of the v_{DC1}-i_{DAB1} plane) and switching mode 5 (applied in the low power regions of the v_{DC1}-i_{DAB1} plane) are used. By adding commutation inductances to the HF AC-link, 'efficient' (i.e. using switching modes 1 and 5 only) full-operating-range CDCB ZVS is achieved. The highest values for the commutation inductances which lead to full-operating-range ZVS are found to be $L_{c1} = L_{c2} = 62.1$ μH, being selected as the final design values for the DAB. The resulting, normalized, cost function is shown in Figure 4.7(c). It should be noted that the calculated switching frequency pattern depicted in Figure 4.7(b) is a combination of $f_{s,opt}$ which is outputted by the optimization algorithm and of a predefined frequency pattern $f_{s,pre}$ according to:

$$f_s = \begin{cases} f_{s,opt} & \text{if } v_{DC1} \geqslant 150 \text{ V}, \\ f_{s,pre} & \text{if } v_{DC1} < 150 \text{ V}. \end{cases} \tag{4.9}$$

When defining $v_{DC1,fs}$ as the DAB input voltage at the boundary between the $f_{s,opt}$ and the $f_{s,pre}$ frequency pattern (i.e. $v_{DC1,fs} = 150$ V, acc. to (4.9)), and $v_{DC1,DABoff}$ as the DAB input voltage below which the active bridges of the DAB are turned off[9] (i.e. $v_{DC1,DABoff} = 30$ V), $f_{s,pre}$ is defined as:

$$\begin{aligned} f_{s,pre} &= f_{s,min} + (v_{DC1} - v_{DC1,DABoff}) \cdot \frac{f_{s,max} - f_{s,min}}{v_{DC1,fs} - v_{DC1,DABoff}} \\ &= 75000 + 375 \cdot (v_{DC1} - 30) \text{ Hz}. \end{aligned} \tag{4.10}$$

In case no predefined switching frequency pattern $f_{s,pre}$ is used in the low voltage intervals of v_{DC1}, f_s is completely determined by the optimizer (i.e. in the whole operating range). However, as can be seen from Figure 4.8 this results in a highly distorted f_s-pattern at low v_{DC1}, where the optimizer cannot find a homogeneous

[9]Remind that around the zero crossing of the AC line voltage (i.e. -30 V$\leqslant v_{AC} \leqslant 30$ V) the bridges of the DAB are set inactive ('dead zone') as power conversion under ZVS conditions is quasi impossible within this voltage interval.

solution for the optimization problem. This is because in this region CDCB is very hard to obtain and (optimal) solutions $\mathbf{x_{opt}}$ strongly differ from point to point, unavoidably leading to discontinuous steps in the modulation angles $\tau_{1,\mathrm{opt}}$, $\tau_{2,\mathrm{opt}}$, and ϕ_{opt}. It is clear that at low v_{DC1} the switching frequency has to be lowered in order to achieve full-operating-range ZVS, but at this point it is not possible to exactly define how. Therefore it is recommended to apply (4.9) or a similar expression which might be freely defined by the user. The final values for L_{c1} and L_{c2} then depend on the selection of $f_{\mathrm{s,pre}}$. From the resulting switching frequency pattern in Figure 4.7(b) it can be seen that the optimization algorithm also applies frequency modulation at high power levels. There a lowered f_{s} leads to the lowest cost function.

Figure 4.9 depicts the value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$, and the worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370\ \mathrm{V}$[10]. From Figures 4.9(e) and 4.9(f) it can be seen that the available commutation charges $Q_{\mathrm{A,av},\alpha}$ and $Q_{\mathrm{B,av},\alpha}$ for switching instant $\theta_{\mathrm{i}} = \alpha$ (see Figure 4.9(e)) as well as the available commutation charges $Q_{\mathrm{A,av},\delta}$ and $Q_{\mathrm{B,av},\delta}$ for switching instant $\theta_{\mathrm{i}} = \delta$ (see Figure 4.9(f)) are higher than or equal to respectively the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ (cf. (3.64), ZVS of the primary side active bridge) and the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ (cf. (3.65), ZVS of the secondary side active bridge). The same goes for the available commutation charges $Q_{\mathrm{A,av},\gamma}$ and $Q_{\mathrm{B,av},\gamma}$ regarding switching instant $\theta_{\mathrm{i}} = \gamma$ (ZVS of the primary side active bridge)

[10]Remind that the values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{\mathrm{DAB1,nom}}$-line).

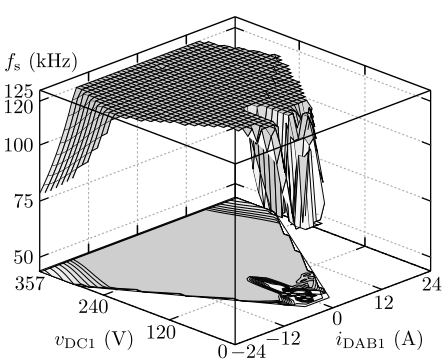


Figure 4.8: Resulting switching frequency pattern regarding simulation example 2 in case no predefined switching frequency $f_{\mathrm{s,pre}}$ is used in the low voltage intervals of v_{DC1}.

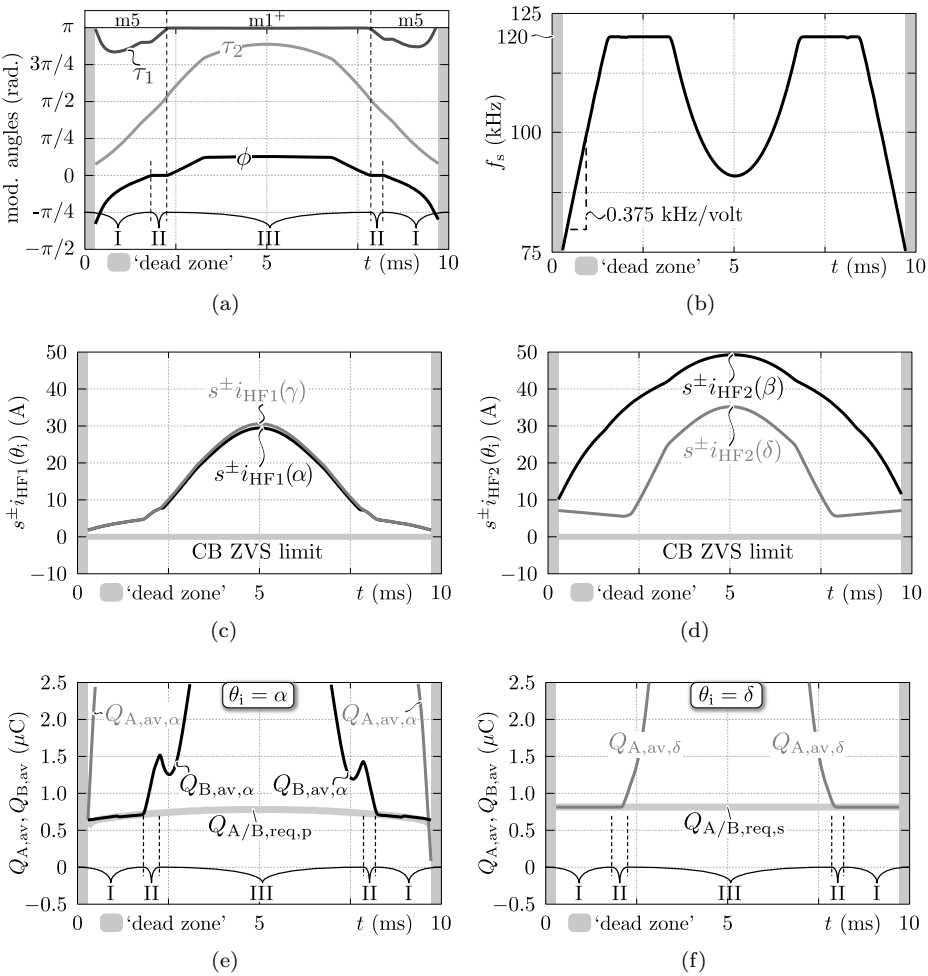


Figure 4.9: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$ (cf. Figure 4.3, $i_{\mathrm{DAB1,nom}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V. The applied conditions are conform simulation example 2 (all switching modes included in the optimizer).

and the available commutation charges $Q_{\mathrm{A,av},\beta}$ and $Q_{\mathrm{B,av},\beta}$ regarding switching instant $\theta_{\mathrm{i}} = \beta$ (ZVS of the secondary side active bridge), which are respectively shown in Figures B.6(b) and B.6(a) of Appendix B. This means that CDCB ZVS is guaranteed. Moreover, as can be seen from Figures 4.9(a) and 4.9(b), the resulting

trajectories of the modulation angles (i.e. $\tau_{1,\mathrm{opt}}$, $\tau_{2,\mathrm{opt}}$, and ϕ_{opt}) and the switching frequency $f_{\mathrm{s,opt}}$ are continuous, being highly desirable. Furthermore, only efficient modes 1 and 5 are used. Figure B.7 in Appendix B depicts the value trajectories calculated under the same conditions (nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$ and worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V) but under reduced input power: $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$ and PF = 0.983. Again, full-operating-range CDCB ZVS involving smooth modulation parameter trajectories is obtained[11]. Remarkable is the fact that in order to achieve CDCB ZVS (i.e. enough charge needs to be available in the respective bridge currents before and after the respective switching instances), currents $s^{\pm} \cdot i_{\mathrm{HF1}}(\theta_{\mathrm{i}})$ and $s^{\pm} \cdot i_{\mathrm{HF2}}(\theta_{\mathrm{i}})$ are mostly higher than 5 to 10 A, as inter alia can be seen in Figures 4.9(c) and 4.9(d). This once more confirms that the theoretical CB ZVS conditions defined by (3.44) are far from sufficient. Note also that the intervals in Figures 4.9 (i.e. intervals 'I', 'II', and 'III') and B.7 (i.e. intervals 'I' and 'II') are used in the next section in order to derive a closed-form analytical solution for the calculation of the modulation parameters $\mathbf{x}$.

Regarding the numerical approach outlined in this section, the modulation scheme obtained from simulation example 2 is the final, optimal, full-operating-range CDCB ZVS modulation scheme used in further chapters/discussions. It should be noted that similar results can be obtained by using only one commutation inductance (i.e. finite L_{c1}, infinite L_{c2} or infinite L_{c1}, finite L_{c2}), which however yield more unbalanced HF AC-link current values. The case with infinite L_{c1} and finite L_{c2} for example would require $L_{\mathrm{c2}} = 29.7\ \mu\mathrm{H}$.

[11] Note that here only efficient switching mode 5 is used due to the low required input power. The values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{\mathrm{DAB1,20\%}}$-line).

4.2 Analytical Approach

Based on the optimal, full-operating-range CDCB ZVS modulation scheme for the DAB obtained from the numerical approach outlined in the previous section, in this section a general, directly employable closed-form analytical solution for the calculation of the modulation parameters $\mathbf{x} = (\phi, \tau_1, \tau_2, f_\mathrm{s})$ which lead to full-operating-range CDCB ZVS operation is proposed. This facilitates the direct application to a given (FBFB) DAB converter, provided that commutation inductors with appropriate inductance value are present in the HF AC-link. The presented expressions for $\mathbf{x}$ are the result of the identification of distinct intervals in the value trajectories depicted in Figure 4.9 and in Figure B.7 (see Appendix B). These value trajectories are obtained using the final (optimal), full-operating-range CDCB ZVS modulation scheme according to the numerical approach outlined in Section 4.1, i.e. conform simulation example 2. Note that in order to solve the equation systems established in this section, a predefined switching frequency or switching frequency pattern is required due to the high number of independent variables. Referring to the switching frequency pattern used in Section 4.1, which according to (4.9) and (4.10) is a combination of $f_\mathrm{s,opt}$ (used at high v_DC1) outputted by the optimization algorithm and of a predefined frequency pattern $f_\mathrm{s,pre}$ (used at low v_DC1), here a similar pattern is applied. The difference is that now at high v_DC1, instead of $f_\mathrm{s,opt}$ (optimizer), a fixed switching frequency that is equal to $f_\mathrm{s,max}$ is used:

$$f_\mathrm{s} = \begin{cases} f_\mathrm{s,max} = 120 \text{ kHz} & \text{if } v_\mathrm{DC1} \geqslant 150 \text{ V}, \\ f_\mathrm{s,pre} \text{ (acc. to (4.10))} & \text{if } v_\mathrm{DC1} < 150 \text{ V}. \end{cases} \tag{4.11}$$

The reason of fixing f_s to $f_\mathrm{s,max}$ at high v_DC1 is that no optimization algorithm is involved in the analytical approach and thus $f_\mathrm{s,opt}$ is not anymore available. Due to the application of a predefined switching frequency pattern, the analytical approach presented in this section provides closed-form solutions for the modulation angles τ_1, τ_2, and ϕ only.

4.2.1 Closed-Form Solution for the Modulation Parameters

Below, it is explained in four steps how, given a predefined switching frequency pattern, the closed-form solution for the calculation of modulation angles τ_1, τ_2, and ϕ, which lead to full-operating-range CDCB ZVS operation of the DAB is derived.

Step 1: Identification of Distinct Trajectory Intervals

In Figure 4.9, which is calculated using the numerical approach (see Section 4.1), three distinct intervals can be identified in the resulting value trajectories. Note that the figure is derived for the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$ (cf. Figure 4.3, $i_{\mathrm{DAB1,nom}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V. The power flow is positive, i.e. switching modes 1^+ and 5 are used in the different trajectory intervals.

Interval I (mode 5)— It can be seen from Figure 4.9(e) that within interval I the commutation charge $Q_{\mathrm{B,av},\alpha}$ that is available in the bridge current (i.e. regarding the primary side bridge current i_{HF1}) after switching instant $\theta_{\mathrm{i}} = \alpha$, is equal to the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ for the primary side active bridge (i.e. cf. (3.64)). The same goes for the commutation charge[12] $Q_{\mathrm{A,av},\delta}$ that is available in the bridge current (i.e. regarding the secondary side bridge current i_{HF2}) before switching instant $\theta_{\mathrm{i}} = \delta$ which, as can be seen from Figure 4.9(f), is equal to the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ for the secondary side active bridge. Consequently, the conditions for interval I are:

$$Q_{\mathrm{B,av},\alpha} = Q_{\mathrm{A/B,req,p}}\ \text{(cf. Figure 4.9(e))}, \tag{4.12}$$

$$Q_{\mathrm{A,av},\delta} = Q_{\mathrm{A/B,req,s}}\ \text{(cf. Figure 4.9(f))}. \tag{4.13}$$

Interval II (mode 5)— Within interval II the commutation charge $Q_{\mathrm{B,av},\alpha}$ that is available in the bridge current after switching instant $\theta_{\mathrm{i}} = \alpha$, is increased (enhanced CDCB ZVS) above the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ for the primary side active bridge. The commutation charge $Q_{\mathrm{A,av},\delta}$ that is available in the bridge current before switching instant $\theta_{\mathrm{i}} = \delta$, is still equal to the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ for the secondary side active bridge. Moreover, it can be seen from Figure 4.9(a) that within interval II the phase-shift angle ϕ equals zero. Consequently, the conditions for interval II are:

$$\phi = 0\ \text{(cf. Figure 4.9(a))}, \tag{4.14}$$

$$Q_{\mathrm{A,av},\delta} = Q_{\mathrm{A/B,req,s}}\ \text{(cf. Figure 4.9(f))}. \tag{4.15}$$

Since ϕ equals zero, this is actually the boundary condition between mode 5 and mode 1^+ DAB operation but, for the reason of consistency, it is still referred to as mode 5 operation.

[12] It should be reminded that commutation charges $Q_{\mathrm{A,av},\alpha}$ and $Q_{\mathrm{B,av},\delta}$ are calculated using respectively the backward integration according to (3.62) and the forward integration according to (3.63), as extensively explained in Section 3.3.2.

Interval III (mode 1^+)— Within interval III the commutation charge $Q_{\mathrm{B,av},\alpha}$ that is available in the bridge current after switching instant $\theta_\mathrm{i} = \alpha$, as well as the commutation charge $Q_{\mathrm{A,av},\delta}$ that is available in the bridge current before switching instant $\theta_\mathrm{i} = \delta$, are increased (enhanced CDCB ZVS) above the minimum required commutation charges, i.e. $Q_{\mathrm{A/B,req,p}}$ respectively $Q_{\mathrm{A/B,req,s}}$. Moreover, it can be seen from Figure 4.9(a) that within interval III the pulse-width modulation angle τ_1 equals π. Consequently, the condition for interval III is:

$$\tau_1 = \pi \text{ (cf. Figure 4.9(a))}. \tag{4.16}$$

Similar intervals can be identified in Figure B.7 of Appendix B which shows the resulting value trajectories calculated using the numerical approach (see Section 4.1) at reduced input power. The figure is derived for the nominal AC input voltage of $V_\mathrm{AC} = 230\ \mathrm{V_{rms}}$, an input current of $I_\mathrm{AC,P} = 0.2 \cdot I_\mathrm{AC,P,nom} = 3.2\ \mathrm{A_{rms}}$, a power factor of PF = 0.983 (cf. Figure 4.3, $i_{\mathrm{DAB1,20\%}}$-line), and an output voltage of $V_\mathrm{DC2} = V_\mathrm{DC2,min} = 370$ V. Note that in Figure B.7 interval III does not exist since only the low power switching mode 5 is used due to the reduced input power.

Step 2: Derivation of Expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$

In order to reproduce the intervals identified above using closed-form solutions for modulation angles τ_1, τ_2, and ϕ, first expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ need to be found. These expressions can then be used in 'interval conditions' (4.12) and (4.13) for interval I, and in 'interval condition' (4.15) for interval II. In particular, the expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ need to be found for mode 5 operation as, conform Figure 4.9 and B.7, this is the DAB operating mode used in intervals I and II. Doing so, they can be combined with expression (3.40) for the mode 5 phase-shift angle ϕ, enabling the establishment of equation systems that can be analytically solved towards τ_1, τ_2, and ϕ (see step 3).

Below the expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$, regarding mode 5 operation, are derived using Figure 4.10, which depicts the primary side (see Figure 4.10(a)) and the secondary side (see Figure 4.10(b)) bridge currents (i_HF1 and i_HF2) that correspond with the example in Figure 3.23. This example relates to a random mode 5 operating point and is used in Section 3.3.2 to demonstrate the CDCB ZVS verification method. According to Figure 4.10, $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ are determined by:

$$Q_{\mathrm{B,av},\alpha} = \frac{1}{2} \cdot \frac{\theta_\mathrm{y} - \theta_\mathrm{i}}{\omega_\mathrm{s}} \cdot (-i_\mathrm{HF1}(\alpha)) = \frac{1}{2} \cdot \frac{\theta_\mathrm{y} - \alpha}{\omega_\mathrm{s}} \cdot (-i_\mathrm{HF1}(\alpha)), \tag{4.17}$$

$$Q_{\mathrm{A,av},\delta} = \frac{1}{2} \cdot \frac{\theta_\mathrm{i} - \theta_\mathrm{x}}{\omega_\mathrm{s}} \cdot (-i_\mathrm{HF2}(\delta)) = \frac{1}{2} \cdot \frac{\delta - \theta_\mathrm{x}}{\omega_\mathrm{s}} \cdot (-i_\mathrm{HF2}(\delta)), \tag{4.18}$$

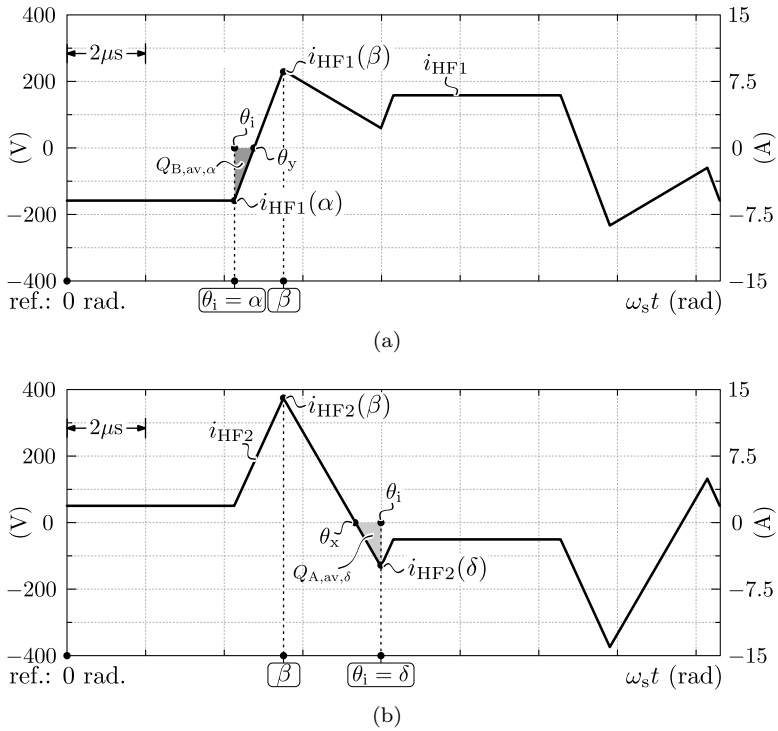


Figure 4.10: Primary side and secondary side bridge currents (i.e. i_{HF1}: sub-figure (a) and i_{HF2}: sub-figure (b)) that correspond with the example in Figure 3.23 of Section 3.3, regarding a random mode 5 operating point of the DAB. The considered operating point is derived using $v_{DC1} = 250$ V, $V_{DC2} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{c1} = L_{c2} = 62.1$ μH, $f_s = 120$ kHz, $\phi = -0.12$ rad., $\tau_1 = 1.53$ rad., and $\tau_2 = 0.94$ rad.

where θ_x and θ_y can be found by applying simple trigonometrical formulas. For θ_y this yields:

$$\frac{\theta_y - \alpha}{-i_{HF1}(\alpha)} = \frac{\beta - \alpha}{i_{HF1}(\beta) + (-i_{HF1}(\alpha))} \tag{4.19}$$

$$\rightarrow \ \theta_y = \alpha + \frac{-i_{HF1}(\alpha) \cdot (\beta - \alpha)}{i_{HF1}(\beta) - i_{HF1}(\alpha)}. \tag{4.20}$$

For θ_x this yields:

$$\frac{\delta - \theta_{\mathrm{x}}}{-i_{\mathrm{HF2}}(\delta)} = \frac{\delta - \beta}{i_{\mathrm{HF2}}(\beta) + (-i_{\mathrm{HF2}}(\delta))} \tag{4.21}$$

$$\rightarrow\ \theta_{\mathrm{x}} = \delta - \frac{-i_{\mathrm{HF2}}(\delta) \cdot (\delta - \beta)}{i_{\mathrm{HF2}}(\beta) - i_{\mathrm{HF2}}(\delta)}. \tag{4.22}$$

By substituting (4.20) and (4.22) into respectively (4.17) and (4.18), the expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ become:

$$Q_{\mathrm{B,av},\alpha} = \frac{i^2_{\mathrm{HF1}}(\alpha) \cdot (\beta - \alpha)}{2\,\omega_{\mathrm{s}}\,(i_{\mathrm{HF1}}(\beta) - i_{\mathrm{HF1}}(\alpha))}, \tag{4.23}$$

$$Q_{\mathrm{A,av},\delta} = \frac{i^2_{\mathrm{HF2}}(\delta) \cdot (\delta - \beta)}{2\,\omega_{\mathrm{s}}\,(i_{\mathrm{HF2}}(\beta) - i_{\mathrm{HF2}}(\delta))}. \tag{4.24}$$

According to Section 3.2: $i_{\mathrm{HF1}}(\alpha) = i_{\mathrm{HF1}}(t_\alpha)$, $i_{\mathrm{HF1}}(\beta) = i_{\mathrm{HF1}}(t_\beta)$, $i_{\mathrm{HF2}}(\beta) = i_{\mathrm{HF2}}(t_\beta)$, $i_{\mathrm{HF2}}(\delta) = i_{\mathrm{HF2}}(t_\delta)$, and $\alpha = \omega_{\mathrm{s}}\,t_\alpha$, $\beta = \omega_{\mathrm{s}}\,t_\beta$, $\delta = \omega_{\mathrm{s}}\,t_\delta$, where the bridge currents $i_{\mathrm{HF1}}(t_\alpha)$, $i_{\mathrm{HF1}}(t_\beta)$, $i_{\mathrm{HF2}}(t_\beta)$ and $i_{\mathrm{HF2}}(t_\delta)$ are given in Table A.5 of Appendix A. The bridge currents $i_{\mathrm{HF1}}(t_{\mathrm{i}})$ and $i_{\mathrm{HF2}}(t_{\mathrm{i}})$ required in Table A.5 are calculated using (3.47) and (3.48), which include commutation inductances L_{c1} and L_{c2}, and using the expressions for respectively $i_{\mathrm{L}}(t_{\mathrm{i}})$, $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$, and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}})$ listed in:

- $i_{\mathrm{L}}(t_{\mathrm{i}}) \rightarrow$ Table A.3;
- $i_{\mathrm{L_{c1}}}(t_{\mathrm{i}})$ and $i'_{\mathrm{L_{c2}}}(t_{\mathrm{i}}) \rightarrow$ Table A.6.

The time instances t_{i} required in Table A.5 are calculated using the expressions in Table A.2. Evidently, the expressions given in the 'mode 5 columns' of the mentioned tables should be taken. Substitution of all these expressions into (4.23) and (4.24) leads to the equations which allow to directly calculate $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$:

$$Q_{\mathrm{B,av},\alpha} = \frac{\Big(L_{\mathrm{c1}}\,(v_{\mathrm{DC1}}\,\tau_1 - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}\,\tau_2) + L\,v_{\mathrm{DC1}}\,\tau_1\Big)^2}{8\,\omega_{\mathrm{s}}^2\,v_{\mathrm{DC1}}\,L\,L_{\mathrm{c1}}\,(L_{\mathrm{c1}} + L)}, \tag{4.25}$$

$$Q_{\mathrm{A,av},\delta} = \frac{\frac{n_1}{n_2} \cdot \Big(L'_{\mathrm{c2}}\,(\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}\,\tau_2 - v_{\mathrm{DC1}}\,(2\,\phi + \tau_1)) + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}\,L\,\tau_2\Big)^2}{8\,\omega_{\mathrm{s}}^2\,L\,L'_{\mathrm{c2}}\,(L'_{\mathrm{c2}}\,(\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}} - v_{\mathrm{DC1}}) + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}\,L)}, \tag{4.26}$$

with $L'_{\mathrm{c2}} = \left(\frac{n_1}{n_2}\right)^2 \cdot L_{\mathrm{c2}}$.

Step 3: Solving the Resulting Equation Systems

By using (4.25) and (4.26) in 'interval conditions' (4.12) and (4.13), and in 'interval condition' (4.15), the conditions for each trajectory interval become:

Conditions for interval I (mode 5)—

$$\frac{\left(L_{\mathrm{c1}}\left(v_{\mathrm{DC1}}\,\tau_1 - \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,\tau_2\right) + L\,v_{\mathrm{DC1}}\,\tau_1\right)^2}{8\,\omega_{\mathrm{s}}^2\,v_{\mathrm{DC1}}\,L\,L_{\mathrm{c1}}\,(L_{\mathrm{c1}}+L)} = Q_{\mathrm{A/B,req,p}}, \tag{4.27}$$

$$\frac{\frac{n_1}{n_2}\cdot\left(L'_{\mathrm{c2}}\left(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,\tau_2 - v_{\mathrm{DC1}}\,(2\,\phi+\tau_1)\right) + \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,L\,\tau_2\right)^2}{8\,\omega_{\mathrm{s}}^2\,L\,L'_{\mathrm{c2}}\left(L'_{\mathrm{c2}}\left(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}} - v_{\mathrm{DC1}}\right) + \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,L\right)} = Q_{\mathrm{A/B,req,s}}. \tag{4.28}$$

Conditions for interval II (mode 5)—

$$\phi = 0, \tag{4.29}$$

$$\frac{\frac{n_1}{n_2}\cdot\left(L'_{\mathrm{c2}}\left(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,\tau_2 - v_{\mathrm{DC1}}\,(2\,\phi+\tau_1)\right) + \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,L\,\tau_2\right)^2}{8\,\omega_{\mathrm{s}}^2\,L\,L'_{\mathrm{c2}}\left(L'_{\mathrm{c2}}\left(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}} - v_{\mathrm{DC1}}\right) + \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,L\right)} = Q_{\mathrm{A/B,req,s}}. \tag{4.30}$$

Condition for interval III (mode 1^+)—

$$\tau_1 = \pi. \tag{4.31}$$

For each of the above trajectory intervals, closed-form solutions for the modulation angles τ_1, τ_2, and ϕ can be determined as explained below. In order to reduce the length of the presented equations, first a set of predefined terms is given:

$$e_1 = \frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,Q_{\mathrm{A/B,req,s}}\,\omega_{\mathrm{s}}, \tag{4.32}$$

$$e_2 = \frac{n_1}{n_2}\cdot v_{\mathrm{DC1}}\,\pi\,i_{\mathrm{DAB1}}, \tag{4.33}$$

$$e_3 = \frac{n_1}{n_2}\cdot\left(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}}\,(L'_{\mathrm{c2}}+L) - v_{\mathrm{DC1}}\,L'_{\mathrm{c2}}\right), \tag{4.34}$$

$$e_4 = 2\,\frac{n_1}{n_2}\,\sqrt{Q_{\mathrm{A/B,req,p}}\,L\,\omega_{\mathrm{s}}^2\,v_{\mathrm{DC1}}\,L_{\mathrm{c1}}\,(L_{\mathrm{c1}}+L)}, \tag{4.35}$$

$$e_5 = L\,L'_{\mathrm{c2}}\,\omega_{\mathrm{s}}\,(e_2 + 2\,e_1 + 2\,\sqrt{e_1\,(e_1+e_2)}). \tag{4.36}$$

Solution for interval I (mode 5)— The conditions for interval I (i.e. (4.27) and (4.28)), together with expression (3.40) for the mode 5 phase-shift angle ϕ, form a system of three equations that can be solved towards the modulation angles τ_1, τ_2, and ϕ, yielding:

$$\tau_1 = \frac{\sqrt{2}\left(L_{c1}\sqrt{\frac{n_1}{n_2}\cdot V_{DC2}\, e_3\, e_5} + e_4\, e_3 \cdot \left(\frac{n_1}{n_2}\right)^{-1}\right)}{v_{DC1}\, e_3\,(L_{c1}+L)}, \tag{4.37}$$

$$\tau_2 = \sqrt{\frac{2\, e_5}{\frac{n_1}{n_2}\cdot V_{DC2}\, e_3}}, \tag{4.38}$$

$$\phi = \frac{\tau_2 - \tau_1}{2} + \frac{i_{DAB1}\cdot \omega_s L \pi}{\tau_2 \cdot \frac{n_1}{n_2}\cdot V_{DC2}}. \tag{4.39}$$

Solution for interval II (mode 5)— The conditions for interval II (i.e. (4.29) and (4.30)), together with expression (3.40) for the mode 5 phase-shift angle ϕ, form a system of three equations that can be solved towards the modulation angles τ_1, τ_2, and ϕ, yielding:

$$\tau_1 = \frac{\sqrt{2}\left(e_5 + \omega_s\, L\, L'_{c2}\, e_2\left(\frac{\frac{n_1}{n_2}\cdot V_{DC2}}{v_{DC1}}\left(\frac{L}{L'_{c2}}+1\right)-1\right)\right)}{\sqrt{\frac{n_1}{n_2}\cdot V_{DC2}\, e_3\, e_5}}, \tag{4.40}$$

$$\tau_2 = \sqrt{\frac{2\, e_5}{\frac{n_1}{n_2}\cdot V_{DC2}\, e_3}}, \tag{4.41}$$

$$\phi = 0. \tag{4.42}$$

Solution for interval III (mode 1^+)— The condition for interval III (i.e. (4.31)), together with expression (3.39) for the mode 1^+ phase-shift angle ϕ, form a system of only two equations that cannot be solved. Nevertheless, it is shown in Section 4.2.2 that when calculating τ_2 with the solution for interval II (i.e. (4.41)), CDCB ZVS is always achieved. ϕ is then calculated with the '$-\sqrt{\ }$' solution[13] of (3.39). As a result, the proposed solution for interval III is:

[13]Remind that the '$-\sqrt{\ }$' solution of (3.39) should be taken in order to achieve efficient DAB operation, see Section 3.2.2.

$$\tau_1 = \pi, \tag{4.43}$$

$$\tau_2 = \sqrt{\frac{2\, e_5}{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}\, e_3}}, \tag{4.44}$$

$$\phi = \frac{-\tau_1 + \tau_2 + \pi}{2} - \sqrt{\frac{-(\tau_2 - \pi)^2 + \tau_1(2\pi - \tau_1)}{4} - \frac{i_{\mathrm{DAB1}} \cdot \omega_{\mathrm{s}} L \pi}{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}}. \tag{4.45}$$

Step 4: Final Calculation Procedure

Using the presented closed-form solutions (4.37)-(4.45) for the modulation angles τ_1, τ_2, and ϕ in the different trajectory intervals I, II, and III, a full-operating-range CDCB ZVS modulation scheme can be calculated. Figure 4.11 summarizes the calculation procedure which starts from an initial set of circuit level variables $\mathbf{h} = \mathbf{h_{init}} = (L_{\mathrm{init}}, L_{\mathrm{c1,init}}, L_{\mathrm{c2,init}},$ and $n_{1,\mathrm{init}}/n_{2,\mathrm{init}})$. Then it iterates through the complete DAB's operating range shown in Figure 3.6, passing the DAB operating point $i_{\mathrm{DAB1}}(\mathrm{i,j,k})$, $v_{\mathrm{DC1}}(\mathrm{i,j,k})$, $V_{\mathrm{DC2}}(\mathrm{i,j,k})$, the circuit variables $\mathbf{h}$, and the predefined switching frequency pattern (i.e. $f_{\mathrm{s}}(v_{\mathrm{DC1}})$, cf. (4.11)) to the core algorithm. Also the minimum required commutation charges[14] $Q_{\mathrm{A/B,req,p}}(v_{\mathrm{DC1}})$ (i.e. regarding ZVS of the primary side active bridge) and $Q_{\mathrm{A/B,req,s}}(V_{\mathrm{DC2}})$ (i.e. regarding ZVS of the secondary side active bridge) are passed to the core algorithm. There, for each operating point $i_{\mathrm{DAB1}}(\mathrm{i,j,k})$, $v_{\mathrm{DC1}}(\mathrm{i,j,k})$, $V_{\mathrm{DC2}}(\mathrm{i,j,k})$, the modulation angles τ_1, τ_2, and ϕ are calculated as follows:

- Step 1: Calculate τ_1, τ_2, and ϕ using (4.37)-(4.39) (interval I):
  - If: the result for ϕ is $\leqslant 0$ and the result for τ_1 is $\leqslant \pi \rightarrow$ stop calculation and output τ_1, τ_2, and ϕ;
  - Else if: the result for ϕ is $\leqslant 0$ and the result for τ_1 is $> \pi \rightarrow$ stop calculation and iterate circuit variables $\mathbf{h}$. It is analytically verified that in this case no CDCB ZVS is possible (see below);
  - Else if: the result for ϕ is $> 0 \rightarrow$ go to step 2.
- Step 2: Calculate τ_1, τ_2, and ϕ using (4.40)-(4.42) (interval II):
  - If: the result for τ_1 is $\leqslant \pi \rightarrow$ stop calculation and output τ_1, τ_2, and ϕ;

[14] The minimum required commutation charges $Q_{\mathrm{A/B,req,p}}(v_{\mathrm{DC1}})$ and $Q_{\mathrm{A/B,req,s}}(V_{\mathrm{DC2}})$ depend on the power switches (here only MOSFETs are considered) selected for the bridges of the DAB. $Q_{\mathrm{A/B,req,p}}(v_{\mathrm{DC1}})$ and $Q_{\mathrm{A/B,req,s}}(V_{\mathrm{DC2}})$ are determined as explained in step 2 of the CDCB ZVS verification method outlined in Section 3.3.2.

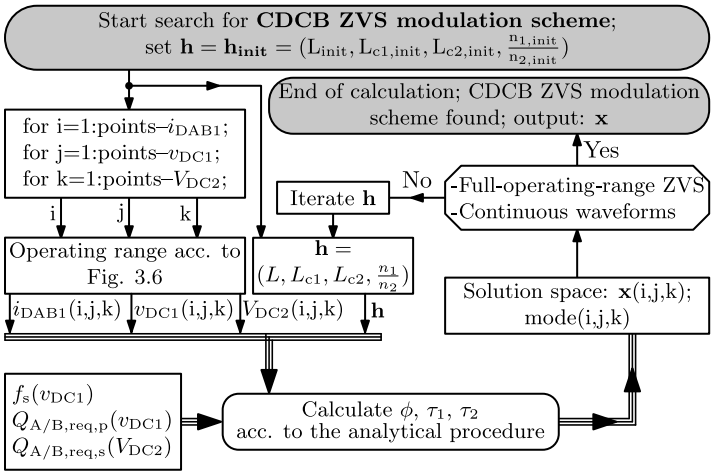


Figure 4.11: Procedure to determine a CDCB ZVS modulation scheme and corresponding modulation parameters ϕ, τ_1, and τ_2, using the analytical approach.

  - Else if: the result for τ_1 is $> \pi \rightarrow$ go to step 3.

- Step 3: Calculate τ_1, τ_2, and ϕ using (4.43)-(4.45) (interval III):
  - If: the result for τ_2 is $\leqslant \pi \rightarrow$ stop calculation and output τ_1, τ_2, and ϕ;
  - Else if: the result for τ_2 is $> \pi \rightarrow$ set τ_2 equal to π and recalculate ϕ using (4.45) $\rightarrow$ stop calculation and output τ_1, τ_2, and ϕ.

Note that the expressions (4.37)-(4.45) are derived for positive power flow (i.e. $i_{DAB1} \geqslant 0$). In case of negative power flow, τ_1, τ_2, and ϕ are calculated by following the same steps, inputting $i_{DAB1} = |i_{DAB1,1^-}|$ into the respective equations and recalculating ϕ with (i.e. according to (3.41)):

$$\forall\ i_{DAB1} < 0 : \phi = -(\tau_1 + \phi - \tau_2)|_{i_{DAB1}=|i_{DAB1,1^-}|}, \tag{4.46}$$

while τ_1 and τ_2 stay unchanged. When the phase-shift angle ϕ that is calculated in step 1 (i.e. regarding interval I) is $\leqslant 0$ and the pulse-width modulation angle τ_1 is $> \pi$, no CDCB ZVS is possible and iteration of circuit variables $\mathbf{h}$ is required. It is analytically verified that in this case the commutation charge $Q_{A,av,\alpha}$ that is available in the bridge current (i.e. regarding the primary side bridge current i_{HF1}) before switching instant $\theta_i = \alpha$, becomes smaller than the minimum required commutation charge $Q_{A/B,req,p}$ for the primary side active bridge (i.e. cf. (3.64)). Note that these conditions (i.e. $\phi \leqslant 0$ and $\tau_1 > \pi$, interval

I) can also be used in order to find an analytical solution for the maximum values of commutation inductances L_{c1} and L_{c2} that lead to full-operating-range ZVS (i.e. for a given switching frequency pattern) or in order to find an analytical solution for the maximum switching frequency (pattern) that leads to full-operating-range ZVS (i.e. for given values of commutation inductances L_{c1} and L_{c2}). These expressions are not given for the reason of brevity but, however, their derivation is relatively straightforward. It can be shown that the overall worst case and thus the determining DAB operating point regarding these maximum values is the one where v_{DC1} is lowest, V_{DC2} is lowest, and i_{DAB1} is highest. This operating point is indicated by a '★' in Figure 3.6 of Section 3.1.

4.2.2 Results of the Analytical Approach

In order to demonstrate the analytical approach, the value trajectories depicted in Figure 4.9 and in Figure B.7 (see Appendix B), which were obtained using the final (optimal), full-operating-range CDCB ZVS modulation scheme according to the numerical approach outlined in Section 4.1 (i.e. conform simulation example 2), are again calculated using the analytical approach. In order to allow a clear comparison (see inter alia Section 4.4) with the results obtained using the numerical approach, the values of the circuit variables L, L_{c1}, L_{c2}, and n_1/n_2 are kept the same as for simulation example 2 of the numerical approach, i.e. not executing the iteration of $\mathbf{h}$. It are the final design values which are the result of an iteration performed during the design phase of the converter prototype system:

- $L = 13\ \mu$H;
- $\frac{n_1}{n_2} = 1$;
- $L_{c1} = L_{c2} = 62.1\ \mu$H.

The switching frequency pattern according to (4.10) is applied, being slightly different as that one for the numerical approach where at high v_{DC1} and high i_{DAB1} a lowered switching frequency results (see Figure 4.7(b)).

Figure 4.12 depicts the value trajectories of several quantities calculated using the analytical approach for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999, and the worst case output voltage of $V_{DC2} = V_{DC2,min} = 370\ V$[15]. As expected, very similar trajectories as in Figure 4.9 (numerical approach) are obtained. From Figures 4.12(e) and 4.12(f) it can be seen that the available commutation charges $Q_{A,av,\alpha}$ and $Q_{B,av,\alpha}$ for switching

[15]Remind that the values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{DAB1,nom}$-line).

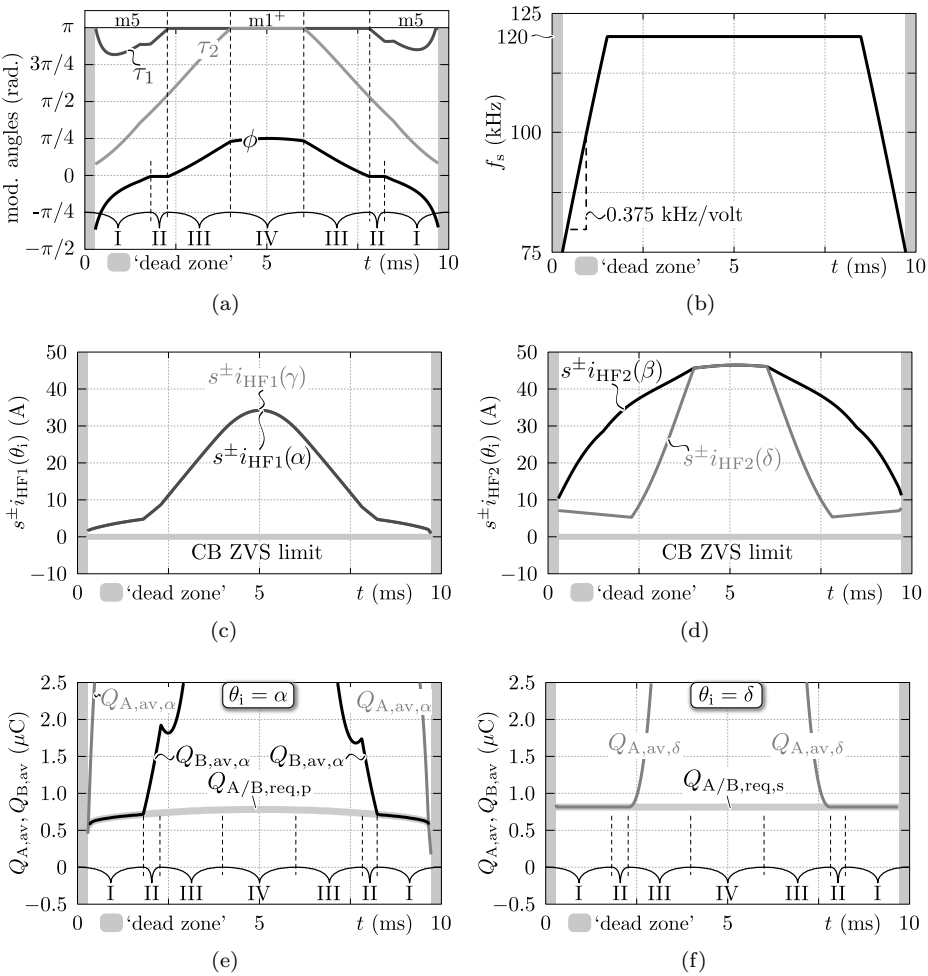


Figure 4.12: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the analytical approach.

instant $\theta_i = \alpha$ (see Figure 4.12(e)) as well as the available commutation charges $Q_{A,av,\delta}$ and $Q_{B,av,\delta}$ for switching instant $\theta_i = \delta$ (see Figure 4.12(f)) are higher than or equal to respectively the minimum required commutation charge $Q_{A/B,req,p}$ (cf. (3.64), ZVS of the primary side active bridge) and the minimum required commutation charge $Q_{A/B,req,s}$ (cf. (3.65), ZVS of the secondary side active bridge).

The same goes for the available commutation charges $Q_{\mathrm{A,av},\gamma}$ and $Q_{\mathrm{B,av},\gamma}$ regarding switching instant $\theta_{\mathrm{i}} = \gamma$ (ZVS of the primary side active bridge) and the available commutation charges $Q_{\mathrm{A,av},\beta}$ and $Q_{\mathrm{B,av},\beta}$ regarding switching instant $\theta_{\mathrm{i}} = \beta$ (ZVS of the secondary side active bridge), which are respectively shown in Figures B.9(b) and B.9(a) of Appendix B. This means that CDCB ZVS is guaranteed. As can be seen from Figures 4.12(a) and 4.12(b), the resulting trajectories of the modulation angles (i.e. τ_1, τ_2, and ϕ) and of the switching frequency f_{s} are again continuous, being highly desirable. Furthermore, only efficient modes 1 and 5 are used. It can thus be concluded that the CDCB ZVS modulation scheme obtained using the analytical approach is very similar to the one obtained in Section 4.1 (according to Figure 4.9) using the numerical approach, validating the analysis. The main difference between the two approaches can be found in trajectory interval III, where the closed-form solution for pulse-width-modulation angle τ_1 is based on the one for trajectory interval II. This deviation is most pronounced in the middle of the interval (i.e. at high v_{DC1}), which can be explained by the fact that, contrary to the numerical approach, for the analytical approach no switching frequency modulation is applied at high v_{DC1}.

Figure B.10 of Appendix B depicts the value trajectories calculated under the same conditions (nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$ and worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V) but under reduced input power: $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$ and PF = 0.983. It can be seen that full-operating-range CDCB ZVS, involving smooth modulation parameter trajectories, is once more obtained[16]. Again, the CDCB ZVS modulation scheme calculated using the analytical approach is very similar (except for some minor deviations) to the one obtained in Section 4.1 (according to Figure B.7 of Appendix B) using the numerical approach.

Figure 4.13 depicts the analytically obtained CDCB ZVS modulation scheme, calculated in the complete DAB's v_{DC1}-i_{DAB1}-plane shown in Figure 3.5 and regarding the worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V. The modulation parameters τ_2 and f_{s} are respectively shown in Figures 4.13(a) and 4.13(b) while, for brevity, τ_1 and ϕ are respectively shown in Figures B.8(a) and B.8(b) of Appendix B. Figure 4.13(d) depicts the calculated ZVS areas in the v_{DC1}-i_{DAB1} plane. It can be seen that the CDCB ZVS conditions are satisfied within the whole operating range while only switching mode 1 (applied in the high power regions of the v_{DC1}-i_{DAB1} plane) and switching mode 5 (applied in the low power regions of the v_{DC1}-i_{DAB1} plane) are used. The modulation scheme shown in Figures 4.13 and B.8 is once more very similar (except for some minor deviations) to the one shown in Figures 4.7 and B.5 obtained using the numerical approach.

[16]Note that here only efficient switching mode 5 is used due to the low required input power. The values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{\mathrm{DAB1,20\%}}$-line).

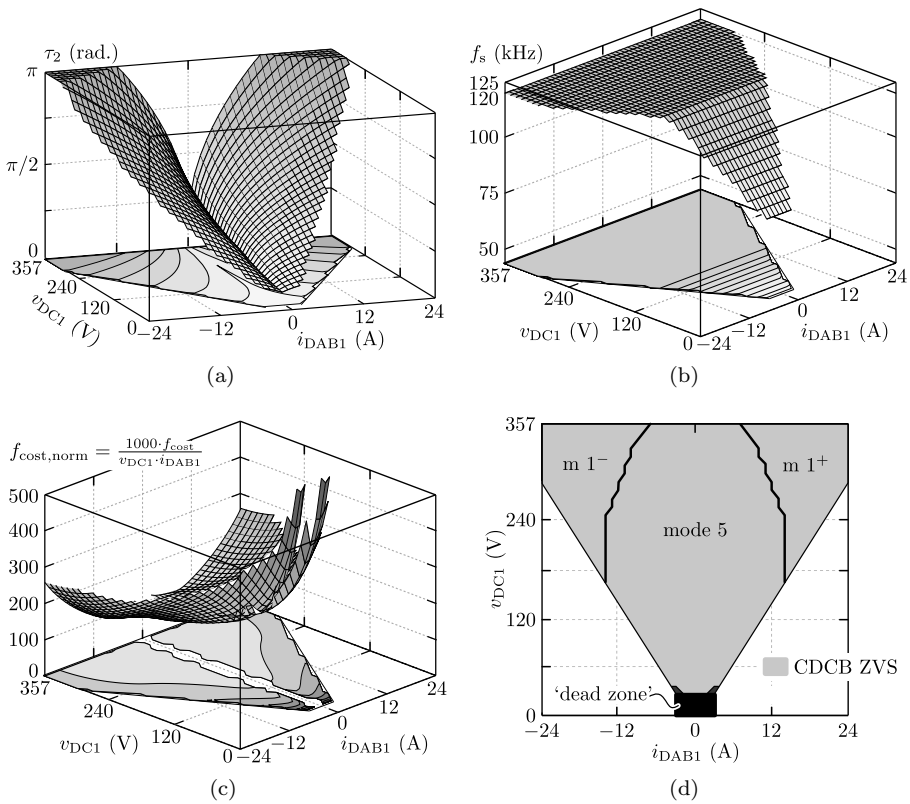


Figure 4.13: Results of the analytical calculation of a CDCB ZVS modulation scheme using primary and secondary side commutation inductances $L_{c1} = L_{c2} = 62.1\ \mu$H. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V.

4.3 Semi-Analytical Approach

In this section a semi-analytical approach is presented [87] as an alternative method to derive a full-operating-range CDCB ZVS modulation scheme for the DAB. From the results obtained using the numerical approach outlined in Section 4.1, it turned out that the commutation charge $Q_{\mathrm{B,av},\alpha}$ that is available in the bridge current (i.e. regarding the primary side bridge current i_{HF1}) after switching instant $\theta_{\mathrm{i}} = \alpha$ and the commutation charge $Q_{\mathrm{A,av},\delta}$ that is available in the bridge current (i.e. regarding the secondary side bridge current i_{HF2}) before switching instant $\theta_{\mathrm{i}} = \delta$ (in particular during mode 5 operation), are the most critical for achieving full-operating-range ZVS. In fact, the analytical approach proposed in Section 4.2 relies on the derivation of closed-form expressions for $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$. These expressions are then balanced with respectively the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ for the primary side active bridge and the the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ for the secondary side active bridge. The resulting equations are combined with the mode 5 expression for the phase-shift angle ϕ, in order to find closed-form solutions for modulation angles τ_1, τ_2, and ϕ. In principle this boils down to controlling $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ at switching instances $\theta_{\mathrm{i}} = \alpha$ and $\theta_{\mathrm{i}} = \delta$. The semi-analytical approach presented in this section, on the other hand, relies on the derivation of closed-form expressions for τ_1, τ_2, and ϕ that allow to control the inductor current i_{L} at switching instances $\theta_{\mathrm{i}} = \alpha$ and $\theta_{\mathrm{i}} = \delta$. Therewith, $i_{\mathrm{L}}(\alpha)$ can be set to a certain primary side commutation current $I^*_{\mathrm{p,comm}}$ and $i_{\mathrm{L}}(\delta)$ can be set to a certain secondary side commutation current $I^*_{\mathrm{s,comm}} = n_2/n_1 \cdot I^*_{\mathrm{s,comm}}$. This is actually a direct way to derive a current-based (CB) ZVS modulation scheme [83, 84]. In order to find a (full-operating-range) CDCB ZVS modulation scheme, both $I^*_{\mathrm{p,comm}}$ and $I^*_{\mathrm{s,comm}}$ are varied using a simple optimizer until $Q_{\mathrm{B,av},\alpha}$ and $Q_{\mathrm{A,av},\delta}$ are higher then or equal to the minimum required commutation charges $Q_{\mathrm{A/B,req,p}}$ and $Q_{\mathrm{A/B,req,s}}$, and until the minimum value of a predefined cost function is found. This approach is named the 'semi-analytical approach' since it combines analytical equations for τ_1, τ_2, and ϕ with an inner, numerical optimization algorithm. Similar as for the analytical approach, a predefined switching frequency pattern is applied, being determined by (4.11).

4.3.1 Semi-Analytical Solution for the Modulation Parameters

Since, compared to the numerical and the analytical approach, the semi-analytical approach does not provide an added value (see conclusions and the end of this chapter and in Chapter 7), here only a brief discussion is given. A detailed discussion of the semi-analytical approach can be found in [87] which is a publication that resulted from this work. The above mentioned closed-form expressions which allow to calculate modulation angles τ_1, τ_2, and ϕ so that $i_{\mathrm{L}}(\alpha)$ equals a certain primary side commutation current $I^*_{\mathrm{p,comm}}$ and $i_{\mathrm{L}}(\delta)$ equals a certain secondary

side commutation current $I'^{*}_{\mathrm{s,comm}}$, are given in Section IV of [84] which is also a publication that resulted from this work. Although the exact derivation of these expression is omitted in this text for the reason of brevity, only the solutions are given below. These can be subdivided into three groups, named 'Mode 5 - solutions A', 'Mode 5 - solutions B', and 'Mode 1^+ - solutions'.

Mode 5 - solutions A—

$$\tau_1 = \omega_\mathrm{s} L \left(\frac{2\, I^{*}_{\mathrm{p,comm}}}{v_{\mathrm{DC1}}} - \frac{d\, I'^{*}_{\mathrm{s,comm}}}{v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} \right) - \sqrt{\frac{d\, \omega_\mathrm{s} L}{v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} \left(\frac{d (I'^{*}_{\mathrm{s,comm}})^2\, \omega_\mathrm{s} L}{v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} - 2\, i_{\mathrm{DAB1}}\, \pi \right)}, \tag{4.47}$$

$$\tau_2 = \frac{-I'^{*}_{\mathrm{s,comm}}\, \omega_\mathrm{s} L}{v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} - \sqrt{\frac{\omega_\mathrm{s} L}{v_{\mathrm{DC1}}\, \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} \left(\frac{(I'^{*}_{\mathrm{s,comm}})^2\, \omega_\mathrm{s} L}{v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}} - \frac{2}{d}\, i_{\mathrm{DAB1}}\, \pi \right)}, \tag{4.48}$$

$$\phi = \frac{-\omega_\mathrm{s} L\, (I^{*}_{\mathrm{p,comm}} + I'^{*}_{\mathrm{s,comm}})}{v_{\mathrm{DC1}}}. \tag{4.49}$$

Mode 5 - solutions B—

$$\tau_1 = \pi, \tag{4.50}$$

$$\tau_2 = \frac{\tau_1}{d} - \frac{2\, \omega_\mathrm{s} L\, I^{*}_{\mathrm{p,comm}}}{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}, \tag{4.51}$$

$$\phi = \frac{\tau_2 - \tau_1}{2} + \frac{i_{\mathrm{DAB1}} \cdot \omega_\mathrm{s} L \pi}{\tau_2 \cdot \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}. \tag{4.52}$$

Mode 1^+ - solutions—

$$\tau_1 = \pi, \tag{4.53}$$

$$\tau_2 = \frac{\tau_1}{d} - \frac{2\, \omega_\mathrm{s} L\, I^{*}_{\mathrm{p,comm}}}{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}, \tag{4.54}$$

$$\phi = \frac{-\tau_1 + \tau_2 + \pi}{2} - \sqrt{\frac{-(\tau_2 - \pi)^2 + \tau_1 (2\pi - \tau_1)}{4} - \frac{i_{\mathrm{DAB1}} \cdot \omega_\mathrm{s} L \pi}{\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}}}}. \tag{4.55}$$

By combining the above closed-form solutions (4.47)-(4.55) for the modulation angles τ_1, τ_2, and ϕ with a simple optimizer, a full-operating-range CDCB ZVS modulation scheme can be calculated. Figure 4.14 summarizes the calculation procedure which starts from an initial set of circuit level variables $\mathbf{h} = \mathbf{h_{init}} = (L_{\text{init}}, L_{\text{c1,init}}, L_{\text{c2,init}},$ and $n_{1,\text{init}}/n_{2,\text{init}})$. Then it iterates through the complete DAB's operating range shown in Figure 3.6, passing the DAB operating point $i_{\text{DAB1}}(\text{i,j,k})$, $v_{\text{DC1}}(\text{i,j,k})$, $V_{\text{DC2}}(\text{i,j,k})$, the circuit variables $\mathbf{h}$, and the predefined switching frequency pattern (i.e. $f_{\text{s}}(v_{\text{DC1}})$, cf. (4.11)), as well as the minimum required commutation charges $Q_{\text{A/B,req,p}}(v_{\text{DC1}})$ and $Q_{\text{A/B,req,s}}(V_{\text{DC2}})$ to the core algorithm. There, for each operating point $i_{\text{DAB1}}(\text{i,j,k})$, $v_{\text{DC1}}(\text{i,j,k})$, $V_{\text{DC2}}(\text{i,j,k})$, the modulation angles τ_1, τ_2, and ϕ are calculated as follows:

1. Calculate τ_1, τ_2, and ϕ using (4.47)-(4.49), 'Mode 5 - solutions A':
   - If: the result for ϕ is $\leqslant 0$ and the result for τ_1 is $\leqslant \pi \rightarrow$ stop calculation and output τ_1, τ_2, and ϕ;
   - Else if: the result for ϕ is $\leqslant 0$ and the result for τ_1 is $> \pi \rightarrow$ go to step 2.
2. Calculate τ_1, τ_2, and ϕ using (4.50)-(4.52), 'Mode 5 - solutions B':
   - If: the result for ϕ is $\leqslant 0 \rightarrow$ stop calculation and output τ_1, τ_2, and ϕ;
   - Else if: the result for ϕ is $> 0 \rightarrow$ go to step 3.
3. Calculate τ_1, τ_2, and ϕ using (4.53)-(4.55), 'Mode 1^+ - solutions'.

The set values $I^*_{\text{p,comm}}$ and $I'^*_{\text{s,comm}}$ for each operating point $i_{\text{DAB1}}(\text{i,j,k})$, $v_{\text{DC1}}(\text{i,j,k})$, $V_{\text{DC2}}(\text{i,j,k})$ are determined using a simple optimizer that iterates $I^*_{\text{p,comm}}$ and $I'^*_{\text{s,comm}}$ until the CDCB ZVS constraints conform the CDCB ZVS verification method outlined in Section 3.3.2 are satisfied. Additionally the optimizer minimizes an arbitrarily defined cost function. After the calculation is finished for the entire DAB operating range, it is checked if full-operating-range CDCB ZVS is achieved. If this is not the case, circuit level variables $\mathbf{h}$ are iterated until CDCB ZVS is obtained in the complete operating range, and until the resulting modulation parameter trajectories are continuous (discontinuous steps in $\mathbf{x}$ are highly undesirable), yielding the final semi-analytical CDCB ZVS modulation scheme. Note that the expressions (4.37)-(4.45) are derived for positive power flow (i.e. $i_{\text{DAB1}} \geqslant 0$). In case of negative power flow, τ_1, τ_2, and ϕ are calculated by following the same steps, inputting $i_{\text{DAB1}} = |i_{\text{DAB1,1}^-}|$ into in the respective equations and recalculating ϕ with (i.e. according to (3.41)):

$$\forall\ i_{\text{DAB1}} < 0 : \phi = -(\tau_1 + \phi - \tau_2)|_{i_{\text{DAB1}}=|i_{\text{DAB1,1}^-}|}, \tag{4.56}$$

while τ_1 and τ_2 stay unchanged.

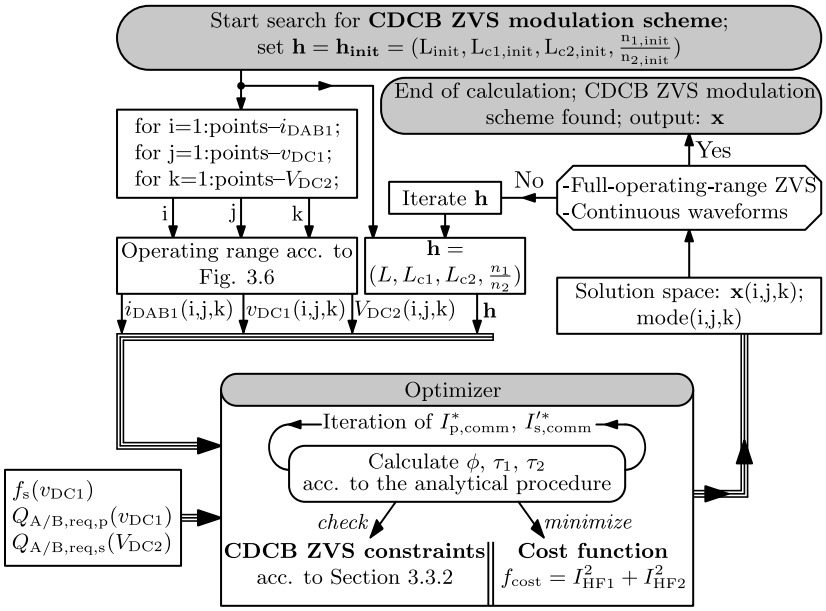


Figure 4.14: Procedure to determine a CDCB ZVS modulation scheme and corresponding modulation parameters ϕ, τ_1, and τ_2, using the semi-analytical approach.

4.3.2 Results of the Semi-Analytical Approach

In order to demonstrate the semi-analytical approach, the value trajectories depicted in Figure 4.9 and in Figure B.7 (see Appendix B) which were obtained using the final (optimal), full-operating-range CDCB ZVS modulation scheme according to the numerical approach outlined in Section 4.1 (i.e. conform simulation example 2), are again calculated using the semi-analytical approach. Similar as for the demonstration of the analytical and the numerical approach, the final design values of the circuit variables L, L_{c1}, L_{c2}, and n_1/n_2 are taken in order to enable a clear comparison:

- $L = 13$ μH;
- $\frac{n_1}{n_2} = 1$;
- $L_{c1} = L_{c2} = 62.1$ μH.

This means that the iteration of $\mathbf{h}$ is not executed. Similar as for the analytical approach, the switching frequency pattern according to (4.11) is applied, being

slightly different as the one for the numerical approach where at high v_{DC1} and high i_{DAB1} a lowered switching frequency results (see Figure 4.7(b)). The cost function used in the optimizer is the same as the one used for the numerical approach, i.e. according to (4.1).

Figure 4.15 depicts the value trajectories of several quantities calculated using the semi-analytical approach for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of PF = 0.999, and the worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370\ \mathrm{V}$[17]. As expected, very similar trajectories as in Figure 4.9 (numerical approach) are obtained. From Figures 4.15(e) and 4.15(f) it can be seen that the available commutation charges $Q_{\mathrm{A,av},\alpha}$ and $Q_{\mathrm{B,av},\alpha}$ for switching instant $\theta_{\mathrm{i}} = \alpha$ (see Figure 4.15(e)) as well as the available commutation charges $Q_{\mathrm{A,av},\delta}$ and $Q_{\mathrm{B,av},\delta}$ for switching instant $\theta_{\mathrm{i}} = \delta$ (see Figure 4.15(f)) are higher than or equal to respectively the minimum required commutation charge $Q_{\mathrm{A/B,req,p}}$ (cf. (3.64), ZVS of the primary side active bridge) and the minimum required commutation charge $Q_{\mathrm{A/B,req,s}}$ (cf. (3.65), ZVS of the secondary side active bridge). The same goes for the available commutation charges $Q_{\mathrm{A,av},\gamma}$ and $Q_{\mathrm{B,av},\gamma}$ regarding switching instant $\theta_{\mathrm{i}} = \gamma$ (ZVS of the primary side active bridge) and the available commutation charges $Q_{\mathrm{A,av},\beta}$ and $Q_{\mathrm{B,av},\beta}$ regarding switching instant $\theta_{\mathrm{i}} = \beta$ (ZVS of the secondary side active bridge), which are respectively shown in Figures B.12(b) and B.12(a) of Appendix B. This means that CDCB ZVS is guaranteed. As can be seen from Figures 4.15(a) and 4.15(b), the resulting trajectories of the modulation angles (i.e. τ_1, τ_2, and ϕ) and of the switching frequency f_{s} are again continuous, being highly desirable. Furthermore, only efficient modes 1 and 5 are used. It can thus be concluded that the CDCB ZVS modulation scheme obtained using the semi-analytical approach is very similar (except from some minor deviations) to the one obtained in Section 4.1 (according to Figure 4.9) using the numerical approach and to the one obtained in Section 4.2 (according to Figure 4.12) using the analytical approach, validating the analysis. The deviation from the numerical approach is most pronounced in the middle of the half cycle (i.e. at high v_{DC1}), which can be explained by the fact that, contrary to the numerical approach, for the semi-analytical approach (similar as for the analytical approach) no switching frequency modulation is applied at high v_{DC1}.

Figure B.13 of Appendix B depicts the value trajectories calculated under the same conditions (nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$ and worst case output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370\ \mathrm{V}$) but under reduced input power: $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$ and PF = 0.983. It can be seen that full-operating-range CDCB ZVS, involving smooth modulation parameter trajectories,

[17] Remind that the values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{\mathrm{DAB1,nom}}$-line).

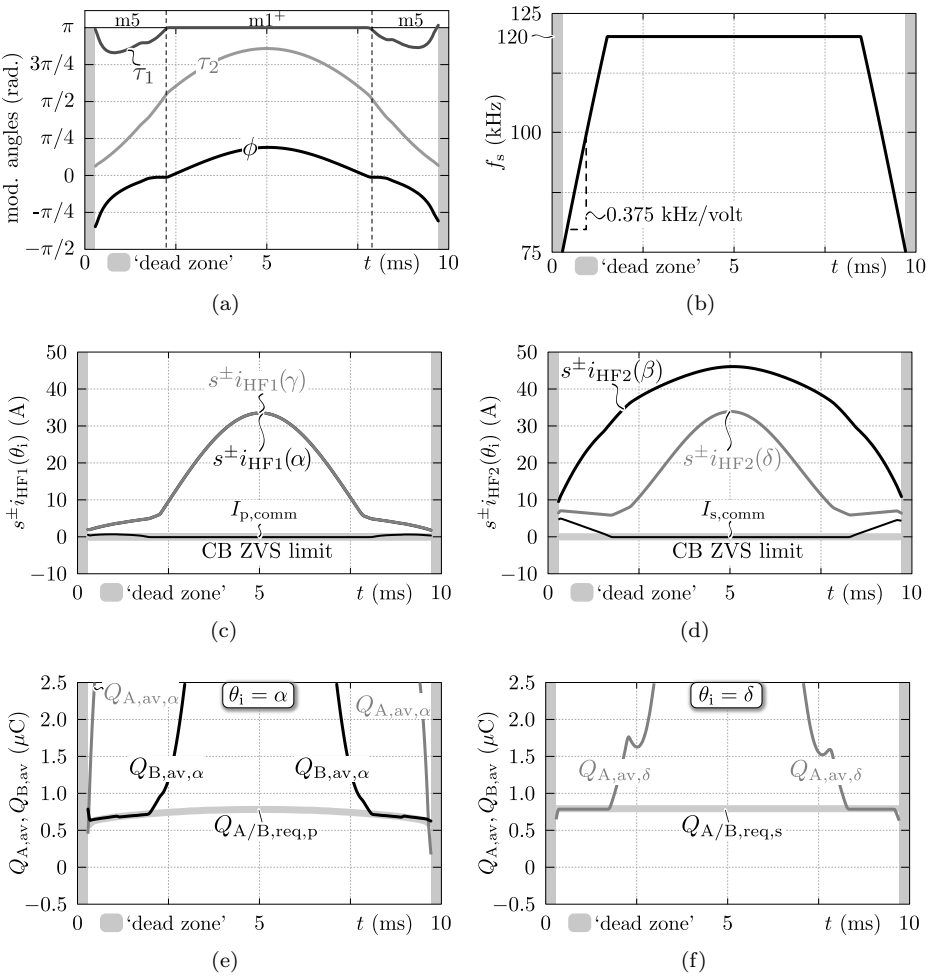


Figure 4.15: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the semi-analytical approach.

is once more obtained[18]. Again, the CDCB ZVS modulation scheme calculated using the semi-analytical approach is very similar (except for some minor deviations)

[18]Note that here only efficient switching mode 5 is used due to the low required input power. The values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF are shown in Figure 4.3 (see $i_{DAB1,20\%}$-line).

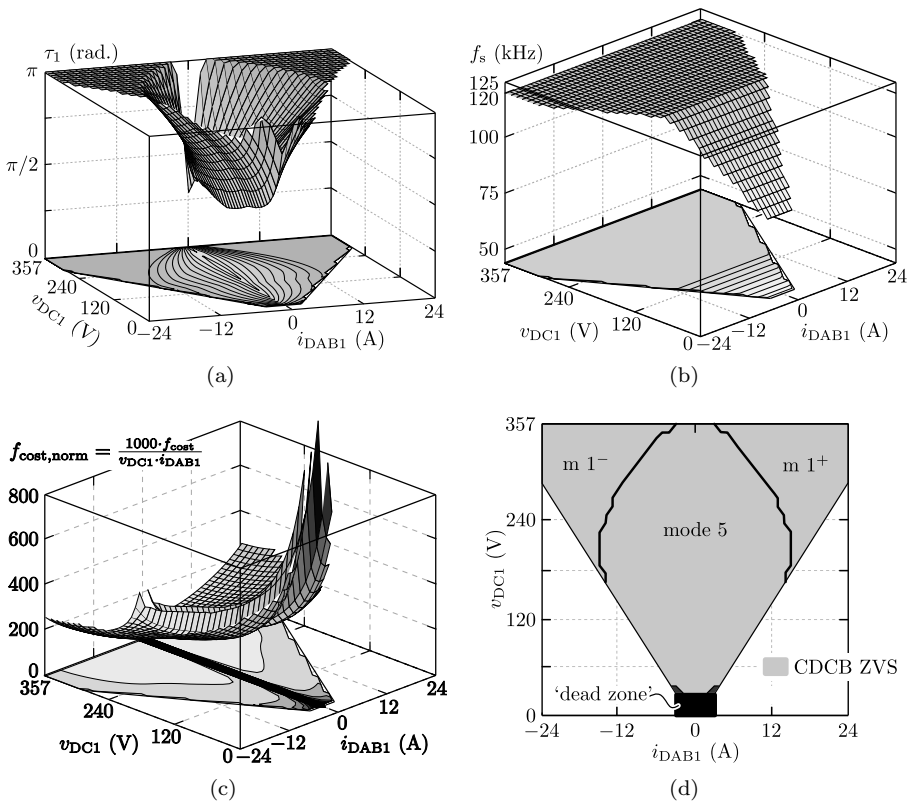


Figure 4.16: Results of the analytical calculation of a CDCB ZVS modulation scheme using primary and secondary side commutation inductances $L_{c1} = L_{c2} = 62.1\ \mu$H. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the semi-analytical approach.

to the one obtained in Section 4.1 (according to Figure B.7 of Appendix B) using the numerical approach, and to the one obtained in Section 4.2 (according to Figure B.10 of Appendix B) using the analytical approach, validating the analysis.

Figure 4.16 depicts the semi-analytically obtained CDCB ZVS modulation scheme, calculated in the complete DAB's v_{DC1}-i_{DAB1}-plane shown in Figure 3.5 and regarding the worst case output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters τ_2 and f_s are respectively shown in Figures 4.16(a) and 4.16(b) while, for brevity, τ_1 and ϕ are respectively shown in Figures B.11(a) and B.11(b) of Appendix B. Figure 4.16(d) depicts the calculated ZVS areas in the v_{DC1}-i_{DAB1} plane. It can be seen that the CDCB ZVS conditions are satisfied within the whole operating range while only switching mode 1 (applied in the high

power regions of the v_{DC1}-i_{DAB1} plane) and switching mode 5 (applied in the low power regions of the v_{DC1}-i_{DAB1} plane) are used. The modulation scheme shown in Figures 4.16 and B.11 is once more very similar (except for some minor deviations) to the one shown in Figures 4.7 and B.5 obtained using the numerical approach, and to the one shown in Figures 4.13 and B.8 obtained using the analytical approach.

4.4 Comparison

In this section a first comparison of the full-operating-range ZVS modulation schemes for the DAB, which are derived above using the three proposed approaches, is presented. The three approaches are:

- The numerical approach according to Section 4.1;
- The analytical approach according to Section 4.2;
- The semi-analytical approach according to Section 4.3.

Note that this first comparison is rather illustrative. An extensive comparison of the three modulation schemes, i.e. regarding the losses in the different converter components and regarding the EMC input filter requirements, is given in Chapter 5. Note also that regarding the effort required from the user to implement the proposed approaches, and regarding the required computational power, the numerical approach performs the worst while the analytical approach performs the best.

4.4.1 Cost Functions

In a first step the cost function calculated with the analytically (index 'A') and the semi-analytically (index 'SA') derived modulation schemes are compared with the cost function calculated with the numerically (index 'N') derived modulation scheme. Figure 4.17(a) depicts the 'Analytical to Numerical' cost function ratio

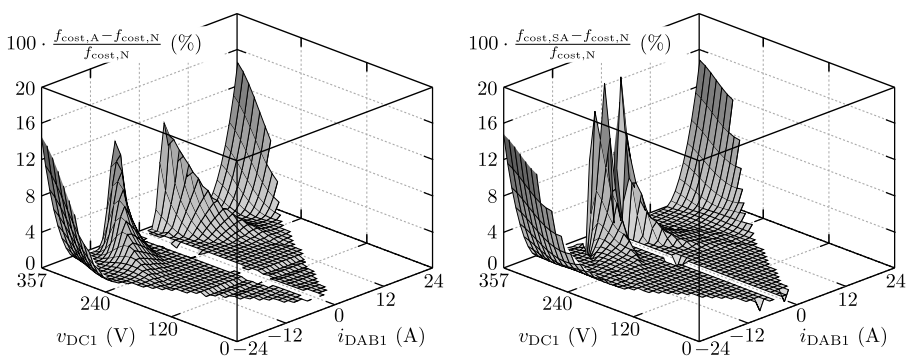


Figure 4.17: (a) 'Analytical to Numerical' cost function ratio, and (b) 'Semi-Analytical to Numerical' cost function ratio (both expressed in percent).

(expressed in percent), which is calculated as:

$$100 \cdot \frac{f_{\text{cost,A}} - f_{\text{cost,N}}}{f_{\text{cost,N}}} \ (\%). \tag{4.57}$$

Figure 4.17(b) depicts the 'Semi-Analytical to Numerical' cost function ratio (expressed in percent), which is calculated as:

$$100 \cdot \frac{f_{\text{cost,SA}} - f_{\text{cost,N}}}{f_{\text{cost,N}}} \ (\%). \tag{4.58}$$

Remind that the individual cost functions $f_{\text{cost,N}}$, $f_{\text{cost,A}}$, and $f_{\text{cost,SA}}$ are defined by (4.1). The depicted cost function ratios are calculated in the complete DAB's v_{DC1}-i_{DAB1}-plane shown in Figure 3.5 and regarding the nominal output voltage of $V_{\text{DC2}} = V_{\text{DC2,nom}} = 400$ V. It can be seen that within the major part of the v_{DC1}-i_{DAB1}-plane, there is no significant difference in the resulting cost functions. However, in some regions, the cost functions of both the analytically and the semi-analytically derived modulation schemes are higher than the cost function of the numerically calculated modulation scheme. This is in particular the case along the mode boundaries and at high v_{DC1} and high i_{DAB1}. For output voltages other than $V_{\text{DC2,nom}}$ similar results are obtained. As expected, this first comparison shows an advantage for the numerically calculated modulation scheme.

4.4.2 HF AC-Link Current Values

As it is more relevant to inspect the results obtained from a run through a half cycle of the AC input voltage, Figure 4.18 depicts the value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\text{AC}} = 230\ \text{V}_{\text{rms}}$, at the nominal input current of $I_{\text{AC,P}} = I_{\text{AC,P,nom}} = 16\ \text{A}_{\text{rms}}$, a power factor of $\text{PF} = 0.999$, and an output voltage of $V_{\text{DC2}} = V_{\text{DC2,nom}} = 400$ V. Remind that the values for i_{DAB1} (see Figure 4.3, $i_{\text{DAB1,nom}}$-line) that are applied during the half cycle in order to achieve the requested AC line current and PF are calculated using control equation (3.12). The resulting trajectories of the different normalized cost functions, with $f_{\text{cost,norm}} = 1000 \cdot f_{\text{cost}}(\mathbf{x})/(v_{\text{DC1}}\, i_{\text{DAB1}})$, are shown in Figure 4.18(a). As could be expected from the cost function ratios shown in Figure 4.17, $f_{\text{cost,norm,N}}$ is the lowest but the difference with $f_{\text{cost,norm,A}}$ and $f_{\text{cost,norm,SA}}$ is negligible. The other value trajectories depicted in Figure 4.18 are:

- Figure 4.18(b): the primary side bridge currents;
- Figure 4.18(c): the secondary side bridge currents;

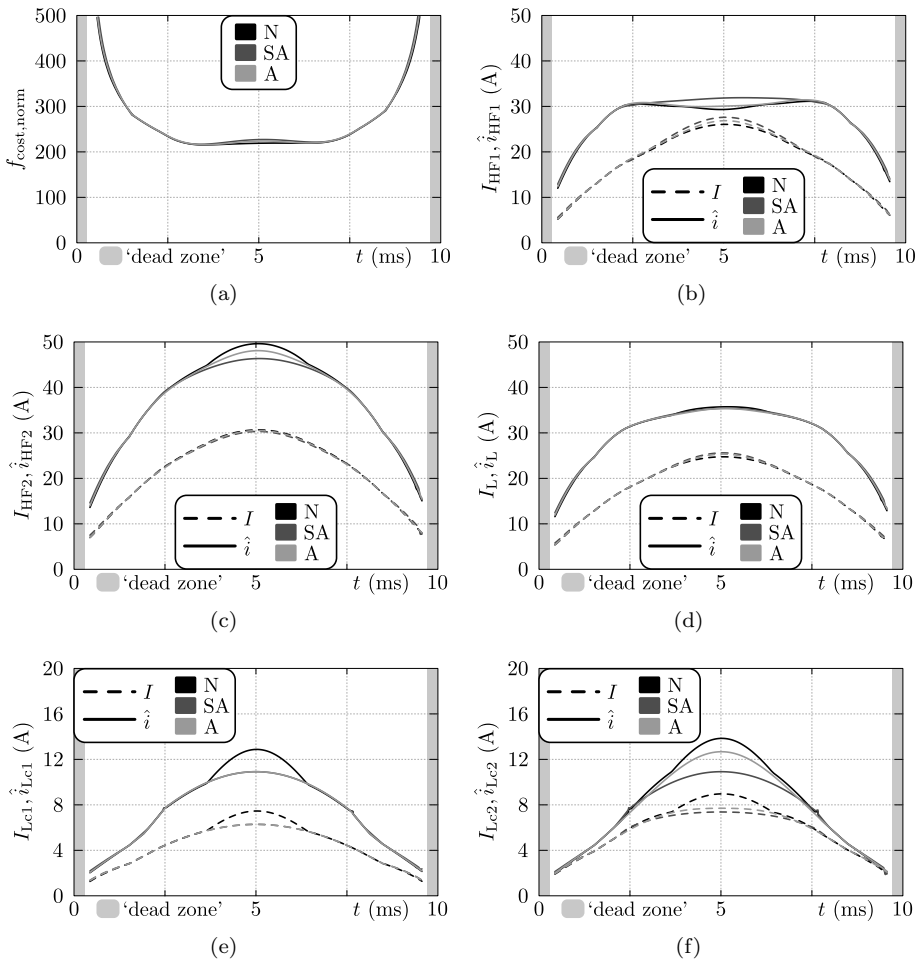


Figure 4.18: Resulting value trajectories of several quantities calculated using the three proposed ZVS modulation schemes, for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$ (cf. Figure 4.3, $i_{\mathrm{DAB1,nom}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V.

- Figure 4.18(d): the currents in inductance L, being the currents flowing in the external series inductor L_{ext};
- Figure 4.18(e): the currents in inductance L_{c1}, being the currents in the primary side commutation inductor L_{c1};

- Figure 4.18(f): the currents in inductance L_{c2}, being the magnetizing currents of the HF AC-link transformer[19].

The dashed lines correspond with the local RMS values of the above mentioned currents while the solid lines correspond with their peak values. It can be seen that although the numerically derived modulation scheme performs the best regarding the cost function and regarding the RMS values of the bridge currents, it performs the worst regarding the RMS values and peak values of the currents in commutation inductances L_{c1} and L_{c2}. The difference is most pronounced in the middle of the half cycle (i.e. at high v_{DC1}). This can be explained by the fact that for the numerically derived modulation scheme frequency modulation is applied at high v_{DC1}, while this is not the case for the analytically and the semi-analytically derived modulation schemes. Very similar results are obtained for the value trajectories calculated under the same conditions (nominal AC input voltage of $V_{AC} = 230\ V_{rms}$ and nominal output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V) but under reduced input power: $I_{AC,P} = 0.2 \cdot I_{AC,P,nom} = 3.2\ A_{rms}$ and PF = 0.983, which are shown in Figure B.14 of Appendix B.

[19]Note that in this work L_{c2} is implemented by the magnetizing inductance of the HF AC-link transformer ($L_{c2} = L_M$), avoiding increased volume and costs (see Section 5.2).

4.5 Conclusion

This chapter is devoted to the derivation of full-operating-range (i.e. regarding the complete DAB's operating range derived in Section 3.1) ZVS modulation schemes for the FBFB DAB used in the investigated 1-S DAB AC–DC converter. Three different approaches are presented, being a numerical approach (see Section 4.1), an analytical approach (see Section 4.2), and a semi-analytical approach (see Section 4.3). All three approaches rely on the current-dependent charge-based (CDCB) ZVS verification method proposed in Section 3.3, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions.

In the introduction of this chapter it is explained why closed-form solutions, such as presented in [92], for the calculation of the modulation parameters are not directly feasible. Therefore, in a first step a **numerical approach** is introduced, involving an optimization procedure which is based on a constrained numerical minimum search (i.e. a constrained nonlinear optimization). The numerical nature of the proposed optimization algorithm allows users to freely define the cost function to be minimized. Thereby converter related losses, but also requirements concerning system volume, weight, control, EMC,... can be included. The CDCB ZVS verification method is implemented in the optimization algorithm in the form of constraint functions. Furthermore, the algorithm examines all twelve switching modes that are possible with the (FBFB) DAB converter. In a first scenario, using the traditional DAB AC-link implementation (i.e. a transformer and series inductor), considering 'theoretical' current-based (CB) ZVS, and minimizing with respect to the summed, squared RMS values of the bridge currents (this cost function is proportional to the conduction losses of the DAB), a similar modulation scheme as in [92] is outputted, validating the algorithm. However, using the CDCB ZVS verification method it is shown that this CB ZVS modulation scheme results in hard-switching operation within large regions of the DAB's operating range. By replacing the CB ZVS constraints by the CDCB ZVS constraints, it is demonstrated that an efficient full-operating-range ZVS modulation scheme which involves continuous modulation parameter trajectories cannot be obtained with the traditional HF AC-link implementation of the DAB. Therefore, in a second scenario, 'commutation inductance(s)' are added, benefiting the ZVS conditions due to the injection of small reactive currents in the active bridges. This yields the first ever reported full-operating-range ZVS modulation scheme which involves smooth and continuous modulation parameter trajectories. Furthermore, it turns out that for each power flow direction only two out of the twelve possible switching modes are feasible for efficient ZVS operation. These are mode 1 (high power mode) and mode 5 (low power mode), i.e. conform Chapter 3, forming the basis of all derived ZVS modulation schemes. Based on the results acquired from the numerical approach, in a second step an **analytical approach** is proposed, providing a general, directly employable closed-form analytical solution for the

calculation of the modulation parameters which lead to full-operating-range CDCB ZVS operation. Therewith, the direct application to a given (FBFB) DAB converter is facilitated, provided that commutation inductors with appropriate inductance value are present in the HF AC-link. The presented expressions for the modulation parameters are the result of the identification and reproduction of distinct intervals in the value trajectories obtained using the numerical approach. In a third step, a **semi-analytical approach** is presented as an alternative method to derive a full-operating-range CDCB ZVS modulation scheme for the DAB. This approach is named the 'semi-analytical approach' since it combines analytical equations for the modulation parameters with an inner, numerical optimization algorithm.

A first comparison of the three approaches shows a minor deviation of the calculated cost functions, and of the RMS and peak values of the resulting HF AC-link currents. This means that the analytical, as well as the semi-analytical approaches yield a close to 'optimal' modulation scheme. From the different optimization examples performed it is furthermore concluded that the DAB's ZVS constraint functions are the determining factor for the final values of the calculated modulation parameters. Consequently, the cost function is of less importance in the determination of a ZVS modulation scheme. This means that also for other cost functions the results of the three approaches will be very similar. This is an important conclusion which promotes the use of the analytical approach as it is directly implementable by the user, and requires the least computational power. The impact of the three calculation approaches on the losses in the different converter components and on the EMC input filter requirements is further investigated in Chapter 5. Regarding the effort required from the user to implement the proposed approaches, and regarding the required computational power, the numerical approach performs the worst while the analytical approach performs the best.

Another conclusion that is drawn from this chapter is that at low DAB input voltages (v_{DC1}), the switching frequency has to be lowered in order to achieve full-operating-range ZVS. If not doing so, very low values for the commutation inductances L_{c1} and L_{c2} would be required, resulting in unacceptably high values of the HF AC-link currents, being detrimental for the conversion efficiency. The modulation schemes derived in this chapter are obtained using equal primary and secondary side commutation inductances (i.e. $L_{\mathrm{c1}} = L_{\mathrm{c2}}$). Nevertheless, HF AC-link implementations with only one commutation inductance (i.e. finite L_{c1}, infinite L_{c2} or infinite L_{c1}, finite L_{c2}) are also feasible, which however yield more unbalanced HF AC-link current values. In this work L_{c2} is implemented by the magnetizing inductance of the HF AC-link transformer ($L_{\mathrm{c2}} = L_{\mathrm{M}}$), avoiding increased volume and costs (see Section 5.2). Furthermore, this chapter also provides guidelines for the effective selection of the circuit level variables $\mathbf{h} = (L, L_{\mathrm{c1}}, L_{\mathrm{c2}},$ and $n_1/n_2)$, and for the switching frequency pattern to be applied.

5

Modeling of the Main Converter Components

Based on the values for the circuit level variables L, L_{c1}, L_{c2}, and n_1/n_2, and based on the CDCB ZVS modulation schemes derived in Chapter 4 (i.e. according to the numerical, the analytical, and the semi-analytical approach), in this chapter the main functional elements of the investigated single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter are designed. As the main focus of this thesis is on the (re)development of the DAB modulation schemes and on the provision of solutions for the fundamental limitations of the existing DAB implementations (see Chapter 2), here the designs of the individual converter components are performed separately. This implies separation of the partial converter functions and omission of outer (global) optimization loops (i.e. with regard to the circuit level variables and the switching frequency). Nevertheless, state-of-the art design methods/procedures, models for the component losses, and volume models are combined with custom developed (local) optimization algorithms in order to obtain a high-efficiency and high-power-density converter design that is in compliance with the system requirements specified in Table 1.1 of Section 1.3. Consequently, each section of this chapter is dedicated to the design of the individual functional converter elements:

- Section 5.1: semiconductors and heat sinks;
- Section 5.2: magnetic elements of the DAB: inductors and transformer;
- Section 5.4: EMC input filter;
- Section 5.3: output filter capacitors;
- Section 5.5: control board.

Besides the component models and design procedures, in each section the three CDCB ZVS modulation schemes proposed in Chapter 4 are compared with regard to the resulting losses in the respective component(s). In particular for the semiconductor - heat sink assemblies (see Section 5.1) and for the magnetic elements of the DAB (see Section 5.2), additionally, possible improvements and further optimizations of the hardware realizations are suggested and the resulting performance enhancement is quantified. Furthermore, in Section 5.4 the EMC input filter requirements for the three modulation schemes are evaluated. Lastly, in Section 5.6, by summation of the losses and volumes of the different sub-components, the overall performance of the converter prototype system (further referred to as 'converter design A') is calculated and compared with the performance that could by achieved with a further optimized design (further referred to as 'converter design B'). In Section 6.2.2 of the next chapter (i.e. Chapter 6), the efficiency curves calculated in this chapter are compared with the efficiencies obtained (measured) from the 3.7 kW DAB AC–DC converter prototype developed in this work, as well as with the efficiency curves of several (similar) state-of-the-art dual-stage prototype systems reported in literature. The final prototype hardware realization is shown in Section 5.6.3 of this chapter.

5.1 Semiconductors and Heat Sinks

This section provides models which allow to accurately calculate the losses generated, and the volume occupied by the semiconductor switching devices (i.e. the MOSFETs including the heat sinks). First, in Section 5.1.1, the selection of the used MOSFETs for both the DAB and the SR is explained/motivated. Thereafter, in Section 5.1.2, basic equations are presented which, given a certain DAB modulation scheme, allow to predict the most relevant semiconductor losses. Thereby, as the modulation schemes presented in Chapter 4 allow to operate the DAB under ZVS within the entire mains period, the conduction losses are dominant. However, for correct prediction of the conduction losses, the dependency of the MOSFET's on-resistance on the junction temperature has to be taken into account and minimization of the thermal resistance between the junctions of all MOSFETs and the ambient is key in order to achieve a high conversion efficiency. This is achieved by means of an optimization of the cooling system which, as autonomous air cooling is one of the system requirements defined in Section 1.3, is implemented using finned heat sinks in combination with fans that blow air through the heat sink channels (i.e. the heat generated by the power devices is subtracted via forced convection cooling). The optimization procedure applied to optimize the heat sink geometry with regard to the total thermal resistance is outlined in Section C.1 of Appendix C. There, the performance of the cooling system used in the final prototype converter as well as the performance of further optimized (keeping the outer dimensions fixed) designs is calculated. Using the presented models, the total losses generated, and the total volume (including the cooling system) occupied by the semiconductors, regarding two heat sink designs (i.e. the one used in the final prototype converter and a second, further optimized, design) and regarding the three ZVS modulation schemes proposed in Chapter 4 (i.e. according to the numerical, the analytical, and the semi-analytical approach), are determined. Note that although the cooling system has a big impact on the losses and on the volume of the system, its design (see Section C.1 of Appendix C) as such is completely independent of the applied DAB modulation scheme.

5.1.1 Semiconductor Selection

The FCH76N60NF SupreMOS® high-voltage super-junction MOSFETs from FAIRCHILD Semiconductor [109] are selected for the active bridges of the DAB while the STY112N65M5 MDmesh^{TM} V power MOSFETs from ST Microelectronics [110] are chosen for the SR[1]. The most relevant device parameters related to this selection are listed in Table 5.1. Of common importance for both the switches of the DAB and of the SR are the maximum blocking voltage V_{DSS}, the maximum

[1]Remind that in this work only Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are considered.

continuous drain current I_{D}, and the maximum continuous drain to source forward current I_{SD} of the body diodes:

- V_{DSS}: The absolute minimum required blocking voltage for the switches of the DAB's secondary side active bridge is approximately equal to the maximum output voltage $V_{\mathrm{DC2,max}} = 470$ V (cf. (3.20)). The absolute minimum required blocking voltage for the switches of the DAB's primary side active bridge and the switches of the SR is approximately equal to the maximum AC line voltage $\hat{V}_{\mathrm{AC,max}} = 358$ V (cf. (3.3)). Note that regarding the blocking voltage of high-voltage MOSFETs it is recommended to consider an additional safety margin of at least 50 to 100 V which takes into account the voltages induced across the parasitic switch and PCB inductances and which therefore adds up to the above minimum values.
- I_{D} and I_{SD}: The minimum required continuous drain current (I_{D}) and continuous drain to source diode forward current (I_{SD}) of a switch is approximately equal to the maximum RMS value of the current that is conducted by the switch. The local (i.e. at a certain time instant within the mains period) RMS values I_{HF1} and I_{HF2} of the DAB bridge currents are depicted in Figures 4.18(b) and 4.18(c) of Section 4.4.2. These values have to be divided by $\sqrt{2}$ in order to find the local RMS value (acc. to (5.5) and (5.6), see later in this section) of the currents conducted by the switches of the respective active bridges. Actually, since the temperature variation of a MOSFET's junction is flattened by thermal capacitances, the worst case equivalent RMS value of the switch current, being defined as the average of the local RMS current (i.e. averaged over a mains period), added by a well-considered safety margin, can be used to determine the minimum required I_{D} and I_{SD}. The same goes for the switches of the SR. The equivalent RMS values of the currents conducted by all switches are derived later in this section (see equations (5.7)-(5.9)).

The MOSFETs in Table 5.1 are selected so that all these requirements are met, including a reasonable safety margin.

Of particular importance for the switches of the DAB (HF switched MOSFETs) are the characteristics that enable a high (soft-) switching performance of the device, being:

- A low total gate charge Q_{g}, leading to reduced turn-on and turn-off times, improved ZVS behavior (fast turn-off) [111], and reduced gate drive losses;
- A highly nonlinear, not too big, parasitic output capacitance C_{oss}, enabling ZVS turn-off (cf. Section 3.3);
- An integrated fast body diode with low reverse recovery charge Q_{rr} and low reverse recovery time t_{rr}, ensuring that all the energy will timely leave the

Quantity	*Value* (FCH76...)	*Value* (STY112...)	*Condition*	*Description*
V_{DSS} (V)	600	650	$T_J = 25°C$	Drain to source voltage
I_D (A)	72.8	96	$T_J = 25°C$	Continuous drain current
I_D (A)	46	61	$T_J = 100°C$	Continuous drain current
$R_{th,J\text{-}C}$ (K/W)	0.23	0.2	–	Thermal resistance, junction to case
$R_{DS(on)}$ (mΩ)	28.7 ($I_D = 38$ A)	19 ($I_D = 48$ A)	$V_{GS} = 10$ V, $T_J = 25°C$	Static drain to source on-resistance (typ.)
I_{SD} (A)	76	96	$T_J = 25°C$	Maximum continuous drain to source diode forward current
Q_g (nC)	230	350	$V_{GS} = 10$ V	Total gate charge (typ.)
Q_{rr} (μC)	1.8 ($I_{SD} = 38$ A)	17 ($I_{SD} = 96$ A)	$V_{GS} = 0$ V	Reverse recovery charge
t_{rr} (ns)	200 ($I_{SD} = 38$ A)	570 ($I_{SD} = 96$ A)	$V_{GS} = 0$ V	Reverse recovery time
	TO-247	Max247	–	Package

Table 5.1: Most relevant parameters of the MOSFETs employed in the DAB (i.e. the FCH76N60NF SupreMOS® high-voltage super-junction MOSFETs from FAIRCHILD [109]) and in the SR (i.e. the STY112N65M5 MDmesh^{TM} V power MOSFETs from ST Microelectronics [110]).

transistor after a switching manouvre. Therewith failures are avoided and repetitive hard commutation (e.g. in case of incorrect timing of the gate signals) is enabled;

- A low drain to source on-resistance $R_{DS(on)}$ and a low junction to case thermal resistance $R_{th,J\text{-}C}$, being highly beneficial regarding the converter's conduction losses.

A good alternative for the FCH76N60NF SupreMOS® high-voltage super-junction MOSFETs from FAIRCHILD are the CoolMOS^{TM} CFD2 super junction MOSFETs from Infineon Technologies AG [111, 112] which are also suitable for hard-switching topologies as they have a high margin in repetitive hard commutation of the body diode.

Of importance for the switches of the SR (LF switched MOSFETs) are especially the characteristics that enable a reduction of the converter's conduction losses, being a low drain to source on-resistance $R_{DS(on)}$ and a low junction to case thermal resistance $R_{th,J\text{-}C}$. The characteristics related to the switching performance of the device are of less importance since the SR's switching devices only change state two times per mains period. The recently introduced STY145N65M5 (also a

MDmesh^{TM} V power MOSFETs from ST Microelectronics [110]) with ultra low on-resistance would even be a better solution than the STY112N65M5 MOSFETs and will be considered in next designs.

5.1.2 Semiconductor Losses

Since the modulation schemes derived in Chapter 4 allow to operate the DAB under ZVS within the entire mains period, switching losses can be neglected in the analysis [39, 64, 68, 92]. Therefore, only conduction losses and the losses of the gate drive units are considered. For the SR also the gate drive losses can be neglected as the MOSFETs of the SR are low frequency switched (100 Hz).

Gate Drive Losses

Assuming an efficiency of 90 % for the gate drive units ($\eta_{\mathrm{gd}} = 0.9$), the total gate drive losses P_{g} related to the eight switches of the DAB[2], and averaged over a full line cycle $T_{\mathrm{L}} = 1/f_{\mathrm{L}}$, are determined with:

$$P_{\mathrm{g}} = 8 \cdot P_{\mathrm{S,g}}, \text{ with} \tag{5.1}$$

$$P_{\mathrm{S,g}} = \frac{1}{\eta_{\mathrm{gd}}} \cdot \frac{Q_{\mathrm{g}}\, \Delta V_{\mathrm{GS}}^2}{\Delta V_{\mathrm{GS,ref}}} \cdot \frac{1}{T_{\mathrm{L}}} \int_0^{T_{\mathrm{L}}} f_{\mathrm{s}}(t)\, \mathrm{d}t, \tag{5.2}$$

where $P_{\mathrm{S,g}}$ are the gate drive losses related to a single switch of the DAB. ΔV_{GS} is the gate to source voltage swing which, as can be seen from Figure 3.18 (top inset), is 18 V for the custom designed gate drive circuits. Note that, for all switches, during the off-state a V_{GS} of -4 V is applied in order to enable fast turn-off and to avoid unwanted turn-on due to coupling effects. During the on-state V_{GS} equals 14 V. Q_{g} is the total (typical) gate charge, measured for a certain reference gate voltage swing $\Delta V_{\mathrm{GS,ref}}$ (for the MOSFETs of the DAB, $Q_{\mathrm{g}} = 230$ nC and $\Delta V_{\mathrm{GS,ref}} = 10$ V, see Table 5.1, FCH76N60NF MOSFETs).

Conduction Losses

The conduction losses of a MOSFET are proportional to the drain to source on-resistance $R_{\mathrm{DS(on)}}$ and to the squared RMS value of the current that is conducted by the switch[3]. Assuming a negligible junction temperature change of the MOSFETs

[2]The gate drive losses related to the switches of the SR can be neglected.

[3]Note that the conduction losses of the internal body diodes can be neglected as they only conduct current during a very small interval of the switching period T_{s}. It is explained in

during a full line cycle T_L, the equivalent (i.e. averaged over T_L) conduction losses of a single MOSFET are determined by:

$$P_{\mathrm{S,cond}} = R_{\mathrm{DS(on)}} \cdot I_{\mathrm{S,eq}}^2, \tag{5.3}$$

where $I_{\mathrm{S,eq}}$ is the equivalent switch RMS current according to:

$$I_{\mathrm{S,eq}} = \sqrt{\frac{1}{T_\mathrm{L}} \int_0^{T_\mathrm{L}} I_\mathrm{S}(t)\,\mathrm{d}t}. \tag{5.4}$$

I_S is the local RMS value of the current conducted by the switch under consideration. For the switches of the primary side active bridge (i.e. active bridge 1, see Figure 3.7), I_S is determined by the primary side bridge current $i_{\mathrm{HF1}}(t)$ while for the switches of the secondary side active bridge (i.e. active bridge 2, see Figure 3.7), I_S is determined by the secondary side bridge current $i_{\mathrm{HF2}}(t)$. In steady-state operation, every switch S_{xx} conducts current during half a switching cycle T_s and the waveforms $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ (e.g. conform Figure 3.10) repeat with negative sign after one half-cycle (i.e. $i_{\mathrm{HF1}}(t+T_\mathrm{s}/2) = -i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t+T_\mathrm{s}/2) = -i_{\mathrm{HF2}}(t)$). Consequently, each of the four switches (S_{11}, S_{12}, S_{13}, and S_{14}) of active bridge 1 carries a local RMS current $I_{\mathrm{S,AB1}}$ and each of the four switches (S_{21}, S_{22}, S_{23}, and S_{24}) of active bridge 2 carries a local RMS current $I_{\mathrm{S,AB2}}$, determined by:

$$I_{\mathrm{S,AB1}} = I_{\mathrm{HF1}}/\sqrt{2}, \tag{5.5}$$

$$I_{\mathrm{S,AB2}} = I_{\mathrm{HF2}}/\sqrt{2}, \tag{5.6}$$

where the local RMS values I_{HF1} and I_{HF2} are respectively calculated with (4.2) and (4.3). The equivalent switch RMS currents, $I_{\mathrm{S,AB1,eq}}$ (switches of active bridge 1) and $I_{\mathrm{S,AB2,eq}}$ (switches of active bridge 2), are thus calculated with:

$$I_{\mathrm{S,AB1,eq}} = \sqrt{\frac{1}{T_\mathrm{L}} \int_0^{T_\mathrm{L}} \frac{I_{\mathrm{HF1}}(t)}{\sqrt{2}}\,\mathrm{d}t}, \tag{5.7}$$

$$I_{\mathrm{S,AB2,eq}} = \sqrt{\frac{1}{T_\mathrm{L}} \int_0^{T_\mathrm{L}} \frac{I_{\mathrm{HF2}}(t)}{\sqrt{2}}\,\mathrm{d}t}. \tag{5.8}$$

As each switch of the SR conducts current during one half of the mains period T_L (acc. to (3.1)), the equivalent RMS value of the current conducted by each SR switch can be approximated with[4]:

Section 3.3.1 that quasi immediately after the body diode is put into conduction, the anti-parallel transistor is turned on, taking over the current.

[4]Note that the HF components of the instantaneous DAB input current i_1 that are not bypassed by the corresponding HF filter capacitance (i.e. C_1, see Figure 3.7), and which thus propagate to the SR, can be neglected for the calculation of the SR's conduction losses.

$$I_{\mathrm{S,SR,eq}} \approx \frac{I_{\mathrm{AC,P}}}{\sqrt{2} \cdot \mathrm{PF}}. \tag{5.9}$$

Before the conduction losses can be calculated using (5.3) and (5.7)-(5.9), the dependency of the MOSFET's drain to source on-resistance on the junction temperature and on the drain to source current has to be modeled. Figure 5.1 depicts these dependencies for the FCH76N60NF MOSFETs used for the active bridges of the DAB. The datasheet characteristics (gray lines) can be described by a 2^{nd} order approximation (black lines) according to:

$$R_{\mathrm{DS(on)}}(T_{\mathrm{J}}) \mid_{I_{\mathrm{D}}=I_{\mathrm{D,ref}}, V_{\mathrm{GS(on)}}=V_{\mathrm{GS(on),ref}}} = a_0 + a_1\, T_{\mathrm{J}} + a_2\, T_{\mathrm{J}}^2, \tag{5.10}$$

$$R_{\mathrm{DS(on)}}(I_{\mathrm{D}}) \mid_{T_{\mathrm{J}}=T_{\mathrm{J,ref}}, V_{\mathrm{GS(on)}}=V_{\mathrm{GS(on),ref}}} = b_0 + b_1\, I_{\mathrm{D}} + b_2\, I_{\mathrm{D}}^2. \tag{5.11}$$

Similarly, a 2^{nd} order approximation can be used to describe the characteristics of the STY112N65M5 MOSFETs used for the SR. The resulting coefficients (a_0, a_1, a_2 and b_0, b_1, b_2) required to evaluate (5.10) and (5.11) for both applied MOSFETs are given in Table 5.2. Note that (5.10) is only valid at a certain reference drain to source current $I_{\mathrm{D,ref}}$ and a certain reference on-state gate voltage $V_{\mathrm{GS(on),ref}}$ while (5.11) is only valid at a certain reference junction temperature $T_{\mathrm{J,ref}}$ and a certain reference on-state gate voltage $V_{\mathrm{GS(on),ref}}$. $T_{\mathrm{J,ref}}$, $I_{\mathrm{D,ref}}$, and $V_{\mathrm{GS(on),ref}}$ are the datasheet reference values as given in Table 5.2. By combining (5.10) and (5.11), a generalized equation can be found which expresses $R_{\mathrm{DS(on)}}$ as a function

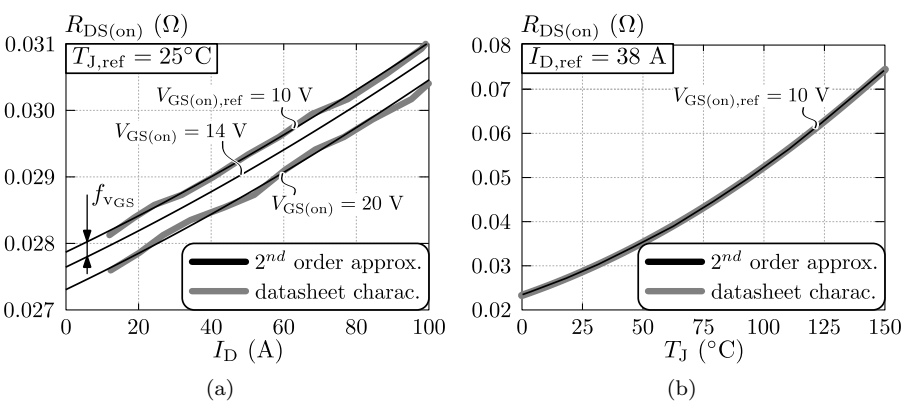


Figure 5.1: Dependency of the drain to source on-resistance $R_{\mathrm{DS(on)}}$ on (a) the drain to source current I_{D} and (b) the junction temperature T_{J}, regarding the FAIRCHILD FCH76N60NF MOSFETs.

	$I_{\mathrm{D,ref}} = 38$ A, $V_{\mathrm{GS(on),ref}} = 10$ V			$T_{\mathrm{J,ref}} = 25°\mathrm{C}$, $V_{\mathrm{GS(on),ref}} = 10$ V		
FCH76N60NF	a_0	a_1	a_2	b_0	b_1	b_2
	$2.33\,e^{-2}$	$1.8921\,e^{-4}$	$1.007\,e^{-6}$	$2.79\,e^{-2}$	$2.6065\,e^{-5}$	$5.3553\,e^{-8}$
	$I_{\mathrm{D,ref}} = 48$ A, $V_{\mathrm{GS(on),ref}} = 10$ V			$T_{\mathrm{J,ref}} = 25°\mathrm{C}$, $V_{\mathrm{GS(on),ref}} = 10$ V		
STY112N65M5	a_0	a_1	a_2	b_0	b_1	b_2
	$1.51\,e^{-2}$	$1.606\,e^{-4}$	$1.2649\,e^{-7}$	$1.79\,e^{-2}$	$2.0204\,e^{-5}$	$3.1405\,e^{-10}$

Table 5.2: Coefficients (a_0, a_1, a_2 and b_0, b_1, b_2) required to evaluate (5.10) and (5.11) (i.e. the 2^{nd} order approximations of the dependency of the drain to source on-resistance $R_{\mathrm{DS(on)}}$ on the junction temperature T_{J} and on the drain to source current I_{D}) for the applied MOSFETs.

FCH76...	α_1	α_2	β_1	β_2	$T_{\mathrm{J,ref}}$	$I_{\mathrm{D,ref}}$
	$8.3587\,e^{-3}$	$3.5136\,e^{-5}$	$1.0402\,e^{-3}$	$1.8487\,e^{-6}$	25°C	38 A
STY112...	α_1	α_2	β_1	β_2	$T_{\mathrm{J,ref}}$	$I_{\mathrm{D,ref}}$
	$8.6966\,e^{-3}$	$6.59\,e^{-6}$	$1.0691\,e^{-3}$	$-1.6643\,e^{-8}$	25°C	48 A

Table 5.3: Coefficients (α_1, α_2 and β_1, β_2) and values for $T_{\mathrm{J,ref}}$ and $I_{\mathrm{D,ref}}$, required to evaluate (5.12) for the applied MOSFETs.

of the deviations ΔT_{J} and ΔI_{D} of respectively the junction temperature T_{J} and the drain to source current I_{D} from the reference junction temperature $T_{\mathrm{J,ref}}$ and the reference drain to source current $I_{\mathrm{D,ref}}$:

$$\begin{aligned} R_{\mathrm{DS(on)}} = \big[& R_{\mathrm{DS(on)}} \,|_{T_{\mathrm{J}}=T_{\mathrm{J,ref}},I_{\mathrm{D}}=I_{\mathrm{D,ref}},V_{\mathrm{GS(on)}}=V_{\mathrm{GS(on),ref}}} \\ & \cdot (1 + \alpha_1\,\Delta T_{\mathrm{J}} + \alpha_2\,\Delta T_{\mathrm{J}}^2) \cdot (1 + \beta_1\,\Delta I_{\mathrm{D}} + \beta_2\,\Delta I_{\mathrm{D}}^2) \big] + f_{\mathrm{vGS}}, \end{aligned} \tag{5.12}$$

with:

$$\Delta T_{\mathrm{J}} = T_{\mathrm{J}} - T_{\mathrm{J,ref}} \qquad \text{and} \qquad \Delta I_{\mathrm{D}} = I_{\mathrm{D}} - I_{\mathrm{D,ref}}. \tag{5.13}$$

$R_{\mathrm{DS(on)}} \,|_{T_{\mathrm{J}}=T_{\mathrm{J,ref}},I_{\mathrm{D}}=I_{\mathrm{D,ref}},V_{\mathrm{GS(on)}}=V_{\mathrm{GS(on),ref}}}$ is the reference datasheet value as listed in Table 5.1. The resulting coefficients (α_1, α_2 and β_1, β_2) for both applied MOSFETs are given in Table 5.3. A displacement term f_{vGS}, determined using linear interpolation (see Figure 5.1(a)), is introduced in order to take into account the dependency of $R_{\mathrm{DS(on)}}$ on the turn-on gate voltage $V_{\mathrm{GS(on)}}$. For the FCH76N60NF MOSFET, and regarding the applied turn-on gate voltage of $V_{\mathrm{GS(on)}} = 14$ V, f_{vGS} was found to be $f_{\mathrm{vGS}} = -2.247\,e^{-4}\ \Omega$. For the STY112N65M5, f_{vGS} could not be calculated due to the absence of information in the datasheet about the gate voltage dependency of $R_{\mathrm{DS(on)}}$, and is assumed to be zero. This leads to a slight (negligible) overestimation of the SR's conduction losses since

with the custom designed gate drive units the on-state gate to source voltage ($V_{\mathrm{GS(on)}} = 14$ V) is higher than $V_{\mathrm{GS(on),ref}} = 10$ V.

In order to calculate the $R_{\mathrm{DS(on)}}$ of a switch, the equivalent RMS value, $I_{\mathrm{S,eq}}$, of the current conducted by the switch has to be substituted into (5.12) (i.e. $\Delta I_{\mathrm{D}} = I_{\mathrm{S,eq}} - I_{\mathrm{D,ref}}$). $I_{\mathrm{S,eq}}$ for the switches of active bridge 1, of active bridge 2, and of the SR are respectively given by (5.7), (5.8), and (5.9). The only quantity that is still missing in order to evaluate (5.12) is the equivalent junction temperature $T_{\mathrm{J,eq}}$ of the switches. It should be reminded that a negligible junction temperature change of the MOSFETs, during a full line cycle T_{L}, is assumed and ΔT_{J} is thus calculated with:

$$\Delta T_{\mathrm{J}} = T_{\mathrm{J,eq}} - T_{\mathrm{J,ref}}, \tag{5.14}$$

where

$$T_{\mathrm{J,eq}} = \sqrt{\frac{1}{T_{\mathrm{L}}} \int_0^{T_{\mathrm{L}}} T_{\mathrm{J}}(t)\,\mathrm{d}t}. \tag{5.15}$$

Expressions for $T_{\mathrm{J,eq}}$ can be obtained by establishing the stationary heat transfer model of the heat sink - semiconductor assembly. The cooling of the switches of the DAB and the switches of the SR is performed using finned heat sinks in combination with fans that blow air through the heat sink channels (i.e. the heat generated by the power devices is subtracted via forced convection cooling). For the two active bridges of the DAB, a heat sink geometry with dual-sided base plate, as shown in Figure C.2(a) of Appendix C, is considered. The DAB's heat sink - semiconductor assembly is depicted in Figure C.1(a) of Appendix C. The four switches of the primary side active bridge (i.e. active bridge 1, see Figure 3.7) are placed in a row and are mounted on the top-side base plate. From the heat transfer perspective and regarding stationary heat transfer, they can be represented by an equivalent power source $P_{\mathrm{AB1,eq}}$ ($= 4 \cdot P_{\mathrm{S1x,eq}}$) which has a power level that is equal to the average losses generated by the four switches during the mains period. The same goes for the four switches of the secondary side active bridge (i.e. active bridge 2, see Figure 3.7) which are mounted on the bottom-side base plate and can be represented by an equivalent power source $P_{\mathrm{AB2,eq}}$ ($= 4 \cdot P_{\mathrm{S2x,eq}}$). For the synchronous rectifier (SR), a heat sink geometry with single-sided base plate is selected, as shown in Figure C.4(a) of Appendix C. The SR's heat sink - semiconductor assembly is depicted in Figure C.1(b) of Appendix C. The four switches of the SR can once more be represented by an equivalent power source $P_{\mathrm{SR,eq}}$ ($= 4 \cdot P_{\mathrm{SSRx,eq}}$). The design and optimization of the heat sink geometries with regard to the total thermal resistance between the surface of the heat sink to the ambient, for both the heat sinks of the DAB and the SR, is extensively described in Section C.1 of Appendix C. The resulting stationary heat transfer model is depicted in Figure 5.2, where

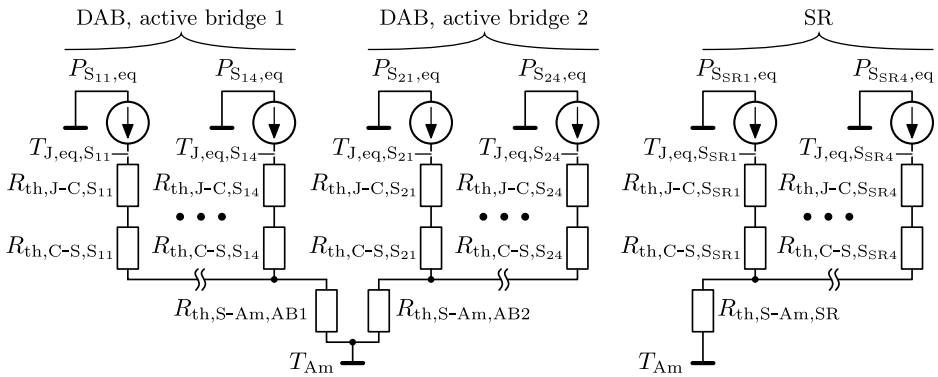


Figure 5.2: Stationary heat transfer model of the complete heat sink - semiconductor assembly of the DAB (left inset) and of the SR (right inset).

- $R_{\text{th,J-C,S}_{xx}}$ are the junction to case thermal resistances of the switches, which are given in Table 5.1 (i.e. $R_{\text{th,J-C}} = 0.23$ W/K for the switches of the DAB and $R_{\text{th,J-C}} = 0.2$ W/K for the switches of the SR);
- $R_{\text{th,C-S,S}_{xx}}$ are the respective thermal resistances between the case of the switches and the surface of the heat sink, i.e. the thermal resistances of the thermal pads[5] (see Figures C.2(a) and C.4(a) of Appendix C);
- $R_{\text{th,S-Am,AB1}}$ and $R_{\text{th,S-Am,AB2}}$ are the thermal resistances between the surface of the heat sink (i.e. the surface of one of the two base plates) to the ambient, for the heat sink of the DAB;
- $R_{\text{th,S-Am,SR}}$ is the thermal resistance between the surface of the heat sink (i.e. the surface of the base plate) to the ambient, for the heat sink of the SR.

$R_{\text{th,C-S}}$ for all switches is defined by:

$$R_{\text{th,C-S}} = \frac{h_{\text{pad}}}{\lambda_{\text{pad}} A_{\text{pad}}}, \tag{5.16}$$

where h_{pad} is the thickness ($h_{\text{pad}} = 1.2\,e^{-4}$ m), λ_{pad} the thermal conductivity ($\lambda_{\text{pad}} = 1.6$ W/mK), and A_{pad} the cross section area of the thermal pads ($A_{\text{pad}} \approx A_{\text{package}} = 3.31\,e^{-4}$ m^2 for the FCH76N60NF MOSFETs and $A_{\text{pad}} \approx A_{\text{package}} = 3.22\,e^{-4}$ m^2 for the STY112N65M5 MOSFETs). $R_{\text{th,S-Am,AB1}}$ ($= R_{\text{th,S-Am,AB2}}$) and $R_{\text{th,S-Am,SR}}$ are obtained from the heat sink optimizations performed in Section C.1 of Appendix C. In these optimizations the heat sink geometries are determined in a

[5]The Hi-Flow 300P thermal pads from Bergquist [113] are used for all switches.

way that, for a given fan and for given outer heat sink dimensions, the total thermal resistance between the surface(s) of the heat sinks and the ambient is minimized. The results are summarized in Table C.2 (three heat sink designs for the DAB) and in Table C.3 (three heat sink designs for the SR) of Appendix C. Note that the considered heat sink material is aluminium. The performance indices and design parameters of the heat sinks used in the final prototype converter (named designs 'A'), which in fact are suboptimal designs since the minimum achievable thickness of the heat sink fins and the minimum achievable channel width[6] were restricted due to limitations of the in-house manufacturing machines/tools, are listed in the top inset of Tables C.2 and C.3. The middle inset of Tables C.2 and C.3 shows the performance indices and design parameters of further optimized designs (named designs 'B'), resulting from an optimization in which a minimum achievable fin thickness and channel width of 1 mm (further referred to as the '1 mm constraint') is assumed. Fin thicknesses and channel widths in the range of 1 mm are enabled by for example using high-end milling machines. Lastly, the bottom inset of Tables C.2 and C.3 shows the performance indices and design parameters of even further optimized designs (named designs 'C'), resulting from an optimization in which a minimum achievable fin thickness and channel width of 0.3 mm (further referred to as the '0.3 mm constraint') is assumed. Fin thicknesses and channel widths in the range of 0.3 mm are enabled by for example using (expensive) electrical discharge machining. $R_{\text{th,S-Am,AB1}}$ ($= R_{\text{th,S-Am,AB2}}$) and $R_{\text{th,S-Am,SR}}$ for designs A (prototype converter) and for designs B (optimized under the '1 mm constraint') are[7]:

- **Designs A (prototype converter):**
  - $R_{\text{th,S-Am,AB1}} = R_{\text{th,S-Am,AB2}} = 0.7298$ K/W;
  - $R_{\text{th,S-Am,SR}} = 1.7264$ K/W;
  - $V_{\text{CS,DAB}} = 0.2917$ (liter, l);
  - $V_{\text{CS,SR}} = 0.0767$ (liter, l);
  - $CSPI_{\text{DAB}} = 9.3907$ (W/K l);
  - $CSPI_{\text{SR}} = 7.5542$ (W/K l);
  - Heat sink material: aluminium.
- **Designs B (optimized under the '1 mm constraint'):**
  - $R_{\text{th,S-Am,AB1}} = R_{\text{th,S-Am,AB2}} = 0.7142$ K/W;
  - $R_{\text{th,S-Am,SR}} = 1.4372$ K/W;
  - $V_{\text{CS,DAB}} = 0.2917$ (liter, l);

[6] The fin thickness (t) and the channel width (s) are defined in Section C.1 of Appendix C.

[7] The heat sinks that are optimized under the '0.3 mm constraint' are considered unfeasible since they require expensive production processes.

- $V_{\mathrm{CS,SR}} = 0.0767$ (liter, l);
- $CSPI_{\mathrm{DAB}} = 9.5967$ (W/K l);
- $CSPI_{\mathrm{SR}} = 9.0741$ (W/K l);
- Heat sink material: aluminium.

V_{CS} is the volume of the cooling system which encompasses the heat sink, the fan, and an airflow inlet between the fan and the heat sink. The volume of the semiconductors themselves is excluded from V_{CS}. $CSPI$ is the cooling system performance index [16, 114, 115] , which is an objective measure that allows to compare different cooling system designs with regard to power density. For the cooling system of the DAB, with dual-sided base plate, $CSPI$ is defined as [114]:

$$CSPI_{\mathrm{DAB}} = \frac{1}{0.5 \cdot R_{\mathrm{th,S\text{-}Am,AB1}} \cdot V_{\mathrm{CS}}} = \frac{1}{0.5 \cdot R_{\mathrm{th,S\text{-}Am,AB2}} \cdot V_{\mathrm{CS}}}. \tag{5.17}$$

The multiplication of $R_{\mathrm{th,S\text{-}Am,AB1}}$ ($= R_{\mathrm{th,S\text{-}Am,AB2}}$) with a factor '0.5' is required since $R_{\mathrm{th,S\text{-}Am,AB1}}$ and $R_{\mathrm{th,S\text{-}Am,AB2}}$ are experienced from just one base plate of the heat sink and thus have to be divided by two in order to take both base plates (top and bottom) into account. For the cooling system of the SR, with single-sided base plate, $CSPI$ is calculated with [115]:

$$CSPI_{\mathrm{SR}} = \frac{1}{R_{\mathrm{th,S\text{-}Am,SR}} \cdot V_{\mathrm{CS}}}. \tag{5.18}$$

Knowing that typical, commercially available heat sink - fan combinations have a $CSPI$ of around 5 [114], the extensive heat sink optimization performed in this work is justified. The achieved $CSPI$ values result in a volume reduction with almost a factor of two compared to the volume of commercially available cooling systems that have the same thermal resistance. Furthermore, custom designed heat sinks allow to fit all converter components into a overall assembly in a more efficient way, leading to higher power densities. Note also that the $CSPI$ values of the cooling systems used in the final prototype converter (designs A) are close to the ones of the designs optimized under the '1 mm constraint' (i.e. designs B).

Referring to Figure 5.2, the (equivalent) junction temperature $T_{\mathrm{J,eq}}$ of a switch can now be expressed as:

$$T_{\mathrm{J,eq}} = T_{\mathrm{Am}} + P_{\mathrm{S,eq}} \cdot (R_{\mathrm{th,J\text{-}C}} + R_{\mathrm{th,C\text{-}S}} + 4 \cdot R_{\mathrm{th,S\text{-}Am}}), \tag{5.19}$$

where, under the assumption that half the gate drive losses of a switch are dissipated in the switch (internally) while the other half is dissipated externally (i.e. in the gate drive units and in the gate resistors),

$$P_{\mathrm{S,eq}} = P_{\mathrm{S,cond}} + \frac{P_{\mathrm{S,g}}}{2}. \tag{5.20}$$

$P_{\mathrm{S,cond}}$ and $P_{\mathrm{S,g}}$ are respectively calculated with (5.3) and (5.2) (for the SR, $P_{\mathrm{S,g}} = 0$, as mentioned above). T_{Am} is the ambient temperature.

At this point all the information that is required in order to calculate the equivalent (i.e. averaged over a line cycle T_{L}) conduction losses $P_{\mathrm{S,cond}}$ (acc. to (5.3)) of all switches is available. Due to the interdependency of the different quantities, a numerical solver needs to be applied in order to solve the equations: $P_{\mathrm{S,cond}} = f(R_{\mathrm{DS(on)}}, \ldots)$, $R_{\mathrm{DS(on)}} = f(T_{\mathrm{J}}, \ldots)$, and $T_{\mathrm{J}} = f(P_{\mathrm{S,cond}}, \ldots)$.

Overview of the Semiconductor Losses

Using the models presented above, below the losses generated by the semiconductor switching devices are calculated for the following scenarios:

1. Heat sink designs A (prototype converter), applying the
   (a) Numerically derived ZVS modulation scheme (cf. Section 4.1);
   (b) Analytically derived ZVS modulation scheme (cf. Section 4.2);
   (c) Semi-analytically derived ZVS modulation scheme (cf. Section 4.3).
2. Heat sink designs B (optimized under the '1 mm constraint'), applying the
   (a) Analytically derived ZVS modulation scheme (cf. Section 4.2).

Scenarios 1(a), 1(b), and 1(c) allow to objectively compare the three different DAB modulation schemes proposed in Chapter 4 with regard to the resulting semiconductor losses. Furthermore, scenario 2(a) can be compared with scenario 1(b) in order to investigate the performance improvement that is possible by replacing the heat sinks used in the prototype converter (i.e. designs A) by further optimized designs, namely the ones optimized under the '1 mm constraint' (i.e. designs B). The results are obtained assuming an ambient temperature of $T_{\mathrm{Am}} = 22°\mathrm{C}$ since this is also the ambient temperate at which the prototype system has been tested (see Chapter 6), and using the MOSFETs listed in Table 5.1. In the figures shown below, the left insets (sub-figures '(a)') show the results for scenarios 1(a), 1(b), and 1(c). The applied modulation schemes are respectively indicated as 'N' (numerical), 'A' (analytical), and 'SA' (semi-analytical). The right insets (sub-figures '(b)') show the results for scenarios 1(b) and 2(a), in which the analytically derived modulation scheme is used. The applied heat sink designs in

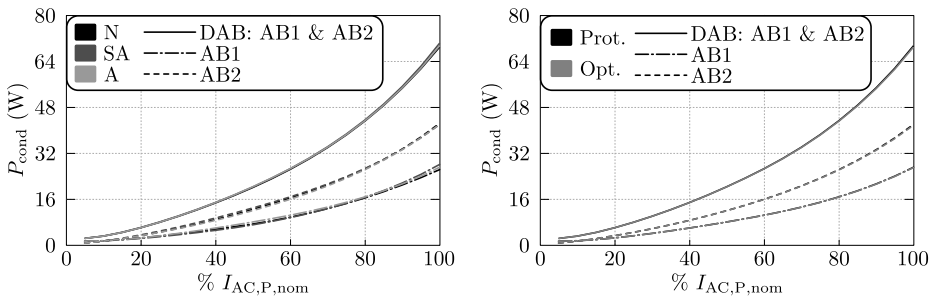


Figure 5.3: Conduction losses generated by the switches of the DAB: (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a).

sub-figures '(b)' are respectively indicated as 'Prot.' (heat sink designs A, prototype converter) and 'Opt.' (heat sink designs B, optimized under the '1 mm constraint').

The different quantities on the y-axes of the figures are depicted as function of the active AC input current $I_{\text{AC,P}}$ (x-axes) which is expressed as percentage of the nominal (active) AC input current $I_{\text{AC,P,nom}} = 16\ \text{A}_{\text{rms}}$. Each figure is obtained for the nominal AC input voltage of $V_{\text{AC}} = V_{\text{AC,nom}} = 230\ \text{V}_{\text{rms}}$ and the nominal DC output voltage of $V_{\text{DC2}} = V_{\text{DC2,nom}} = 400$ V. In order to meet the power factor requirement specified in Table 1.1 of Section 1.3, the applied power factor (PF) is calculated with:

$$\text{PF}(I_{\text{AC,P}}) = 0.983 + (I_{\text{AC,P}} - 0.2\, I_{\text{AC,P,nom}}) \cdot \frac{0.999 - 0.983}{I_{\text{AC,P,nom}} \cdot (1 - 0.2)}. \quad (5.21)$$

Conduction losses of the DAB— Figure 5.3 shows the conduction losses generated by the switches of the DAB. The different loss distributions are indicated as follows:

- Dot dashed lines: total conduction losses for the four switches of active bridge 1 (indicated by 'AB1');
- Dashed lines: total conduction losses for the four switches of active bridge 2 (indicated by 'AB2');
- Solid lines: total conduction losses for all eight switches of the DAB (indicated by 'DAB').

From Figure 5.3(a), regarding scenarios 1(a), 1(b), and 1(c), it can be seen that there is no substantial difference between the three ZVS modulation schemes

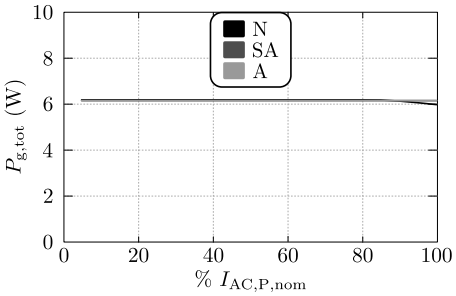


Figure 5.4: Gate drive losses of all the switches of the DAB regarding modulation schemes 'N', 'A', and 'SA'.

with regard to the DAB's semiconductor conduction losses (the loss lines quasi fall together). The numerically derived ZVS modulation scheme ('N') shows a negligible advantage at high power levels compared to the analytically ('A') and the semi-analytically ('SA') derived schemes. This could be expected as the modulation parameters for the numerical approach are optimized with regard to the RMS values of the bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$. The almost equal performance of the three proposed ZVS modulation schemes confirms the conclusion made in Section 4.5, stating that the ZVS constraint functions are the determining factor for the final values of the calculated modulation parameters and that, consequently, the cost function is of less importance in the determination of a ZVS modulation scheme.

From Figure 5.3(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing the DAB's heat sink used in the prototype converter (i.e. design A, indicated by 'Prot.') by a further optimized design, namely the one optimized under the '1 mm constraint' (i.e. design B, indicated by 'Opt.'), the semiconductor conduction losses quasi stay the same (loss lines fall together). This is because the $CSPI$s of the two different DAB cooling system designs ('Prot.' vs. 'Opt.') are almost equal (see above). It can thus be concluded that no substantial performance enhancement can be achieved by using heat sink design B ('Opt.') instead of heat sink design A ('Prot.'), and the heat sink used in the prototype converter to cool the switches of the DAB is close to optimal.

Gate drive losses of the DAB— From Figure 5.4 it can be seen that there is no substantial difference between the three ZVS modulation schemes regarding the gate drive losses. The numerically derived ZVS modulation scheme ('N') shows a negligible advantage at high power levels compared to the analytically ('A') and semi-analytically ('SA') derived schemes since in the high power intervals frequency modulation is applied for the 'N'-scheme (i.e. the switching frequency is lowered).

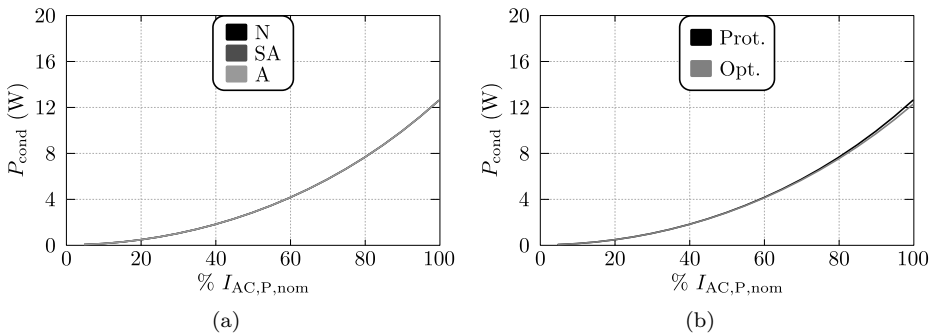


Figure 5.5: Conduction losses generated by the switches of the SR: (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a).

Conduction losses of the SR— The conduction losses of the SR's semiconductors regarding scenarios 1(a), 1(b), and 1(c) are shown in Figure 5.5(a) and are independent of the applied modulation scheme (i.e. the lines for the 'N', the 'SA, and the 'A'-scheme completely fall together). From Figure 5.5(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing the SR's heat sink used in the prototype converter (i.e. design A, indicated by 'Prot.') by a further optimized design, namely the one optimized under the '1 mm constraint' (i.e. design B, indicated by 'Opt.'), no substantial performance enhancement can be achieved. Similar as for the DAB, the heat sink used in the prototype converter to cool the switches of the SR is close to optimal.

Junction Temperatures— Figure 5.6(a) depicts the junction temperatures of all switches (AB1: dot dashed lines, AB2: dashed lines, SR: solid lines) regarding scenarios 1(a), 1(b), and 1(c). As expected, no substantial difference can be noticed between the three ZVS modulation schemes. A bigger difference exists between scenario 1(b) and scenario 2(a) as can be seen from Figure 5.6(b), where the junction temperature of the SR's switching devices is about 5°C lower for heat sink design B compared to heat sink design A (i.e. at the maximum power level). The junction temperatures of the DAB's switching devices on the other hand stay quasi unchanged.

Total semiconductor losses— Figure 5.7(a) depicts the total semiconductor losses regarding regarding scenarios 1(a), 1(b), and 1(c). It can be seen that, all summed up, the difference between the three ZVS modulation schemes is negligible (lines fall together). The same can be said for the difference between the total semiconductor losses obtained with heat sink designs A ('Prot.') and heat sink designs B ('Opt.'), i.e. regarding scenarios 1(b) and 2(a) (see Figure 5.7(b)). It can thus be concluded that, on the one hand, all three proposed modulation schemes perform equally regarding the total semiconductor losses and, on the other hand,

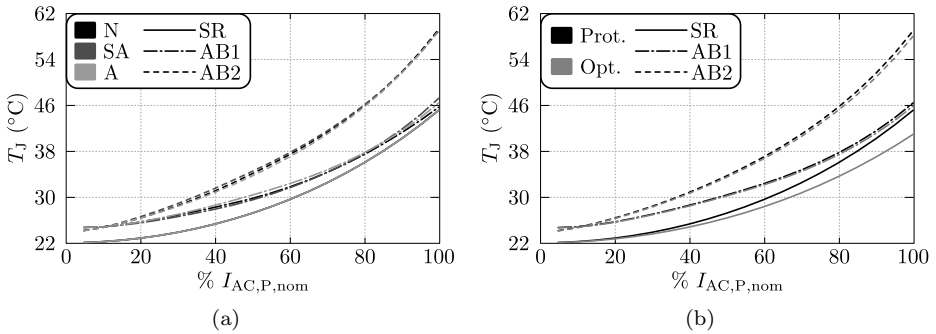


Figure 5.6: Junction temperatures of all semiconductors, i.e. the switches of active bridge 1 (DAB), of active bridge 2 (DAB), and of the SR: (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a).

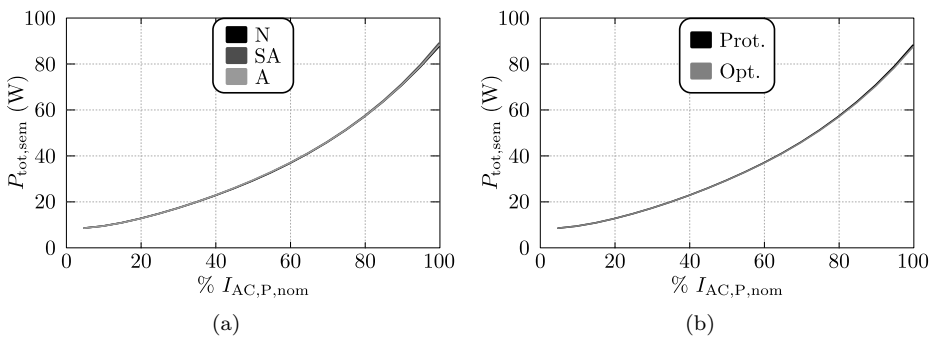


Figure 5.7: Total losses generated by all semiconductors (DAB and SR): (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a).

no noticeable improvement can be achieved by replacing the heat sink designs used in the final prototype converter by the ones optimized under the '1 mm constraint'.

Lastly, in Figure 5.8(a) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.8(b) (scenarios 1(b), 2(a)) the total loss of efficiency $\Delta\eta_{tot,sem}$ (expressed in %) that results from the total semiconductor losses $P_{tot,sem}$ is shown, where $\Delta\eta_{tot,sem}$ is calculated as:

$$\Delta\eta_{tot,sem}(I_{AC,P}) = 100 \cdot \left(1 - \frac{I_{AC,P} \cdot V_{AC,nom} - P_{tot,sem}(I_{AC,P})}{I_{AC,P} \cdot V_{AC,nom}}\right). \quad (5.22)$$

The total loss of efficiency is almost equal for all three modulation schemes ('N', 'A', or 'SA') and for both heat sink designs ('Prot.' versus 'Opt'). It can also be seen

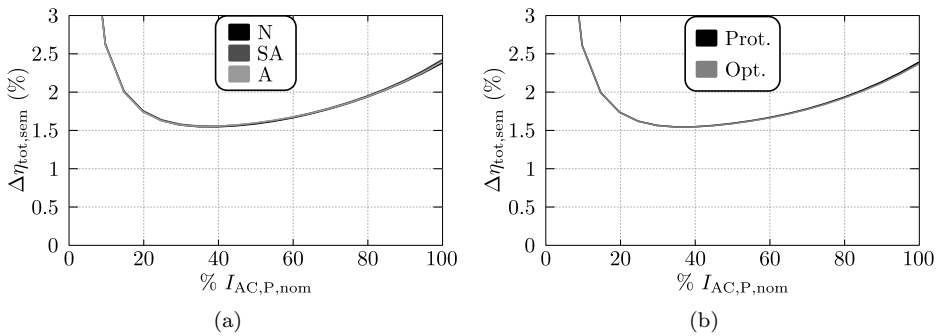


Figure 5.8: Total efficiency loss due to the total losses generated by all semiconductors (DAB and SR): (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a).

that already a significant 'amount' of efficiency is lost in the semiconductors only. It is shown in Section 5.6 that the semiconductors are the biggest loss contributors, which was already assumed in Section 4.1.1 when defining the cost function for the optimization algorithm used to derive a ZVS modulation scheme for the DAB.

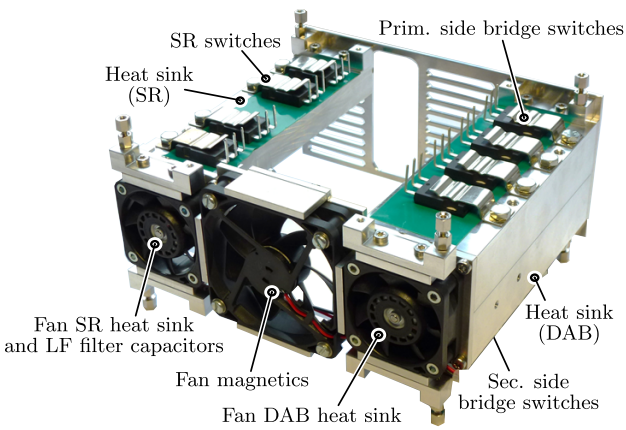


Figure 5.9: Final heat sink - semiconductor assembly (heat sink of the DAB and the SR) of the prototype converter system.

5.1.3 Semiconductor Volume (Incl. Cooling System)

The final heat sink - semiconductor assembly (DAB and SR) is shown in Figure 5.9. The (boxed) volume $V_{\mathrm{CS,tot,DAB}}$ of the DAB's cooling system and the (boxed) volume $V_{\mathrm{CS,tot,SR}}$ of the SR's cooling system are respectively listed in Table C.2 and Table C.3 of Appendix C, i.e. $V_{\mathrm{CS,tot,DAB}} = 0.399$ liter and $V_{\mathrm{CS,tot,SR}} = 0.1227$ liter. Note that $V_{\mathrm{CS,tot,DAB}}$ and $V_{\mathrm{CS,tot,SR}}$ include the heat sink, the fan, the airflow inlet, as also the semiconductor switching devices. Remind (see Section C.1.3 of Appendix C) that the part of the SR's fan that does not faces fins is not included in the calculation of $V_{\mathrm{CS,tot,SR}}$ but is accounted for in the volume calculation of the LF output filter capacitors (see Section 5.3.4), which are also cooled by this fan. The 60 x 60 x 10.5 mm fan in the middle of Figure 5.9 is used to cool the magnetic elements of the DAB, and its volume is accounted for in Section 5.2.5.

5.2 Inductors and Transformer

The DAB DC–DC converter (see Figure 3.7), as the main building block of the investigated 1-S DAB AC–DC converter (see Figure 3.1), consists of three discrete magnetic elements, being:

- The HF AC-link transformer;
- The inductor L_{ext}, which is placed in series with the HF transformer;
- The primary side commutation inductor L_{c1}.

The secondary side commutation inductance L_{c2} is implemented by the magnetizing inductance of the HF AC-link transformer ($L_{\text{c2}} = L_{\text{M}}$), avoiding increased volume and costs. Referring to the equivalent circuit model of the DAB's HF AC-link shown in Figure 2.10, the equivalent inductance value L of the lossless DAB model shown in Figure 3.12 is calculated with:

$$L = L_{\text{ext}} + L_{\text{tr1}} + \left(\frac{n_1}{n_2}\right)^2 \cdot L_{\text{tr2}}, \tag{5.23}$$

where L_{tr1} and L_{tr2} are respectively the primary and secondary side leakage inductances of the transformer. Consequently, the inductance value L_{ext} of the external series inductor can be calculated using 5.23, requiring the transformer to be designed first (i.e. L_{tr1} and L_{tr2} are determined by the final transformer design). Conform Chapter 4, the final design values of the circuit variables L, L_{c1}, L_{c2}, and n_1/n_2 are:

- $L = 13\ \mu\text{H}$;
- $\frac{n_1}{n_2} = 1$;
- $L_{\text{c1}} = L_{\text{c2}} = 62.1\ \mu\text{H}$.

Note that in this work all parasitic elements (e.g. the transformer's and the inductor's coupling capacitances) are neglected. Remind that the equivalent inductance value L serves as the main energy transfer element of the DAB (see Section 2.1.1 of Chapter 2 and Section 3.2.1 of Chapter 3).

5.2.1 Summary of the Design Procedure

In the scope of this work, two optimization algorithms[8] (i.e. one for the inductors and one for the transformer) are developed in order to optimize each magnetic

[8]The detailed implementation of the optimization algorithms is out of the scope of this text.

element with regard to the occupied (boxed) volume and with regard to the losses. Apart from the currents and voltages, losses in inductors and transformers depend on the geometry and the arrangement of the windings, the type of wires, the type of the core, and the geometry and material of the core. The resulting (boxed) volume is mainly determined by the core geometry and the end turns of the windings. For the different optimizations, planar cores are considered because of their advantageous properties with respect the achievable power density and because of their excellent electromagnetic and thermal characteristics [39, 116]. Moreover, the flat geometry of planar cores turns out to fit better in the mechanical design of the converter prototype than other core types such as for example the double U cores used in [117], in particular with regard to the cooling facilities. All possible EELP and EILP core combinations from FERROXCUBE [118] (ferrite core material: 3F3 and 3F4) and EPCOS [119] (ferrite core material: N49, N87, N92, and N97) in the dimensions range from ELP32 up to ELP64 are considered. The number of stacked cores is limited by setting a maximum of 15 cm to the total core length. Litz wires are chosen to reduce eddy current losses in the windings [120–122], being particularly effective at high switching frequencies. A Litz wire consists of a bundle of strands which are individually enamelled and weaved along the entire divided conductor in a way that all wires pass through all points of the bundle's cross section. The total bundle current is then divided equally among the separate strands. Furthermore, four possible winding arrangements are investigated, including split, concentric, hexagonal and orthogonal type windings. Also the paralleling of several Litz bundles, as well as the interleaving (for the transformer design) of the different windings, is implemented in the algorithms. All possible combinations of above mentioned design variables are top level iterated.

With the goal to achieve the required inductance values L_{ext}, L_{c1}, and L_{c2} ($= L_{\mathrm{M}}$), for each iteration in a **first step** the reluctance model R_{m} of the considered magnetic element is calculated according to the methods proposed in [123], which inter alia provides a new analytical approach in order to determine the 3D air gap reluctance $R_{\mathrm{m,air}}$. The inductance values are controlled with the air gap length l_{g}, while guaranteeing that the peak flux density $\hat{B}$ and the air gap length l_{g} do not exceed a predefined maximum value, i.e. $\hat{B}_{\max}$ respectively $l_{\mathrm{g,max}}$. This introduces an upper and a lower limit to the possible number of turns. For the transformer, the minimum and maximum number of turns, i.e. $n_{1,\min}$ respectively $n_{1,\max}$, for the primary side winding are determined by:

$$n_{1,\min} = \mathrm{ciel}\left(\frac{(V\cdot s)_{\mathrm{p,max}}}{2\,\hat{B}_{\max}\,A_{\mathrm{c}}}\right), \tag{5.24}$$

$$n_{1,\max} = \mathrm{floor}\left(\sqrt{L'_{\mathrm{M}}\left(R_{\mathrm{m,core}} + R_{\mathrm{m,air}}\right)\,|_{l_{\mathrm{g}}=l_{\mathrm{g,max}}}}\right), \tag{5.25}$$

where $(V\cdot s)_{\mathrm{p,max}}$ is the maximum Volt-seconds product (primary side of the

transformer), A_c the effective core cross section, $R_{m,core}$ the reluctance of the core, $R_{m,air}$ the reluctance of the air gap, and L_M ($=L_{c2}$) the magnetizing inductance of the transformer (note that $L'_M = (n_1/n_2)^2 \cdot L_M$). The functions 'ciel' and 'floor' respectively represent the round-up and the round-down operation. The number of turns n_1 for the primary side winding of the transformer then needs to be in the range:

$$n_{1,min} \leqslant n_1 \leqslant n_{1,max}. \tag{5.26}$$

Evidently, the number of turns n_2 for the secondary side winding is directly linked to n_1 via the transformer's turns ratio n_1/n_2. For the inductors, the minimum and maximum number of turns, i.e. $n_{ind,min}$ respectively $n_{ind,max}$, are determined by:

$$n_{ind,min} = \text{ciel}\left(\frac{L_{ind}\, i_{ind,max}}{\hat{B}_{max}\, A_c}\right), \tag{5.27}$$

$$n_{ind,max} = \text{floor}\left(\sqrt{L_{ind}\,(R_{m,core} + R_{m,air})\,|_{l_g=l_{g,max}}}\right), \tag{5.28}$$

where $i_{ind,max}$ is the maximum peak inductor current and L_{ind} ($=L_{ext}$ or L_{c1}) the inductance value of the considered inductor. The number of turns n_{ind} for the inductors then needs to be in the range:

$$n_{ind,min} \leqslant n_{ind} \leqslant n_{ind,max}. \tag{5.29}$$

The upper boundary of the maximum allowed operating flux density $\hat{B}_{max}$ is set by the core material saturation flux density[9] B_{sat}, applying a 30 % safety margin in order to achieve low core losses and in order to avoid operation close to saturation. Subsequently, using an inner iteration loop, the number of turns n_1 (transformer) is varied from $n_{1,min}$ to $n_{1,max}$ while the number of turns n_{ind} (inductors) is varied from $n_{ind,min}$ to $n_{ind,max}$. For each inner iteration the air gap length l_g required to achieve the requested inductance value is determined using the above mentioned reluctance models.

In a **second step**, a predefined objective function, which is determined by the total losses (i.e. the core losses and the winding losses) of the magnetic element (inductors/transformer), is minimized for each iteration of the above mentioned design variables. The applied loss models are summarized in Section 5.2.2. The optimization algorithm[10] used to minimize the cost function iterates the number of strands in the Litz bundles, as well as the diameter of the individual strands, in

[9] The core material saturation flux density at a core temperature of 100°C is taken.

[10] The numerical optimization algorithm is implemented in MATLAB™ using the 'fmincon'-function of the Optimization Toolbox™.

order to achieve a window filling that is optimal with regard to the winding losses. Thereby, constraint functions set restrictions on the positioning of the individual Litz bundles by bringing into relation the number of strands, the strand diameter, and wire positioning functions with the given core window area, taking into account creepage distances. This involves functions that describe the dependency of the outer Litz bundle diameter on the number of strands and on the strand diameter. These functions are derived using fitting algorithms that are applied to a database of commercially available Litz wires from the RUPALIT Classic product range of PACK-FEINDRAHTE [124].

In a **third step**, the results obtained from each design iteration/optimization (i.e. the multi-dimensional design space) are mapped into a two-dimensional performance space (i.e. the boxed volume (power density) versus the total losses (efficiency)). The boundary of the feasible performance space, named the Pareto Front, indicates the best possible compromise between the losses and the volume of the magnetic element. The particular design that is located in the corner point of the Pareto Front, and that fits into the final mechanical assembly, is chosen for the final hardware implementation, being a quasi optimal trade-off between efficiency and power density. Note that the Litz wires from the RUPALIT Classic product range of PACK-FEINDRAHTE [124] which are closest (i.e. with respect to the number of strands and the strand diameter) to the results outputted by the optimization algorithms are selected for the final realizations.

5.2.2 Loss Models

In this section, the models used to calculate the winding losses and the core losses of the magnetic elements to be designed are summarized, while referring to the most relevant literature.

Core Losses

For the calculation of the core losses, the improved Generalized Steinmetz Equation (iGSE) [125] has been evaluated as the most accurate state-of-the-art loss model which only requires the Steinmetz material parameters [122, 126]. Core loss calculations with other models, such as the improved improved Generalized Steinmetz Equation (i^{2}GSE) [127], are based on parameters that cannot be extracted from the data provided by the core manufacturers. Therefore, in this work the iGSE is used to estimate the core losses, i.e. no extra characterization of material parameters is required. This method takes into account the losses due to domain wall motion, which is directly related to the time dependency $\mathrm{d}B/\mathrm{d}t$ of the core's flux density. Therefore the iGSE is applicable for non-sinusoidal flux waveforms such is the case for the magnetic components of the DAB, which

experience piecewise-linear flux-time functions. With the iGSE, the core losses per unit volume (index "V") are calculated using the Steinmetz parameters k, α, and β, according to [122, 125]:

$$P_{\mathrm{core,V}} = \frac{1}{T}\int_0^T k_{\mathrm{i}} \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\,\mathrm{d}t, \tag{5.30}$$

where ΔB is the peak-to-peak flux density, while k_{i} is determined by:

$$k_{\mathrm{i}} = \frac{k}{(2\,\pi)^{\alpha-1}\int_0^{2\,\pi} |\cos\theta|^{\alpha}\, 2^{\beta-\alpha}\,\mathrm{d}\theta}. \tag{5.31}$$

The Steinmetz parameters k, α, and β are extracted out of the data provided by the core manufacturers. This data provides information about the core losses per volume (or per weight) as a function of frequency f, peak flux density $\hat{B}$, and temperature T, enabling the extraction of k, α, and β using the empirical Steinmetz Equation $P_{\mathrm{core,V}} = k\, f^{\alpha}\, \hat{B}^{\beta}$, which is valid for sinusoidal excitation only and is thus in agreement with the data provided by the core material datasheets.

Winding Losses

The ohmic losses in the Litz wires (further referred to as Litz bundles) can be separated into skin effect losses P_{S} from self-induced eddy currents inside the conductors, external proximity effect losses $P_{\mathrm{P,e}}$ from eddy currents due to the external magnetic field H_{e} that originates in the air gap fringing field and in the magnetic field from neighboring Litz bundles, and internal proximity effect losses $P_{\mathrm{P,i}}$ from eddy currents due to the internal magnetic field H_{i} that is produced by the bundle itself. The per unit length (index 'L') skin-effect losses (including the DC losses) of a Litz bundle consisting of n_{s} strands, are calculated with [122]:

$$P_{\mathrm{S,L}} = n_{\mathrm{s}} \cdot R_{\mathrm{DC,s,L}} \cdot F_{\mathrm{R}}(f) \cdot \left(\frac{\hat{I}}{n_{\mathrm{s}}}\right)^2, \tag{5.32}$$

where $\hat{I}$ are the Fourier amplitude coefficients of the current time function $i_{\mathrm{b}}(t)$, i.e. regarding the total current $i_{\mathrm{b}}(t)$ in the Litz-wire bundle, at the different harmonic frequencies f. $R_{\mathrm{DC,s,L}}$ is the per unit length DC resistance of a single strand:

$$R_{\mathrm{DC,s,L}} = \frac{4}{\sigma\pi d_{\mathrm{s}}^2}, \tag{5.33}$$

with d_{s} the diameter of the strand and σ the electric conductivity of the conductor material ($\sigma = 5.26 \cdot 10^7$ (1/Ωm) for the considered Litz wires [124]). F_{R} is the

skin-effect factor and is calculated as:

$$F_{\mathrm{R}}(f) = \frac{\xi}{4\sqrt{2}} \cdot \left(\frac{\mathrm{ber}_0(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right), \tag{5.34}$$

with

$$\xi = \frac{d_{\mathrm{s}}}{\sqrt{2}\,\delta}, \tag{5.35}$$

where δ is the skin depth according to:

$$\delta = \frac{1}{\sqrt{\pi\,\mu_0\,\sigma\,f}}. \tag{5.36}$$

μ_0 is the permeability of the conductor material ($\mu_0 = 4\,\pi\,10^{-7}$ H/m for air and copper). The per unit length proximity losses in a Litz bundle are calculated as [122]:

$$\begin{aligned} P_{\mathrm{P,L}} &= P_{\mathrm{P,e,L}} + P_{\mathrm{P,i,L}} \\ &= n_{\mathrm{s}} \cdot R_{\mathrm{DC,s,L}} \cdot G_{\mathrm{R}}(f) \left(\hat{H}_{\mathrm{e}}^2 + \frac{\hat{I}^2}{2\,\pi^2\,d_{\mathrm{b}}^2} \right). \end{aligned} \tag{5.37}$$

G_{R} is the proximity-effect factor and is determined by:

$$G_{\mathrm{R}}(f) = -\frac{\xi\,\pi^2\,d_{\mathrm{s}}^2}{2\sqrt{2}} \cdot \left(\frac{\mathrm{ber}_2(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} + \frac{\mathrm{bei}_2(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right). \tag{5.38}$$

H_{e} is the external magnetic field that originates in the air gap fringing field and in neighboring Litz bundles, and is calculated using the 2D analytical approach proposed in [122]. This approach relies on an imaging and mirroring method in order to inter alia model the impact of a surrounding magnetic conducting material. Thereby the air gap fringing fields are modeled by means of fictitious conductors with eddy currents equal to the magneto-motive force across the air gap. H_{i}, with $\hat{H}_{\mathrm{i}} = \hat{I}^2/(2\,\pi^2\,d_{\mathrm{b}}^2)$, see (5.37), is the internal magnetic field across one strand, which originates in its neighboring strands. For the calculation of H_{i} it is assumed that the current is equally distributed over the Litz bundle's cross-sectional area (note that d_{b} is the diameter of the Litz bundle).

5.2.3 Optimization Results

The results obtained from the optimization of the individual magnetic elements of the DAB, i.e. the two dimensional performance spaces (losses versus volume), are shown in Figure 5.10, where Figure 5.10(a) depicts the performance space for the inductor L_{ext} while the performance space for the HF AC-link transformer is shown in Figure 5.10(b). Note that the optimizations are performed for nominal operating conditions, i.e. at the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.999$, and the nominal output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. The designs that are chosen for the final hardware realization are marked. It should be noted that the performance spaces in Figure 5.10 are calculated using the current-based (CB) ZVS DAB modulation scheme presented in [84], i.e. they are not representative for the final current-dependent charge-based (CDCB) ZVS modulation schemes presented in Chapter 4. This is due to the fact that during the initial design phase of the prototype converter, the influence of the parasitic switch capacitances on the commutation behavior of the DAB's half bridges hadn't been analyzed in detail. In fact, relying on the information available in literature, inter alia in [39], it was assumed that ZVS commutation of a bridge leg is achieved when the drain to source current $i_{\mathrm{DS,S_{xx}}}$ of the switch S_{xx} which initiates the commutation, i.e. the switch which is turned off and causes a state change of the leg, is bigger than or equal to 2 A at the switching instant, $i_{\mathrm{DS,S_{xx}}}(t = t_{\mathrm{turn-off}}) \geqslant 2$ A. Additionally, this assumption made the primary side commutation inductance L_{c1} unnecessary and therefore inductor L_{c1} was even not included in the initial hardware design.

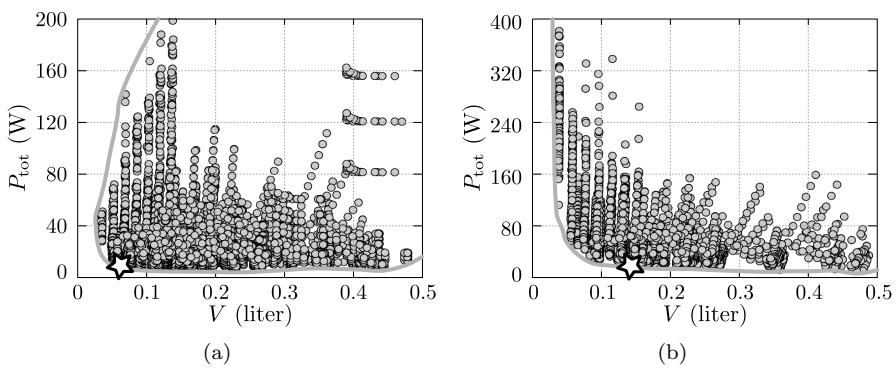


Figure 5.10: Two dimensional performance spaces (losses versus volume) for (a) the inductor L_{ext} and (b) the HF AC-link transformer used in the prototype converter. The performance spaces are calculated for nominal operating conditions, using the CB ZVS modulation scheme presented in [84], yielding sub-optimal conditions with regard to the CDCB ZVS modulation schemes presented in Chapter 4.

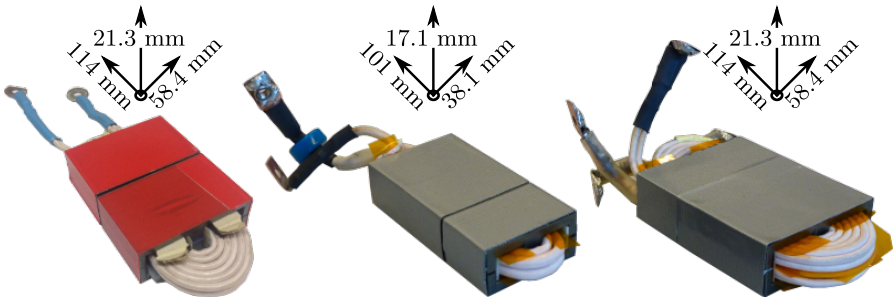


Figure 5.11: Hardware realizations of the three magnetic elements of the DAB converter, being the primary side commutation inductor L_{c1} (left inset) and the main inductor L_{ext} (middle inset), which is placed in series with the HF AC-link transformer (right inset).

Only after the first testing and after facing multiple device failures it became clear that an extensive analysis of the commutation behavior was essential, leading to the development of the CDCB ZVS verification method proposed in Section 3.3.2 and subsequently to the CDCB ZVS modulation schemes presented in Chapter 4. Consequently, with the CDCB ZVS modulation schemes, the currents and voltage of the magnetic elements are substantially different than with the initial CB ZVS modulation scheme. As a result, compared to the initial design, the inductance values and thus the air gap lengths had to be adapted[11] accordingly. Furthermore, the addition of a primary side commutation inductor L_{c1} turned out to be essential. However, the realization of L_{c1} was simply done by duplicating the HF AC-link transformer design, removing one of the two windings, and adapting the air gap length according to the calculated inductance value L_{c1}. All this makes that the designs of the inductors L_{ext} and L_{c1}, and of the HF AC-link transformer, used in the final prototype converter are non-optimal. These designs are further referred to as designs 'A' and their design values are listed in Tables 5.4-5.6. Figure 5.11 depicts the corresponding hardware realizations.

In order to investigate the performance enhancement that can be achieved by replacing magnetic designs A (prototype converter) by further optimized designs, the optimization of all magnetic elements is repeated (again at nominal operating conditions) using the (correct), analytically derived CDCB ZVS modulation scheme presented in Section 4.2. Thereby, the core dimensions of both the inductor L_{ext} and of the HF AC-link transformer are taken the same as for inductor/transformer designs A, enabling simple replacement by the optimized designs. Figure 5.12(a) depicts the new performance space for the inductor L_{ext} while the new performance

[11] Note that it was verified if the new air gap lengths and the resulting peak flux densities $\hat{B}$ do not exceed the predefined maximum values, i.e. $l_{g,max}$ respectively $\hat{B}_{max}$.

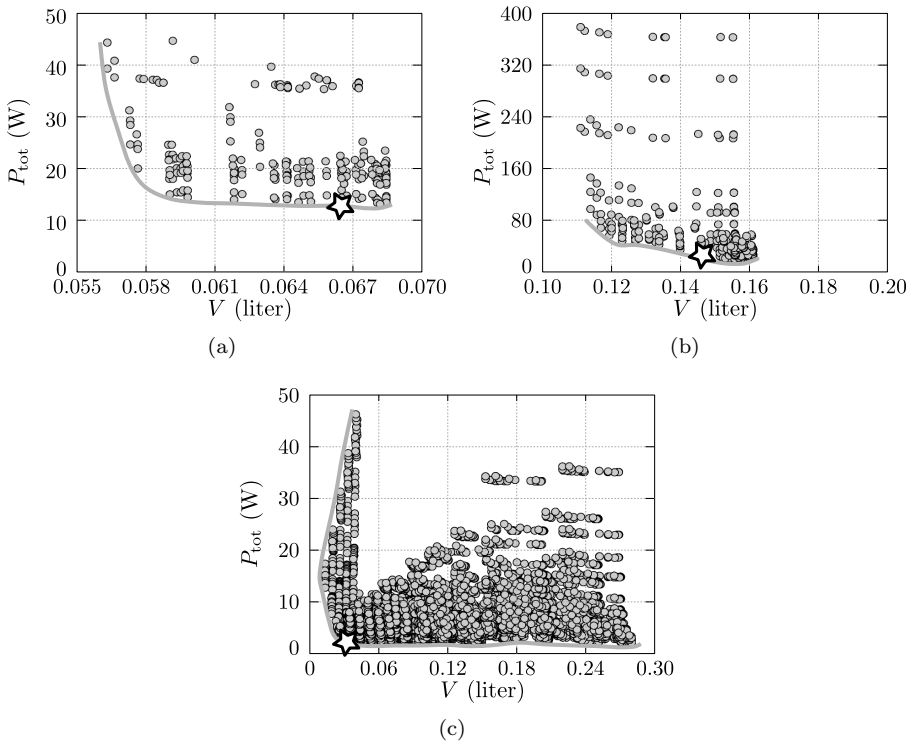


Figure 5.12: Two dimensional performance spaces (losses versus volume) for (a) the inductor $L_{\rm ext}$, (b) the HF AC-link transformer, and (c) the primary side commutation inductor $L_{\rm c1}$. The spaces are calculated for nominal operating conditions, using the analytically derived CDCB ZVS modulation scheme presented in Section 4.2.

space for the HF AC-link transformer is shown in Figure 5.12(b). Due to the fact that the core dimensions are fixed to the ones for designs A, the volume range in Figures 5.12(a) and 5.12(b) is very narrow (i.e. the volume only changes due to the changing dimensions of the winding's end turns). For the primary side commutation inductor $L_{\rm c1}$, however, the optimization is performed using all degrees of freedom, i.e. also the core dimensions are iterated during the optimization run. Figure 5.12(c) depicts the new performance space for the inductor $L_{\rm ext}$, evidently showing a much wider volume range. The new, optimal designs of the magnetic elements selected for comparison with the initial designs A are marked in Figure 5.12 and are further referred to as designs 'B'. Their design values are also listed in Tables 5.4-5.6. A comprehensive performance evaluation, i.e. regarding the losses, of both magnetic designs A and designs B is given below.

Variable	*Design A (prot.)*	*Design B (opt.)*	*Description*
n_{ind}	4	4	number of turns
L_{ind} (μH)	12.2	12.3	inductance value
l_{g} (mm)	0.603	0.602	air gap length
n_{s}	1458	1302	number of strands in a Litz bundle
d_{s} (μm)	71	80	strand diameter
N_{par}	1	1	number of paralleled Litz bundles
	N97	N97	core material
	EELP38	EELP38	core type/combination
	3	3	number of stacked core combinations
$l_{\mathrm{core,tot}}$ (m)	0.076	0.076	total core length
V_{ind} (liter, l)	0.0661	0.0666	boxed volume of the inductor

Table 5.4: Design values for the main inductor L_{ext}, i.e. regarding design 'A' (prototype converter) and design 'B' (further optimized).

Variable	*Design A (prot.)*	*Design B (opt.)*	*Description*
n_{ind}	6	13	number of turns
L_{ind} (μH)	62.1	62.1	inductance value
l_{g} (mm)	0.234	0.92	air gap length
n_{s}	700	184	number of strands in a Litz bundle
d_{s} (μm)	80	50	strand diameter
N_{par}	2	2	number of paralleled Litz bundles
	N97	N97	core material
	EELP58	EELP32	core type/combination
	2	3	number of stacked core combinations
$l_{\mathrm{core,tot}}$ (m)	0.076	0.061	total core length
V_{ind} (liter, l)	0.143	0.0358	boxed volume of the inductor

Table 5.5: Design values for the primary side commutation inductor L_{c1}, i.e. regarding design 'A' (prototype converter) and design 'B' (further optimized).

5.2.4 Losses in the Inductors and Transformer

Using the models presented above, below the losses in inductors L_{ext} and L_{c1}, and in the HF AC-link transformer are calculated for the following scenarios:

1. Inductor/transformer designs A (prototype converter), applying the
   (a) Numerically derived ZVS modulation scheme (cf. Section 4.1);

Variable	*Design A (prot.)*	*Design B (opt.)*	*Description*
n_1/n_2	1	1	turns ratio
n_1	6	6	number of turns (primary side winding)
n_2	6	6	number of turns (secondary side winding)
L_{tr1} (μH)	0.76	0.69	primary side leakage inductance
L_{tr2} (μH)	0.76	0.69	secondary side leakage inductance
$L_{\mathrm{M}} = L_{\mathrm{c2}}$ (μH)	62.1	62.1	magnetizing inductance, which is equal to the secondary side commutation inductance
l_{g} (mm)	0.234	0.234	air gap length
$n_{\mathrm{s},1}$	700	812	number of strands in a Litz bundle (primary side winding)
$n_{\mathrm{s},2}$	700	812	number of strands in a Litz bundle (secondary side winding)
$d_{\mathrm{s},1}$ (μm)	80	71	strand diameter (primary side winding)
$d_{\mathrm{s},2}$ (μm)	80	71	strand diameter (secondary side winding)
$N_{\mathrm{par},1}$	2	2	number of paralleled Litz bundles (primary side winding)
$N_{\mathrm{par},2}$	2	2	number of paralleled Litz bundles (secondary side winding)
	no interleaving		interleaving of the windings
	N97	N97	core material
	EELP58	EELP58	core type/combination
	2	2	number of stacked core combinations
$l_{\mathrm{core,tot}}$ (m)	0.076	0.076	total core length
V_{trans} (liter, l)	0.143	0.143	boxed volume of the transformer

Table 5.6: Design values for the HF AC-link transformer, i.e. regarding design 'A' (prototype converter) and design 'B' (further optimized).

   (b) Analytically derived ZVS modulation scheme (cf. Section 4.2);
   (c) Semi-analytically derived ZVS modulation scheme (cf. Section 4.3).

2. Inductor/transformer designs B (further optimized), applying the
   (a) Analytically derived ZVS modulation scheme (cf. Section 4.2).

Scenarios 1(a), 1(b), and 1(c) allow to objectively compare the three different DAB modulation schemes proposed in Chapter 4 with regard to the losses in the inductors and in the HF AC-link transformer. Furthermore, scenario 2(a) can be compared with scenario 1(b) in order to investigate the performance improvement that is possible by replacing the inductors/transformer used in the prototype converter (i.e. designs A) by further optimized designs (i.e. designs B). In the

figures show below, the left insets (sub-figures '(a)' and '(c)') show the results for scenarios 1(a), 1(b), and 1(c). The applied modulation schemes are respectively indicated as 'N' (numerical), 'A' (analytical), and 'SA' (semi-analytical). The right insets (sub-figures '(b)' and '(d)') show the results for scenarios 1(b) and 2(a), in which the analytically derived modulation scheme is used. The applied designs in sub-figures '(b)' and '(d)' are respectively indicated as 'Prot.' (designs A, prototype converter) and 'Opt.' (designs B, further optimized).

The different quantities on the y-axes of the figures are depicted as function of the active AC input current $I_{\mathrm{AC,P}}$ (x-axes), which is expressed as percentage of the nominal (active) AC input current $I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$. Each figure is obtained for the nominal AC input voltage of $V_{\mathrm{AC}} = V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$ and the nominal DC output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. In order to meet the power factor requirement specified in Table 1.1 of Section 1.3, the applied power factor (PF) is calculated with (5.21).

Inductor L_{ext}— Figure 5.13(a) shows the winding losses (dashed lines), the core losses (dot-dashed lines), and the total losses (solid lines) in the main inductor L_{ext}. It can be seen that there is no substantial difference between the three modulation schemes with regard to the losses in L_{ext} (the loss lines quasi fall together). The numerically derived ZVS modulation scheme ('N') shows a negligible advantage at high power levels compared to the analytically ('A') and the semi-analytically ('SA') derived schemes.

From Figure 5.13(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing the inductor used in the prototype converter (i.e. design A, indicated by 'Prot.') by a further optimized design (i.e. design B, indicated by 'Opt.'), the losses quasi stay the same (loss lines fall together). Consequently, no substantial performance enhancement can be achieved by using inductor design B ('Opt.') instead of inductor design A ('Prot.'). Note that for both designs, the boxed volume is equal, see Table 5.4.

Figure 5.13(c) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.13(d) (scenarios 1(b), 2(a)) show the total loss of efficiency $\Delta\eta_{\mathrm{Lext}}$ (expressed in %) that results from the total losses in the main inductor L_{ext}, where $\Delta\eta_{\mathrm{Lext}}$ is calculated as:

$$\Delta\eta_{\mathrm{Lext}}(I_{\mathrm{AC,P}}) = 100 \cdot \left(1 - \frac{I_{\mathrm{AC,P}} \cdot V_{\mathrm{AC,nom}} - P_{\mathrm{tot,Lext}}(I_{\mathrm{AC,P}})}{I_{\mathrm{AC,P}} \cdot V_{\mathrm{AC,nom}}}\right). \tag{5.39}$$

It can once more be concluded that the applied modulation scheme ('N', 'A', or 'SA'), as well as the applied inductor design ('Prot.' or 'Opt') have quasi no impact on the total losses in the main inductor L_{ext} and thus on the efficiency loss due to these losses.

Inductor L_{c1}— Figure 5.14(a) shows the winding losses (dashed lines), the core losses (dot-dashed lines), and the total losses (solid lines) in the primary side

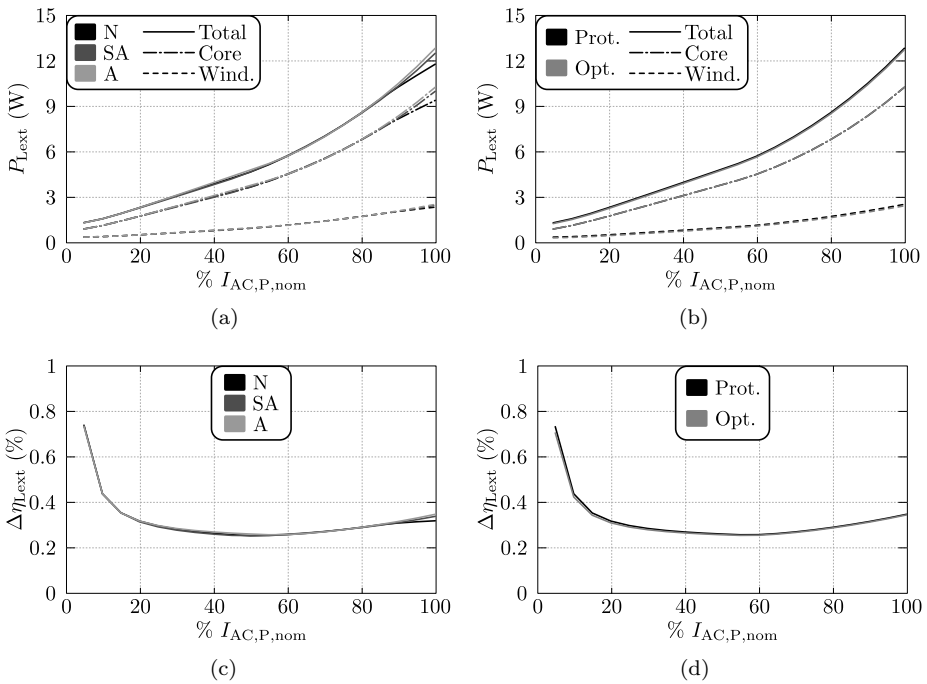


Figure 5.13: (a)-(b) Losses in the main inductor L_{ext}, (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a). (c)-(d) Efficiency loss due to the total losses in the main inductor L_{ext}, (c) according to scenarios 1(a), 1(b), and 1(c); (d) according to scenarios 1(b) and 2(a).

commutation inductor L_{c1}. It can be seen that there is no substantial difference between the three modulation schemes with regard to the losses in L_{c1} (the loss lines quasi fall together). The analytically derived ZVS modulation scheme ('A') shows a minor advantage, both at low and at high power levels, compared to the numerically ('N') and the semi-analytically ('SA') derived schemes.

From Figure 5.14(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing the inductor used in the prototype converter (i.e. design A, indicated by 'Prot.') by a further optimized design (i.e. design B, indicated by 'Opt.'), the losses are substantially reduced. This can be explained by the fact that the hardware realization of L_{c1} (prototype converter) was simply done by duplicating the HF AC-link transformer design, removing one of the two windings, and adapting the air gap length according to the required inductance value L_{c1}. Consequently, a noticeable performance enhancement can be achieved by using inductor design B ('Opt.') instead of inductor design A ('Prot.'). Note that by doing so, also a considerable volume reduction is achieved (see Table 5.5).

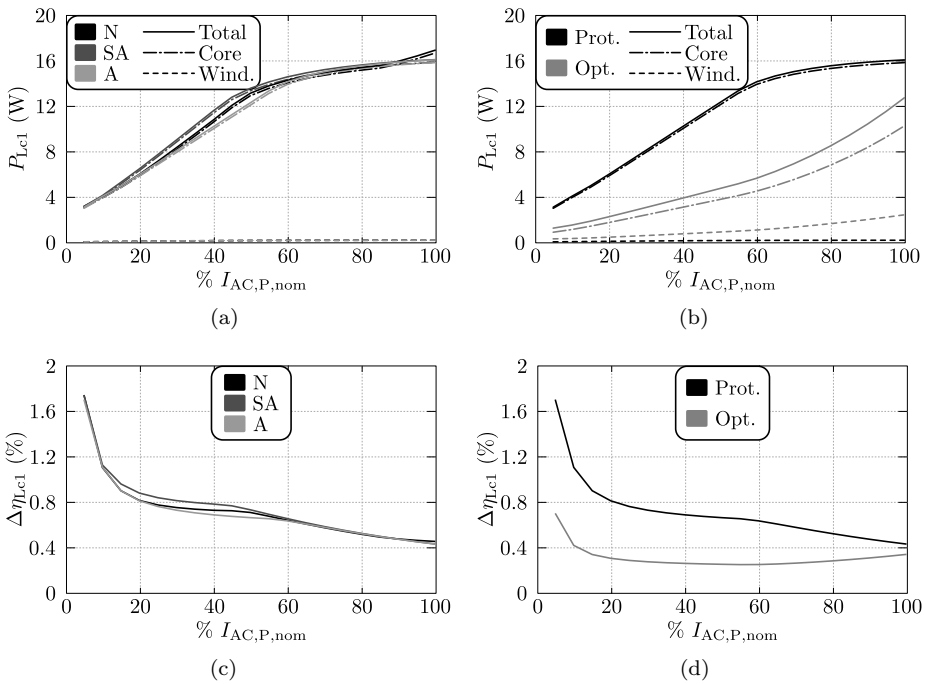


Figure 5.14: (a)-(b) Losses in the primary side commutation inductor L_{c1}, (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a). (c)-(d) Efficiency loss due to the total losses in the primary side commutation inductor L_{c1}, (c) according to scenarios 1(a), 1(b), and 1(c); (d) according to scenarios 1(b) and 2(a).

Figure 5.14(c) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.14(d) (scenarios 1(b), 2(a)) show the total loss of efficiency $\Delta\eta_{Lc1}$ (expressed in %) that results from the total losses in the primary side commutation inductor L_{c1}. It can once more be concluded that the applied modulation scheme ('N', 'A', or 'SA') has only a small impact on the total losses in L_{c1}, and thus on the efficiency loss due to these losses (see Figure 5.14(c)). However, the applied inductor design ('Prot.' or 'Opt') has a great impact on the losses in L_{c1}, and thus on the efficiency loss due to these losses (see Figure 5.14(d)). It is thus appropriate to replace inductor design A by inductor design B.

HF AC-link transformer— Figure 5.15(a) shows the winding losses (dashed lines), the core losses (dot-dashed lines), and the total losses (solid lines) in the HF AC-link transformer. It can be seen that there is no substantial difference between the three modulation schemes with regard to the losses in the transformer (the loss lines quasi fall together). The analytically derived ZVS modulation scheme ('A')

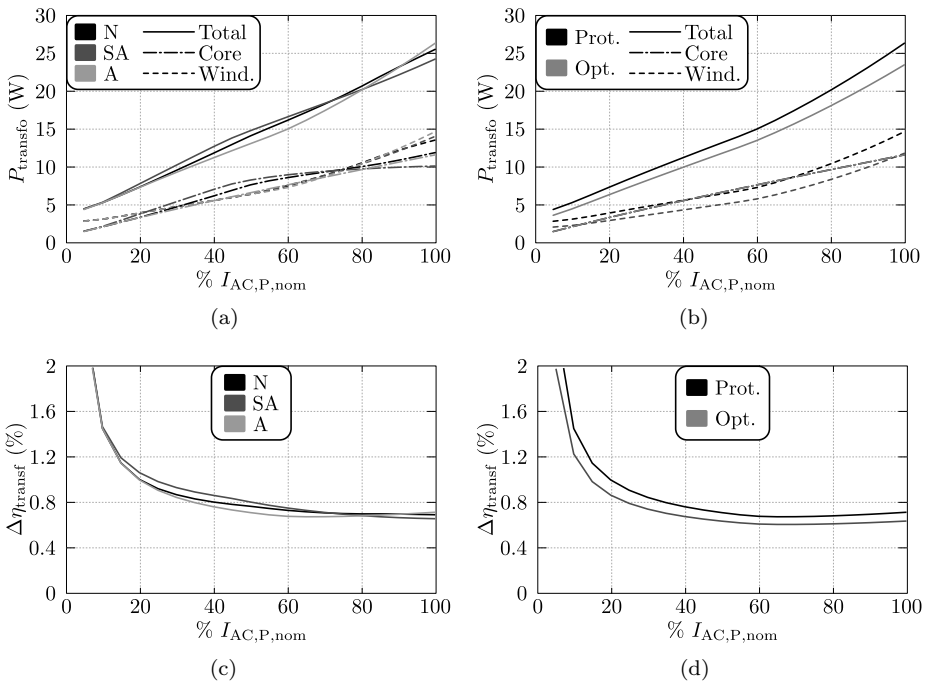


Figure 5.15: (a)-(b) Losses in the HF AC-link transformer, (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a). (c)-(d) Efficiency loss due to the total losses in the HF AC-link transformer, (c) according to scenarios 1(a), 1(b), and 1(c); (d) according to scenarios 1(b) and 2(a).

shows a minor advantage at low power levels while the semi-analytically ('SA') derived ZVS modulation scheme shows a slight advantage at high power levels.

From Figure 5.15(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing the transformer used in the prototype converter (i.e. design A, indicated by 'Prot.') by a further optimized design (i.e. design B, indicated by 'Opt.'), a more pronounced loss reduction is achieved. Note that for both designs, the volume is equal, see Table 5.6.

Figure 5.15(c) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.15(d) (scenarios 1(b), 2(a)) show the total loss of efficiency $\Delta\eta_{\text{transf}}$ (expressed in %) that results from the total losses in the HF AC-link transformer. It can once more be concluded that the applied modulation scheme ('N', 'A', or 'SA') has only a small impact on the total losses in the transformer, and thus on the efficiency loss due to these losses (see Figure 5.15(c)). However, the applied transformer design ('Prot.' or 'Opt') has a bigger impact on the transformer losses, and thus on the efficiency loss due

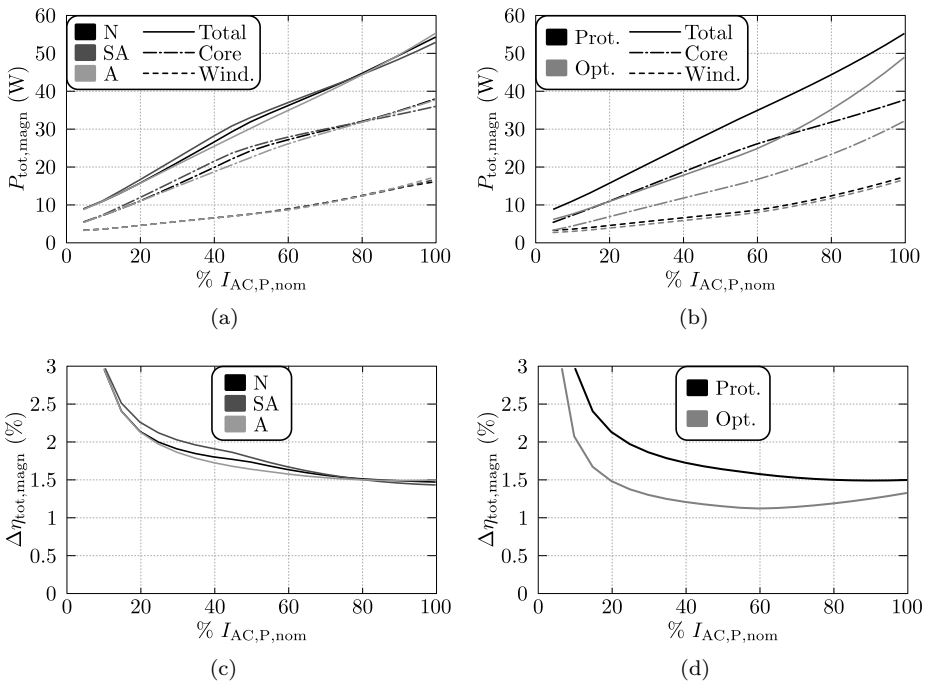


Figure 5.16: (a)-(b) Total losses in all magnetic elements of the DAB, (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a). (c)-(d) Efficiency loss due to the total losses in all magnetic elements of the DAB, (c) according to scenarios 1(a), 1(b), and 1(c); (d) according to scenarios 1(b) and 2(a).

to these losses (see Figure 5.15(d)). It might be appropriate to replace transformer design A by transformer design B.

Total losses— Figure 5.16(a) shows the summed winding losses (dashed lines), core losses (dot-dashed lines), and total losses (solid lines) in all the magnetic elements of the DAB. It can be seen that there is no substantial difference between the three modulation schemes with regard to the total losses in the magnetics (the loss lines quasi fall together). The analytically derived ZVS modulation scheme ('A') shows a minor advantage at low power levels while the semi-analytically ('SA') derived ZVS modulation scheme shows a slight advantage at high power levels.

From Figure 5.16(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing all magnetic designs A (prototype converter, indicated by 'Prot.') by magnetic designs B (further optimized, indicated by 'Opt.'), a substantial loss reduction is achieved, which is mainly due to the improved design of the primary

	$\hat{B}$ (mT), L_{ext}		$\hat{B}$ (mT), L_{c1}		$\hat{B}$ (mT), transf.	
	Design A	Design B	Design A	Design B	Design A	Design B
N	207.8	-	258.7	-	272.3	-
SA	207	-	119.4	-	189.2	-
A	206.6	206.6	189.2	134.7	219.5	219.5

Table 5.7: Peak flux densities $\hat{B}$ in all the magnetic elements of the DAB, calculated for the different modulation schemes and regarding magnetic designs A (prototype converter) and B (further optimized).

side commutation inductor L_{c1}, also resulting in a noticeable volume reduction (see Table 5.5).

Figure 5.16(c) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.16(d) (scenarios 1(b), 2(a)) show the total loss of efficiency $\Delta\eta_{\text{tot}}$ (expressed in %) that results from the total losses in all magnetic elements of the DAB. It can once more be concluded that the applied modulation scheme ('N', 'A', or 'SA') has only a small impact on the total losses in the magnetics, and thus on the efficiency loss due to these losses (see Figure 5.16(c)). However, the applied magnetic designs ('Prot.' or 'Opt') have a substantial impact on the total losses and thus on the efficiency loss due to these losses (see Figure 5.16(d)). Especially the replacement of the primary side commutation inductor L_{c1} is appropriate.

For completeness, the peak flux densities $\hat{B}$ in all the magnetic elements of the DAB, calculated for the different modulation schemes and regarding magnetic designs A (prototype converter) and B (further optimized), are listed in Table 5.7. It is clear that these values are all below the maximum allowed operating flux density $\hat{B}_{\text{max}}$, being defined as $\hat{B}_{\text{max}} = 0.7 \cdot B_{\text{sat,100°C}} = 0.7 \cdot 410 = 287$ mT for the employed magnetic material (i.e. N97 from EPCOS).

5.2.5 Volume of the Inductors and Transformer

The boxed volumes of the inductors and the HF AC-link transformer regarding designs A (prototype converter) and designs B (further optimized) are listed in Tables 5.4-5.6:

- Main inductor L_{ext}: $V_{\text{ind}} = 0.0661$ liter (design A and design B);
- Primary side commutation inductor L_{c1}: $V_{\text{ind}} = 0.143$ liter for design A and $V_{\text{ind}} = 0.0358$ liter for design B;
- HF AC-link transformer: $V_{\text{trans}} = 0.143$ (design A and design B).

The 60 x 60 x 10.5 mm fan (BISONIC, 12V DC, type BP601012M-W) in the middle of Figure 5.9 is used to cool the magnetic elements of the DAB, having a boxed volume of 0.0378 liter.

5.2.6 Remarks

The subject of further investigation/optimization might be to consider a T-type instead of a Pi-type equivalent circuit of the HF AC-link, which allows integration of the main inductor L_{ext} and the primary side commutation inductor L_{c1} by effectively using/tailoring the transformer's leakage inductances in order to obtain the same circuit behavior [102–104, 128]. Furthermore, at present, a thermal model for the magnetic elements, based on an extensive nodal network [116, 129], is under development. Consequently, the thermal behavior, as well as the influence of the temperature on the losses of the magnetics, could not be verified in advance. Nevertheless, temperature measurements (thermal camera) are performed during stationary converter operation at full power, showing 'safe' operating temperatures of less than 90°C.

5.3 Output Filter Capacitors

5.3.1 LF Output Filter Capacitors

Since the DAB handles the double line frequency component of the input power, a low-frequency (LF) filter capacitor $C_{2,\mathrm{st}}$ (see Figure 3.1) is placed at the converter's DC output side in order to limit the output voltage ripple by smoothing the inherent energy flow variation. Assuming unity power factor control, i.e. PF = 1, where the input current $i_{\mathrm{AC}}(t)$ is directly proportional to the input voltage $v_{\mathrm{AC}}(t)$, the output power (i.e. before $C_{2,\mathrm{st}}$) of the 1-S DAB AC–DC converter can be written as:

$$\begin{aligned} p_{\mathrm{DC2}}(t) &= \eta\, v_{\mathrm{AC}}(t)\, i_{\mathrm{AC}}(t) = \eta\, V_{\mathrm{AC}}\, I_{\mathrm{AC}} \cdot (1 - \cos(2\,\omega_{\mathrm{L}}\, t)), \\ &= P_{\mathrm{DC2}} \cdot (1 - \cos(2\,\omega_{\mathrm{L}}\, t)), \end{aligned} \tag{5.40}$$

where η is the total conversion efficiency and $\omega_{\mathrm{L}} = 2\,\pi\, f_{\mathrm{L}}$ the angular frequency of the mains. $p_{\mathrm{DC2}}(t)$ thus consists of a constant power component P_{DC2} which is aimed for the load, and a time varying, 100 Hz power component $\tilde{p}_{\mathrm{DC2}}(t) = -P_{\mathrm{DC2}} \cdot \cos(2\,\omega_{\mathrm{L}}\, t)$ which is delivered to $C_{2,\mathrm{st}}$ when $p_{\mathrm{DC2}}(t) > P_{\mathrm{DC2}}$ and which is delivered by $C_{2,\mathrm{st}}$ when $p_{\mathrm{DC2}}(t) < P_{\mathrm{DC2}}$. Under the assumption of a constant output voltage V_{DC2}, the capacitor current $i_{\mathrm{C}_{2,\mathrm{st}}}(t)$ can be calculated as:

$$i_{\mathrm{C}_{2,\mathrm{st}}}(t) \approx \frac{\tilde{p}_{\mathrm{DC2}}(t)}{V_{\mathrm{DC2}}} = \frac{-P_{\mathrm{DC2}} \cdot \cos(2\,\omega_{\mathrm{L}}\, t)}{V_{\mathrm{DC2}}}. \tag{5.41}$$

With $i_{\mathrm{C}_{2,\mathrm{st}}}(t) = C_{2,\mathrm{st}} \cdot \mathrm{d}\tilde{V}_{\mathrm{DC2}}(t)/\mathrm{d}t$, the output voltage ripple $\tilde{V}_{\mathrm{DC2}}(t)$ becomes:

$$\begin{aligned} \tilde{V}_{\mathrm{DC2}}(t) &= \frac{1}{C_{2,\mathrm{st}}} \int i_{\mathrm{C}_{2,\mathrm{st}}}(t)\mathrm{d}t \\ &= \frac{-P_{\mathrm{DC2}} \cdot \sin(2\,\omega_{\mathrm{L}}\, t)}{2\,\omega_{\mathrm{L}}\, C_{2,\mathrm{st}}\, V_{\mathrm{DC2}}}. \end{aligned} \tag{5.42}$$

As a result, the amplitude of the output voltage ripple equals:

$$\hat{\tilde{V}}_{\mathrm{DC2}} = \frac{P_{\mathrm{DC2}}}{2\,\omega_{\mathrm{L}}\, C_{2,\mathrm{st}}\, V_{\mathrm{DC2}}}. \tag{5.43}$$

In the final hardware prototype, the LF output filter capacitance $C_{2,\mathrm{st}}$ is realized using three 390 μF, 500 V DC, electrolytic capacitors (ELCOs), type EETED2W391EA, from Panasonic [130], which are placed in parallel. This leads to a total LF output filter capacitance value of $C_{2,\mathrm{st}} = 1170$ μF. For

nominal conditions, i.e. $V_{\mathrm{AC}} = V_{\mathrm{AC,nom}} = 230$ V, $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16$ A, and $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V, and under the assumption of a conversion efficiency of $\eta = 96$ % and a power factor of PF = 1, this results in an very acceptable output voltage ripple amplitude of $\hat{\tilde{V}}_{\mathrm{DC2}} \approx 12$ V. The worst case (i.e. at $V_{\mathrm{AC}} = V_{\mathrm{AC,max}} = 253$ V, $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16$ A, and $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V) ripple amplitude is $\hat{\tilde{V}}_{\mathrm{DC2}} \approx 14.2$ V, which is still less than 4% of the output voltage.

5.3.2 HF Output Filter Capacitors

Besides the electrolytic LF output filter capacitors, small HF filter capacitors are placed at the output of the DAB (see Figure 3.7) in order to bypass the HF components of the instantaneous DAB output current i_2. These capacitors are placed as close as possible to the DAB's half bridges, avoiding resonances due to parasitic PCB inductances. Moreover, in order to avoid propagation of non-bypassed HF currents to the LF filter capacitors, as well as oscillations due to the interaction of parasitic inductances (e.g. the (equivalent) series inductances of the LF and the HF filter capacitors) with the capacitances $C_{2,\mathrm{st}}$ and C_2, a 1 μH, 29 A rated SMD inductor, type IHLP5050EZER1R0M01, from Vishay Dale [131] is placed in between the LF and the HF output filter capacitors. The HF filter capacitance value C_2 is realized using seven 1.5 μF, 630 V DC, metallized polypropylene MKP film capacitors, type B32674D6155, from EPCOS [119], which are placed in parallel. This leads to a total HF output filter capacitance value of $C_2 = 10.5$ μF and a maximum HF voltage ripple amplitude of less than 2 V for the HF filter capacitors.

5.3.3 Capacitor Losses

Losses in the LF filter capacitors are caused by their equivalent series resistance (ESR) and by the leakage current. The (maximum) ESR value listed in the datasheet of the employed 390 μF EETED2W391EA ELCOs from Panasonic is 0.34 Ω at 120 Hz. According to the datasheet, the leakage current I_{leak} of a single capacitor is calculated as $I_{\mathrm{leak}} = 3 \cdot 10^{-6} \cdot \sqrt{C\,V}$ (A), with C the capacitance value in μF and V the capacitor voltage. Consequently, the total power loss $P_{\mathrm{C_{2,st}}}$ in the LF output filter capacitors is determined by [132]:

$$P_{\mathrm{C_{2,st}}} = 3 \cdot (I^2_{\mathrm{C_{2,st}}} \cdot \mathrm{ESR} + I_{\mathrm{leak}} \cdot V_{\mathrm{DC2}}), \tag{5.44}$$

where $I_{\mathrm{C_{2,st}}}$ is the RMS value of the current that flows through a single capacitor. The factor 3 is applied since three capacitors are placed in parallel. The total losses in the LF output capacitors $C_{2,\mathrm{st}}$, expressed as percentage of the nominal

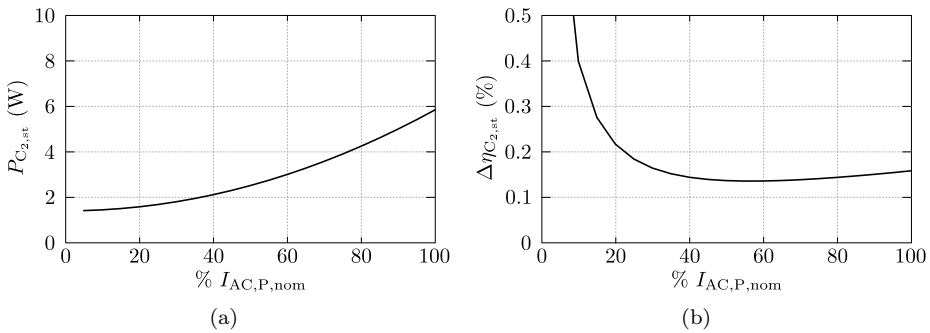


Figure 5.17: (a) Total losses in the LF output filter capacitors. (b) Efficiency loss due to the total losses in the LF output filter capacitors.

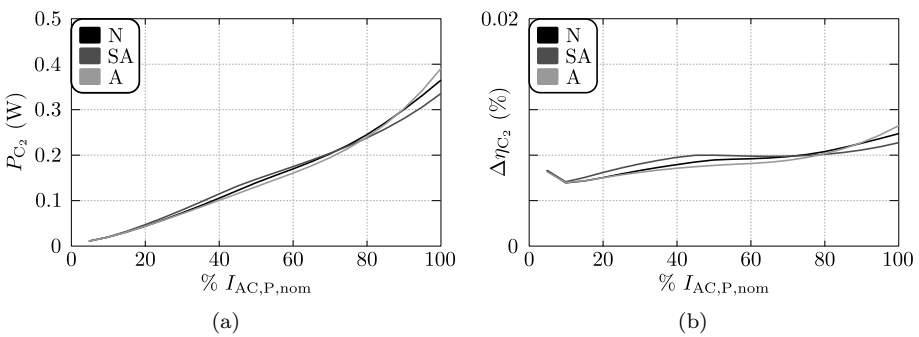


Figure 5.18: (a) Total losses in the HF output filter capacitors. (b) Efficiency loss due to the total losses in the HF output filter capacitors.

(active) AC input current $I_{AC,P,nom} = 16\ A_{rms}$, and calculated for the nominal AC input voltage of $V_{AC} = V_{AC,nom} = 230\ V_{rms}$ and the nominal DC output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V, are shown in Figure 5.17(a) while Figure 5.17(b) depicts the efficiency loss due to these losses. Note that the LF capacitor losses are independent of the applied DAB modulation scheme.

Since the leakage current of polypropylene film capacitors is very low, the losses in the EPCOS HF output filter capacitors are mainly caused by the ESR, producing a total loss of less than 0.5 W (see Figure 5.18). Consequently, the losses in the HF output filter capacitors can be neglected. Furthermore, the 1 μH SMD inductor which is placed between the HF and the LF output filter capacitances has a DC resistance of 3 mΩ, also yielding negligible losses.

5.3.4 Capacitor Volume

For the electrolytic LF output filter capacitors, with a diameter of 35 mm and a height of 40 mm for a single capacitor, the total boxed volume is 0.147 liter. The part of the SR's fan that does not faces heat sink fins is facing the LF filter capacitors, which are thereby cooled. Consequently, an additional volume of 0.024 liter (part of the SR's fan that faces the LF capacitors and that is not taken into account in the volume of the SR's cooling system, see Section 5.1.3) is added to the LF capacitor's volume for the system volume calculation (see Section 5.6). For the polypropylene HF output filter capacitors, with a width of 31.5 mm, a depth of 12.5 mm, and a height of 19 mm (single capacitor), the total boxed volume is 0.052 liter. Note that, for a given rated voltage, the volume/capacitance ratio for electrolytic capacitors is much lower than for film capacitors. Therefore electrolytic capacitors instead of film capacitors are selected for the filtering of the LF currents.

5.4 EMC Input Filter

In order to comply with the CISPR 22 Class B standard[12] [56] for conducted emission (CE), an electromagnetic compatibility (EMC) filter is designed. Thereby, a differential mode (DM) filter is required in order to attenuate the HF components of the instantaneous, HF switched, DAB input current i_1 (see Figures 3.1 and 3.7), and a common mode (CM) filter for suppressing the CM noise on the earth wire. The design of the DM and CM filters is usually performed separately, i.e. DM filter design rules and procedures are well known and are typically more straightforward than those for the CM filter design, which is mostly based on trial-and-error methods and/or on the experience of the designer [106, 133, 134].

In the context of this work, where the main goal is to address the major shortcomings of the existing analyses and circuit implementations of DAB converters, and to demonstrate that a single-stage DAB AC–DC converter is feasible for the realization of single-phase, bidirectional, and isolated energy conversions, the EMC input filter is of minor importance. For this reason, and due to the fact that EMC compliance with the CISPR 22 Class B standard could not be experimentally verified due to the unavailability of the required measurement equipment, the filter has been designed with a moderate level of detail. In fact, the main objective of the EMC filter design performed in this thesis is to get a realistic idea of the volume occupied and the losses generated by the filter, and of the impact of the three different ZVS modulation schemes proposed in Chapter 4 on the required DM filter attenuation. Consequently, this section only provides a brief summary of the applied design procedures, the main (simulation) results, the final hardware realization, and the filter losses/volume. Figure 5.19 shows the complete schematic of the single-stage DAB AC–DC converter, including the employed two-stage DM and the three-stage CM EMC filter architectures.

5.4.1 DM Filter Design

The differential mode (DM) EMC input filter is designed according to the procedure outlined in [106], and conform the guidelines given in [107] regarding filter damping, in order to comply with the CISPR 22 Class B standard [56] in the frequency range of 150 kHz – 30 MHz. The employed procedure includes the correct modeling of the line impedance stabilization network (LISN) and of the EMC test receiver (see Figure 5.19), i.e. conform the CISPR 16 standard [135]. This enables a prediction of the measurement results and thus gives the basis for the calculation of the required attenuation and for the design of the DM input filter. The video-filtered quasi-peak

[12] Devices that are marketed for use in commercial, industrial or business environments are classified as Class A digital devices. Devices that are marketed for use in residential environments, notwithstanding their use in commercial, industrial, or business environments are classified as Class B digital devices.

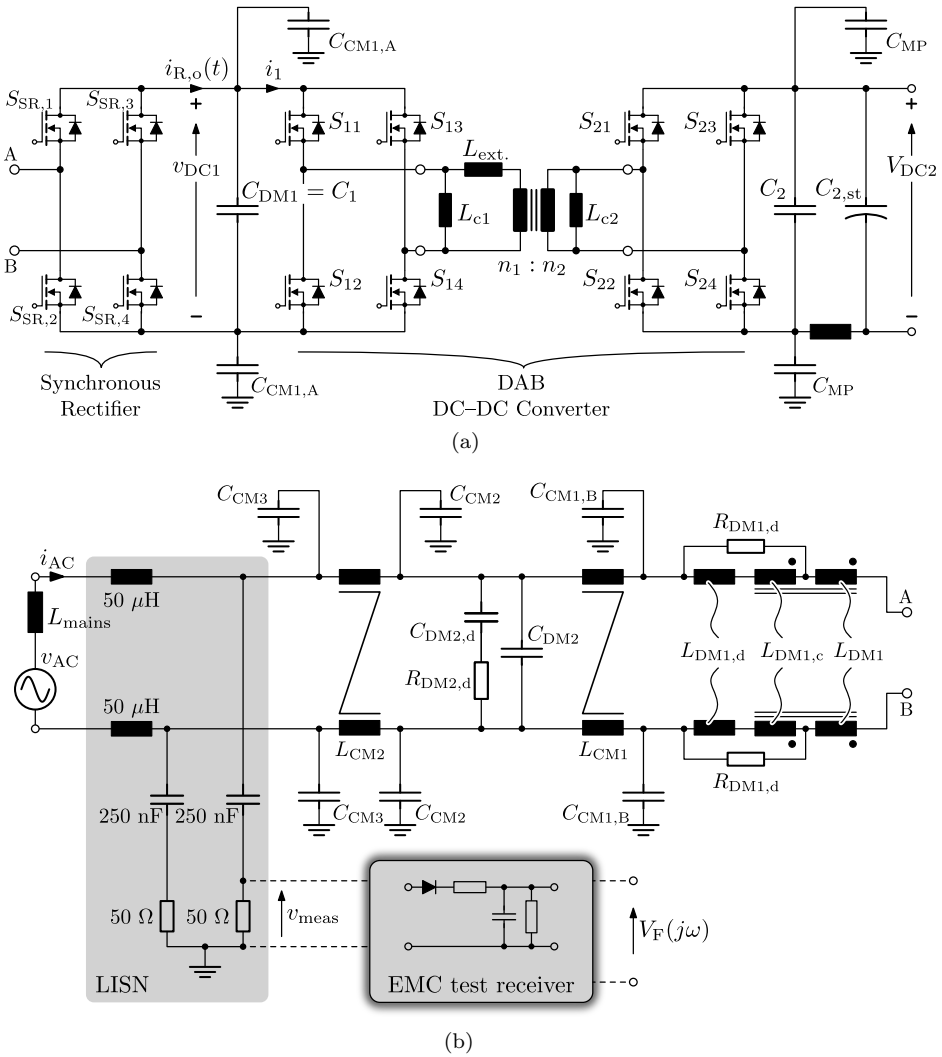


Figure 5.19: Complete schematic of the single-stage DAB AC–DC converter, including the two-stage DM and the three-stage CM EMC filters, the line impedance stabilization network (LISN), and the EMC test receiver.

(QP) values $V_F(j\omega)$ at the output of the EMC test receiver need to be lower than the CISPR 22 Class B limit $Lim_B(j\omega)$. For all three ZVS modulation schemes (numerical 'N', analytical 'A', and semi-analytical 'SA') proposed in Chapter 4, the top inset of Table 5.8 lists the most critical (i.e. with regard to the required filter attenuation) output values $V_{F,f_{crit}}$, as well as the Class B limit value $Lim_{B,f_{crit}}$ at

the corresponding frequency f_{crit}, in case no DM input filter is present[13]. The unit for $V_{\text{F,f}_{\text{crit}}}$ and $Lim_{\text{B,f}_{\text{crit}}}$ is 'dB·μV'. The required attenuation $Att_{\text{req,f}_{\text{crit}}}$ (in dB) of the input filter, including a margin of 6 dB, is consequently given by:

$$Att_{\text{req,f}_{\text{crit}}} = V_{\text{F,f}_{\text{crit}}} - Lim_{\text{B,f}_{\text{crit}}} + 6\ dB, \tag{5.45}$$

which is also listed in the top inset of Table 5.8. Though the difference is quasi negligible, it can be seen that $Att_{\text{req,f}_{\text{crit}}}$ is lowest for the numerically derived ZVS modulation scheme, which can be explained by the fact that, contrary to the analytically and the semi-analytically derived modulation schemes, switching frequency modulation is applied at high v_{DC1} (see Chapter 4). This results in a broader spectral distribution of the harmonic power and/or reduction of the amplitudes of individual harmonics [108], which translates to a slightly lower filter volume.

In Figure 5.20, the simulated (nominal operating conditions) video-filtered quasi-peak (QP) values $V_{\text{F}}(j\omega)$ (indicated by a '☆'), before insertion of the designed

[13]Note that the values listed in Table 5.8 are obtained from simulations that are performed under nominal operating conditions, i.e. at the nominal AC input voltage of $V_{\text{AC}} = 230\ \text{V}_{\text{rms}}$, the nominal input current of $I_{\text{AC,P}} = I_{\text{AC,P,nom}} = 16\ \text{A}_{\text{rms}}$, a power factor of PF = 0.999, and an output voltage of $V_{\text{DC2}} = V_{\text{DC2,nom}} = 400$ V.

		N	SA	A
Excl. filter	f_{crit} (kHz)	236.1	237.3	236.3
	$V_{\text{F,f}_{\text{crit}}}$ (dB·μV)	169.3	171.6	170.4
	$Lim_{\text{B,f}_{\text{crit}}}$ (dB·μV)	62.23	62.19	62.22
	$V_{\text{F,f}_{\text{crit}}} - Lim_{\text{B,f}_{\text{crit}}}$ (dB·μV)	107.07	109.41	108.18
	$Att_{\text{req,f}_{\text{crit}}}$ (dB)	107.07+6 = 113.07	109.41+6 = 115.41	108.18+6 = 114.18
Incl. filter (prototype)	$V_{\text{F,f}_{\text{crit}}}$ (dB·μV)	62.53	64.93	63.79
	$V_{\text{F,f}_{\text{crit}}} - Lim_{\text{B,f}_{\text{crit}}}$ (dB·μV)	0.3	2.74	1.57
Incl. filter (modified)	$V_{\text{F,f}_{\text{crit}}}$ (dB·μV)	55.57	58.01	57.4
	$V_{\text{F,f}_{\text{crit}}} - Lim_{\text{B,f}_{\text{crit}}}$ (dB·μV)	-6.66	-4.18	-4.82

Table 5.8: Critical video-filtered quasi-peak (QP) values $V_{\text{F,f}_{\text{crit}}}$ at the output of the EMC test receiver, as well as the Class B limit value $Lim_{\text{B,f}_{\text{crit}}}$ at the corresponding frequency f_{crit}, for all three ZVS modulation schemes (numerical 'N', analytical 'A', and semi-analytical 'SA') proposed in Chapter 4. Top inset: excluding the DM input filter (these values determine the required filter attenuation $Att_{\text{req,f}_{\text{crit}}}$); middle inset: including the DM input filter (prototype system); bottom inset: including the DM input filter (modified design).

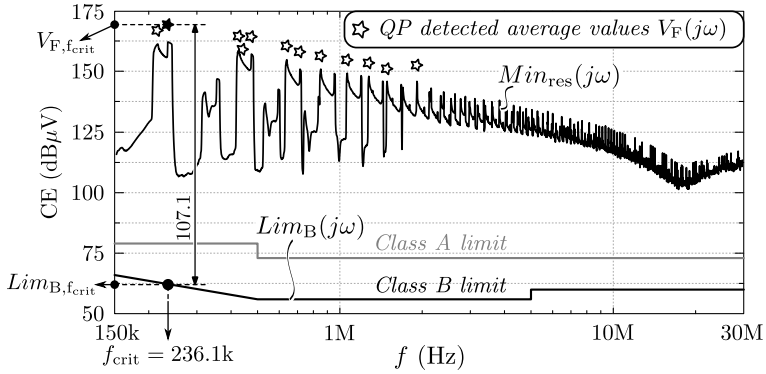


Figure 5.20: Simulation of the QP measurement (based on the video-filtered values of voltage $V_F(j\omega)$) for the numerically derived ZVS modulation scheme, before insertion of the designed DM input filter and under the assumption of zero mains impedance. Also shown is the absolute lower boundary $Min_{res}(j\omega)$ for the measurement result, as well as the CE limits according to CISPR 22 Classes A and B.

DM input filter and under the assumption of zero mains impedance, are shown for the numerically derived ZVS modulation scheme, along with the CISPR 22 Classes A and B limits. The critical output value $V_{F,f_{crit}}$ is indicated by a '★'. The curve $Min_{res}(j\omega)$ is obtained as the square root of the sum of the squares of the RMS values of all harmonic components $V_{meas}(j\omega)$ located within the resolution bandwidth (RBW) of the EMC test receiver [106]. Note that v_{meas} is the voltage at the LISN output, and is applied to the input of the EMC test receiver (see Figure 5.19). $Min_{res}(j\omega)$ can be seen as a signal that shows equal spectral power (equivalent RMS value) at the angular frequency $\omega = 2\pi f$, as given for the original signal within the RBW, defining an absolute lower boundary for the measurement result. This boundary can be used in order to simplify the DM filter design and/or to omit precise modeling of the EMC test receiver but, however, leads to an underestimation of the required filter attenuation. Therefore, the $Min_{res}(j\omega)$-line is only shown for illustration.

The DM filter needs to be primarily designed in order to provide the required attenuation $Att_{req,f_{crit}}$ listed in Table 5.8 so that, in combination with an appropriate CM filter, the converter complies with the EMC standards. However, control-oriented aspects also have to be considered, ensuring a satisfactory operation of the converter in combination with the input filter. Using the recursive design procedure outlined in [106], the two-stage DM filter structure shown in Figure 5.19 turns out to be most appropriate for achieving these goals[14]. In order to provide

[14]The components of the DM filter in Figure 5.19 are indexed 'DM' (i.e. 'DM1' for the first filter stage and 'DM2' for the second filter stage). The capacitive part C_{DM1} of the first DM

Filter stage 1			
Component	*Value*	*Quantity*	*Specification*
L_{DM1} / $L_{\mathrm{DM1,c}}$, coupled inductor	34.6 / 1.64 μH	2	Magnetics [136], High Flux 60, CO58083A2, 23:5 turns, 11 AWG wire
$L_{\mathrm{DM1,d}}$, inductor	6.9 μH	2	Magnetics [136], MPP60, CO55351A2, 13 turns, 11 AWG wire
C_{DM1}, X2 capacitor (MKP)	13.2 μF	6 in par.	EPCOS [119] – B32923E3225, 2.2 μF, 305 V_{AC}
$R_{\mathrm{DM1,d}}$, SMD resistor	0.19 Ω	2 x 2 in par.	0.38 Ω - 1 W
Filter stage 2			
Component	*Value*	*Quantity*	*Specification*
L_{DM2}=L_{mains}	0...300 μH	–	Mains inductance
C_{DM2}, X2 capacitor (MKP)	1 μF	1	EPCOS [119] – B32923C3105, 1 μF, 305 V_{AC}
$C_{\mathrm{DM2,d}}$, X2 capacitor (MKP)	0.47 μF	1	EPCOS [119] – B32922C3474, 0.47 μF, 305 V_{AC}
$R_{\mathrm{DM2,d}}$, SMD resistor	20 Ω	2 in ser.	10 Ω - 0.33 W

Table 5.9: Differential mode (DM) EMC input filter components.

sufficient damping of the filter resonances without decreasing the attenuation in the frequency range that is relevant for compliance with the CISPR standard, for each filter stage an (optimized) passive damping network is employed. Thereby, a series inductor damping network with coupled inductors is selected for the first filter stage while a parallel capacitor damping network is used for the second filter stage. The final values[15] and specifications of the DM filter components employed in the converter prototype system developed in this work are listed in Table 5.9. Note that the second filter stage is formed by capacitance C_{DM2} in combination with the LISN ($R_{\mathrm{LISN}} = 50\ \Omega$, $C_{\mathrm{LISN}} = 250$ nF, $L_{\mathrm{LISN}} = 50\ \mu$H, see Figure 5.19) and the mains impedance (inductance) L_{mains}, i.e. no discrete inductor L_{DM2} is present.

Figure 5.21 depicts the resulting attenuation characteristics $Att_{\mathrm{Filt}}(j\omega)$ of the filter (including the LISN) for three different mains inductances ($L_{\mathrm{mains}} = 0, 100, 300\ \mu$H). The dashed lines correspond with the final filter without damping (undamped filter), i.e. without $L_{\mathrm{DM1,c}}$, $L_{\mathrm{DM1,d}}$, and $R_{\mathrm{DM1,d}}$ (damping network of the first filter stage) and without $C_{\mathrm{DM2,d}}$ and $R_{\mathrm{DM2,d}}$ (damping network of the second filter stage), while the solid lines show the attenuation characteristics with inclusion of the above mentioned damping networks. Also indicated in Figure 5.21 is the filter attenuation value $Att_{\mathrm{Filt,f_{crit}}}$ at the, for the numerically derived ZVS modulation

filter stage is effectively realized by the HF DC-link capacitance C_1, which quasi fully absorbs the HF components of the instantaneous, HF switched, DAB input current i_1, and thus acts as an inherently integrated input filter.

[15] Remind that, in order to limit the required reactive power flow capability of the DAB converter, the total DM EMC filter capacitance value has been restricted to: $(C_{\mathrm{DM1}} + C_{\mathrm{DM2}})_{\max} \leqslant 14.2\ \mu$F (see Section 3.1 of Chapter 3).

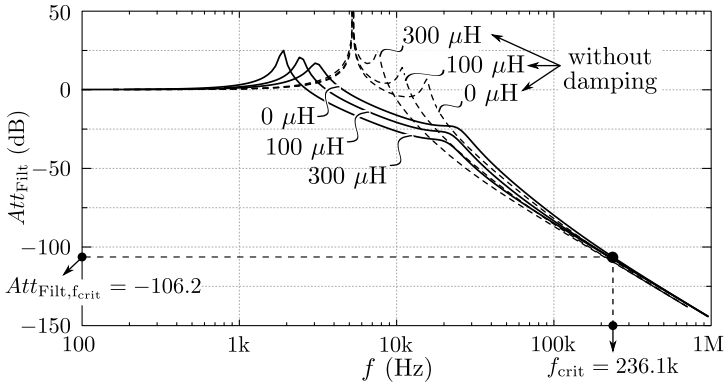


Figure 5.21: DM input filter attenuation characteristics (incl. LISN) for three different mains impedances (inductances): $L_{\mathrm{mains}} = 0, 100, 300$ μH. Solid lines: with damping networks; dashed lines: without damping networks.

scheme, 'critical' frequency f_{crit} (see Table 5.8). As can be seen from Figure 5.22, the filter damping increases the filter input impedance and thus reduces the amplitudes of the oscillating currents and voltages that result from mains voltage distortions. Additionally, as shown in Figure 5.23, it decreases the filter output impedance at parallel resonant frequencies, facilitating the design of the system control. For an assumed worst case mains inductance of $L_{\mathrm{mains}} = L_{\mathrm{mains,max}} = 300$ μH, it is calculated that the magnitude of the filter output impedance is significantly lower than the converter's input impedance up to a frequency of about 1.5 kHz, determining the absolute minimum control bandwidth [106, 107], i.e. $B_{w,\mathrm{min}} \approx$ 1.5 kHz.

Figure 5.24 shows the simulated (nominal operating conditions) video-filtered quasi-peak (QP) values $V_{\mathrm{F}}(j\omega)$ (indicated by a '☆'), along with the CISPR 22 Classes A and B limits and the lower boundary value $Min_{\mathrm{res}}(j\omega)$, for the numerically derived modulation scheme, after insertion of the designed DM input filter and under the assumption of zero mains impedance. It can be seen that the critical output value $V_{\mathrm{F,f_{crit}}}$ (indicated by a '★') quasi falls together with the Class B limit. The value $V_{\mathrm{F,f_{crit}}}$, after insertion of the designed filter, is listed in the middle inset of Table 5.8 and is 0.3 dB higher than $Lim_{\mathrm{B,f_{crit}}}$. This means that the attenuation provided by the DM input filter used in the final prototype converter is slightly too low for complying with the CISPR 22 Class B standard, especially when considering the additional margin of 6 dB. The reason is that, similar as for the magnetic components (see Section 5.2.3), the initial EMC input filter design is based on the current-based (CB) ZVS DAB modulation scheme presented in [84], requiring a lower filter attenuation than when using the final current-dependent charge-based (CDCB) ZVS modulation schemes presented in Chapter 4. For the analytically and the semi-analytically derived ZVS modulation schemes the situation is even worse

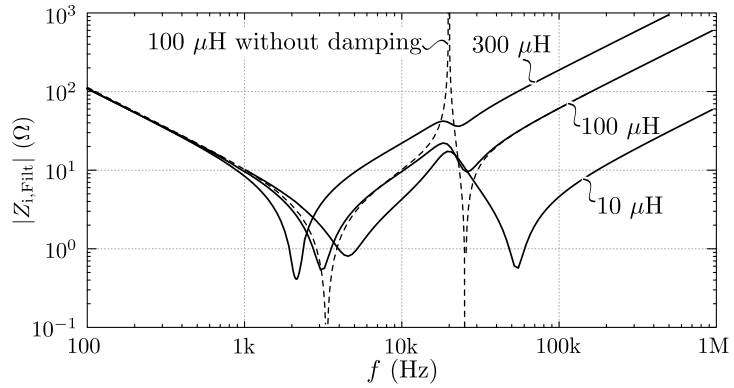


Figure 5.22: Magnitude of the filter input impedance (excl. LISN) for open-circuit filter output and for three different mains impedances (inductances): $L_{\text{mains}} = 10, 100, 300$ μH. Solid lines: with damping networks; dashed line: without damping networks.

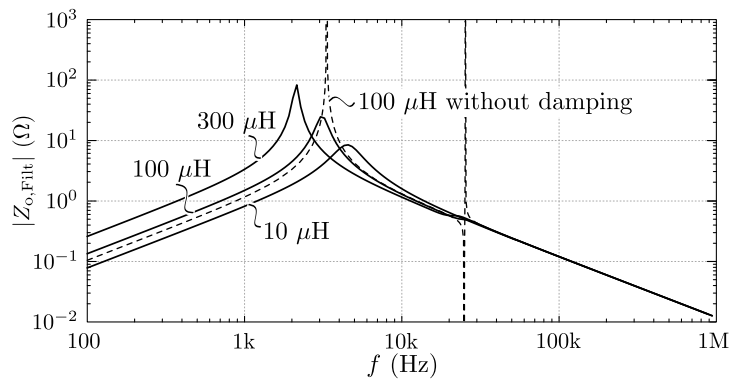


Figure 5.23: Magnitude of the filter output impedance (excl. LISN) for three different mains impedances (inductances): $L_{\text{mains}} = 10, 100, 300$ μH. Solid lines: with damping networks; dashed line: without damping networks.

than for the numerically derived modulation scheme, as can also be seen from the middle inset of Table 5.8. Figure 5.25 is a repetition of Figure 5.24, employing a slightly modified filter design whereby capacitance value C_{DM2} is increased from 1 μF to 2.2 μF. Now compliance with the CISPR 22 Class B standard is achieved, i.e. $V_{\text{F,f}_{\text{crit}}}$ is substantially lower than $Lim_{\text{B,f}_{\text{crit}}}$. The same is true for the analytically and the semi-analytically derived ZVS modulation schemes, as can be seen from the bottom inset of Table 5.8. Note that the replacement of C_{DM2} does not imply a substantial increase of the filter volume, neither it has a noticeable effect on the other filter characteristics and the achievable power factor.

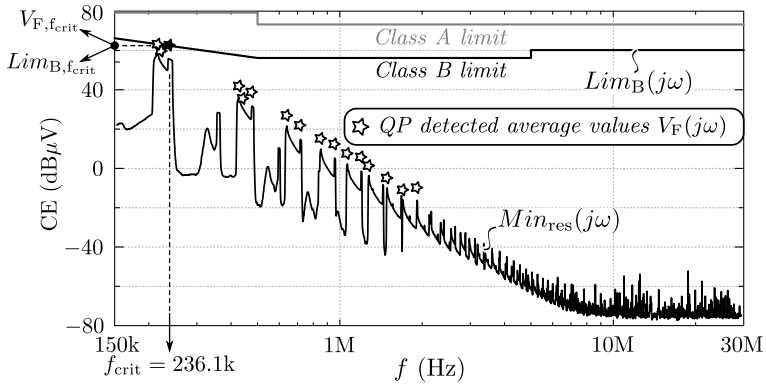


Figure 5.24: Simulation of the QP measurement (based on the video-filtered values of voltage $V_{\mathrm{F}}(j\omega)$) for the numerically derived ZVS modulation scheme, after insertion of the designed DM input filter (prototype converter) and under the assumption of zero mains impedance. Also shown is the absolute lower boundary $Min_{\mathrm{res}}(j\omega)$ for the measurement result, as well as the CE limits according to CISPR 22 Classes A and B.

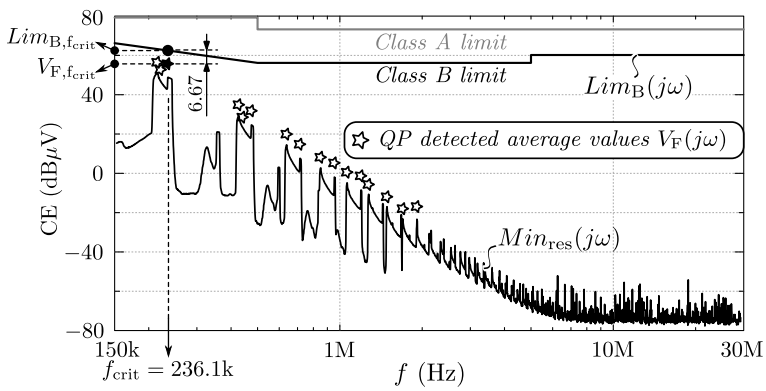


Figure 5.25: Simulation of the QP measurement (based on the video-filtered values of voltage $V_{\mathrm{F}}(j\omega)$) for the numerically derived ZVS modulation scheme, after insertion of the designed DM input filter (modified design) and under the assumption of zero mains impedance. Also shown is the absolute lower boundary $Min_{\mathrm{res}}(j\omega)$ for the measurement result, as well as the CE limits according to CISPR 22 Classes A and B.

The simulated (nominal operating conditions) low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [57] for Class A equipment, are depicted in Figure 5.26 and are well below the limits.

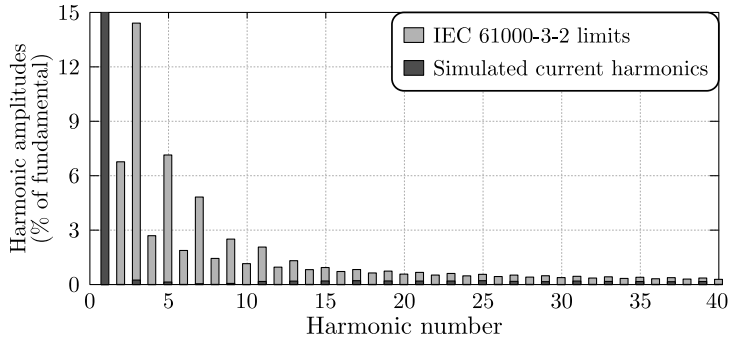


Figure 5.26: Simulated low-frequency harmonics of the mains current, compared to the IEC 61000-3-2 limits.

5.4.2 CM Filter Design

In order to successfully design a common mode (CM) filter that suppresses the CM noise on the earth wire, an equivalent CM noise source model is required [133, 134]. Thereby, detailed knowledge of the relevant parasitic impedances, through which the CM currents circulate, is essential. These impedances are mainly formed by parasitic distributed capacitances that manifest between the different converter components and the heat sinks which, for the system at hand, are connected to the distribution protective earth (PE). In addition, the different values for the stray capacitances to PE, as well as the inductances of the interconnections and their mutual magnetic couplings should be taken into account. As a result, the design of the CM EMC filter is mostly performed after the realization of a first converter prototype system[16]. The parasitic impedances can then be identified through impedance measurements and a CM noise propagation model can be derived for the frequency range where the main CM filter components are to be designed. Consequently, several design iterations of the prototype system and/or the CM filter might be required until compliance with CISPR 22 Class B standard for conducted emission (CE) is obtained. This can be a very time intensive and complex task. Therefore, and as in the context of this work the EMC input filter (especially the CM filter part[17]) is of minor importance, here the CM filter design is omitted. Nevertheless, for comprehensiveness a CM filter has been added to the converter hardware. However, the selection of the filter architecture and the determination of the CM component values are based on intuition, rather than on modeling and optimization. Therefore it cannot be assured that the filter complies

[16]The fact that the DM filter components have an influence on the behavior of the CM current propagation paths implies that the design of the DM filter needs to be available/ready for a CM modeling procedure.

[17]Note that it is the DM filter and not the CM filter which mainly defines the EMC filter volume, the low-load power factor, and the dynamics of the system.

AC-side: filter stage 1			
Component	*Value*	*Quantity*	*Specification*
L_{CM1}, inductor	0.34 mH @ 100 kHz	1	Vacuumschmelze VAC [137], VITROPERM 500F, L2020-W409, 2 x 5 turns, 11 AWG wire
$C_{CM1,A}$, Y2 capacitor (MKP)	6.8 nF	2 x 1	EPCOS [119] – B32021A3682, 6.8 nF, 300 V_{AC}
$C_{CM1,B}$, Y2 capacitor (MKP)	2.2 nF	2 x 1	EPCOS [119] – B32021A3222, 2.2 nF, 300 V_{AC}
AC-side: filter stage 2			
Component	*Value*	*Quantity*	*Specification*
L_{CM2}, inductor	0.34 mH @ 100 kHz	1	Vacuumschmelze VAC [137], VITROPERM 500F, L2020-W409, 2 x 5 turns, 11 AWG wire
C_{CM2}, Y2 capacitor (MKP)	10 nF	2 x 1	EPCOS [119] – B32022A3103, 10 nF, 300 V_{AC}
AC-side: filter stage 3			
Component	*Value*	*Quantity*	*Specification*
C_{CM3}, Y2 capacitor (MKP)	1 nF	2 x 1	EPCOS [119] – B32021A3102, 1 nF, 300 V_{AC}
DC-side			
Component	*Value*	*Quantity*	*Specification*
C_{MP}, Y2 capacitor (MKP)	13.6 nF	2 x 2	EPCOS [119] – B32021A3682, 6.8 nF, 300 V_{AC}

Table 5.10: Common mode (CM) EMC input filter components.

with the standard. As can be seen from Figure 5.19, in which the components of the CM filter are indexed 'CM' (i.e. 'CM1' for the first, 'CM2' for the second, and 'CM3' for the third filter stage), a three-stage CM EMC filter structure is employed. The final values and specifications of the CM filter components used in the converter prototype system are listed in Table 5.10.

5.4.3 EMC Filter Losses and Volume

Figure 5.27 shows the hardware realization of the CM and DM EMC input filter. With a width of 132 mm, a height of 72 mm, and a depth of 25 mm, the total boxed volume of the filter board is 0.238 liter[18]. An additional volume of 0.042 liter is occupied by six CM filter capacitors that are placed on another PCB, yielding a total EMC filter volume of 0.279 liter.

[18]Note that this volume includes the converter's AC connection terminals and an AC fuse, the converter's DC connection terminals and a DC fuse (both not shown in the picture), a 2-electrode surge arrestor (type EC600-X, EPCOS), and several metal oxide varistors.

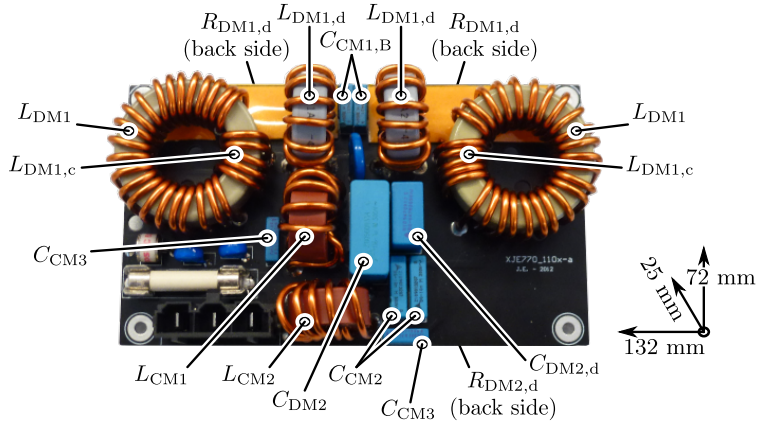


Figure 5.27: Hardware realization of the EMC input filter.

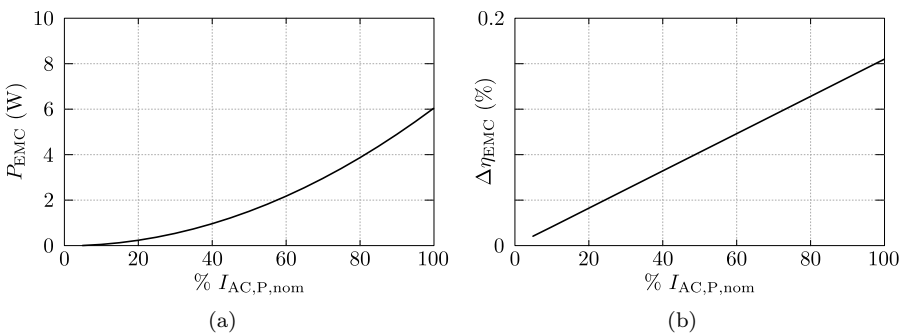


Figure 5.28: (a) Total losses in the EMC input filter. (b) Efficiency loss due to the total losses in the EMC input filter.

Since the leakage current of polypropylene film capacitors is very low, the losses in the EPCOS HF EMC filter capacitors are mainly caused by the ESR, producing a total loss of less than 0.4 W. Consequently, the losses in the EMC filter capacitors can be neglected. The same goes for the losses (less than 0.1 W) in damping resistors $R_{DM1,d}$ and $R_{DM2,d}$, and for the core losses of the DM inductors. The reason is that the largest part of the HF components of the instantaneous, HF switched, DAB input current i_1, are bypassed by DM filter capacitance C_{DM1}. As a result, the main contributors to the overall losses of the EMC input filter are the losses due to DC resistance of the CM and DM inductor windings.

The total losses of the EMC input filter, expressed as percentage of the nominal (active) AC input current $I_{AC,P,nom} = 16\ A_{rms}$, and calculated for the nominal AC input voltage of $V_{AC} = V_{AC,nom} = 230\ V_{rms}$ and the nominal DC output voltage

of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V, are shown in Figure 5.28(a), while Figure 5.28(b) depicts the efficiency loss due to these losses. Note that the EMC filter losses are quasi independent of the applied DAB modulation scheme. In future, the design of the EMC input filter may be performed with respect to the optimization of a certain Performance Index (e.g. maximum power density or minimum losses) such as in [138].

5.5 Control Board

5.5.1 Controller Hardware

The control hardware consists of an on-board FPGA, in particular the ALTERA EP3C25E144C8N CYCLONE III, which is operated with a clock frequency of 62.5 MHz and programmed in the VHDL hardware description language. The FPGA is responsible for generating the PWM gate drive signals, for reading in the current and voltage measurement peripherals (A/D converters), and for 'fast' overcurrent and overvoltage protection. Moreover it communicates over Ethernet with an off-board PC-based Real-Time Target (RTT) from Triphase [139]. The use of the Triphase RTT allows flexible implementation of different control algorithms. In a next phase the functions of the RTT can be implemented on the 3C25 FPGA by means of an embedded CPU [139]. The RTT can be programmed and operated through Matlab/Simulink^{TM} where the controllers, the 'slow' protection, the start-stop procedures, the control parameter generation, and the delay and dead-time compensation are implemented (see Section 5.5.2). The Real-TimeWorkshop^{TM} automatic code generator translates the Matlab/Simulink^{TM} model into C-code which is compiled and executed by the RTT. Figure 5.29 shows the hardware implementation of the control board with inter alia the ALTERA CYCLONE III FPGA, the ETHERNET interface, a CAN-bus interface, as well as several auxiliary power supplies for powering all low voltage circuitry and the gate drive units.

5.5.2 Controller Software

The cascaded control structure used to control the DAB input current i_{DAB1} in accordance to (3.12) is shown in Figure 5.30. The dashed lines indicate which part of the controller hardware (see Section 5.5.1) performs each particular task. The

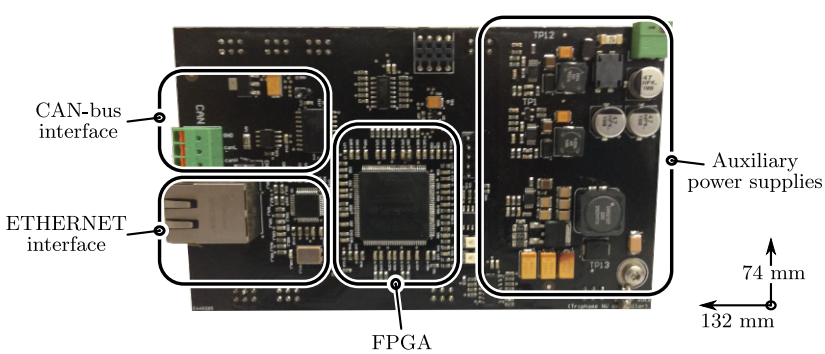


Figure 5.29: Hardware implementation of the control board.

measured quantities (index m) that are available in the PFGA as digital signals are also indicated in Figure 5.30. A PI current control loop controls i_{DAB1} based on a reference value $i_{\mathrm{DAB1,ref}}$ which is generated using a Phase Locked Loop (PLL) and calculation of (3.12). The set values $\hat{I}^*_{\mathrm{AC,P}}$, dir^*, and PF* origin from an external source such as the battery management system or the vehicle power management system. For testing of the prototype system a fixed voltage was used at the output of the DAB and the set values were manually applied. Optionally, an outer PI voltage controller can be used to control the output voltage V_{DC2}.

The control parameters needed for the DAB to generate the set current $i_{\mathrm{DAB1,set}}$ are determined using lookup tables which are stored in the memory of the RTT. The control parameter lookup tables are calculated for the whole converter's operating range conform Figure 3.6, using the CDCB ZVS modulation schemes derived in Chapter 4. Based on $[i_{\mathrm{DAB1,set}}; v_{\mathrm{DC1,m}}; V_{\mathrm{DC2,m}}]$, the modulation parameters $\mathbf{x_{set}}$, the delay vector $\mathbf{t_{sw,del,set}}$, and the dead time vector $\mathbf{t_{dead,set}}$ are determined using linear table interpolation. $\mathbf{t_{sw,del,set}}$ and $\mathbf{t_{dead,set}}$ consist of respectively the switching delays $t_{\mathrm{sw,del}}$ (according to equation (3.66)) and dead times $t_{\mathrm{dead,min}}$ (according to equation (3.67)) at the different commutation instances $\theta_{\mathrm{i}} = \{\alpha, \beta, \gamma, \text{ and } \delta\}$ (see Section 3.3.2). Lastly, the modulator function calculates the frequency counter f_{ctr}, and the timing and duty-cycle counters for each bridge leg: $\mathbf{T_{ctr}} = [T_{\mathrm{ctr,11}}; T_{\mathrm{ctr,12}}; T_{\mathrm{ctr,21}}; T_{\mathrm{ctr,22}}]$; $\mathbf{D_{ctr}} = [D_{\mathrm{ctr,11}}; D_{\mathrm{ctr,12}}; D_{\mathrm{ctr,21}}; D_{\mathrm{ctr,22}}]$. These, as well as the enable signals **EN** and the SR state st_{SR}, are inputted to the FPGA PWM-generation modules.

The closed loop control of DAB converters is typically performed in this fashion [39, 92], i.e. using lookup tables in which pre-calculated values for the modulation parameters (i.e. the duty-cycles, the phase-shift angle, the dead-times, and the delay compensation) are stored. It turns out that the use of a pre-calculated set of control values is the simpler and more straightforward method to control DAB converters. The lack of the massive calculation power needed to solve the control equations is the major reason. Using lookup tables, complex relations can be pre-calculated. Moreover, high density non-volatile memories make a high number of table dimensions feasible. Furthermore, the lookup table is used to put the converter in a quasi-static operating point, drawing a given current in the presence of two back emfs. However, table entries are dedicated results for one particular DAB converter. In practice, the system may be sensitive to changes of inductance values, and care should be taken when using high-performance MOSFETs. Loss of ZVS can easily cause device destruction. The DAB inductances, however, could be considered as another dimension of the lookup table.

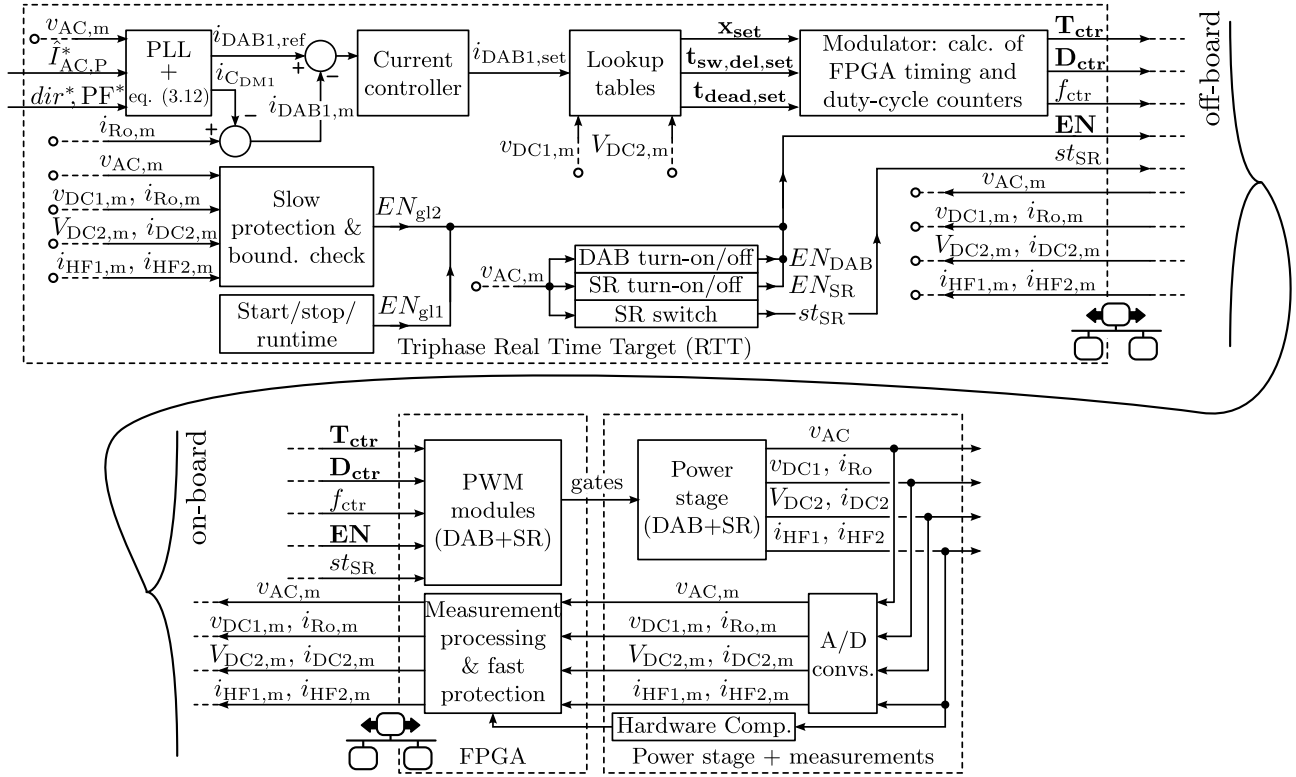


Figure 5.30: Control structure employed to control the input current i_{DAB1} in accordance to (3.12) as well as the modulator function, the synchronous rectifier switch, and the enabling/disabling units (i.e. the start/stop/runtime, overcurrrent and overvoltage protection, and boundary check). The dashed lines indicate which part of the controller hardware (RRT, FPGA, or power stage/measurements) performs each particular task.

5.6 Overall Converter Losses and Volume

The summation of the losses and volumes of the different converter components, which are designed in the previous sections, leads to the overall performance (i.e. with regard to the conversion efficiency and the power density) of the investigated single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter. Below, the achieved (calculated) conversion efficiency and power density of the complete system are presented for two converter designs:

1. Converter design A (prototype converter), which is implemented using heat sink designs A (see Section 5.1) and using inductor/transformer designs A (see Section 5.2);
2. Converter design B (further optimized), which is implemented using heat sink designs B (see Section 5.1) and using inductor/transformer designs B (see Section 5.2).

The prototype converter system developed in this work (see Section 5.6.3) is realized in accordance with converter design A. Converter design B, which uses further optimized heat sinks (i.e. the thickness of the fins and the width of the heat sink channels are adapted in order to achieve a lower thermal resistance) and further optimized magnetic components, yields higher conversion efficiencies and a higher power density compared to converter design A (prototype system) and is used to quantify the performance enhancement that is possible by applying minor adjustments to the component hardware realizations. As the outer dimensions of the adjusted components, i.e. the heat sinks and the DAB's magnetic components, stay the same (except for the dimensions of the primary side commutation inductor L_{c1}), these adjustments do not imply a complete redesign of the mechanical assembly, enabling simple replacement.

5.6.1 Converter Losses and Efficiency

Figure 5.31 depicts the total converter losses and the corresponding conversion efficiencies, calculated for the following scenarios:

1. Converter design A (prototype converter), applying the
   (a) Numerically derived ZVS modulation scheme (cf. Section 4.1);
   (b) Analytically derived ZVS modulation scheme (cf. Section 4.2);
   (c) Semi-analytically derived ZVS modulation scheme (cf. Section 4.3).
2. Converter design B (further optimized), applying the

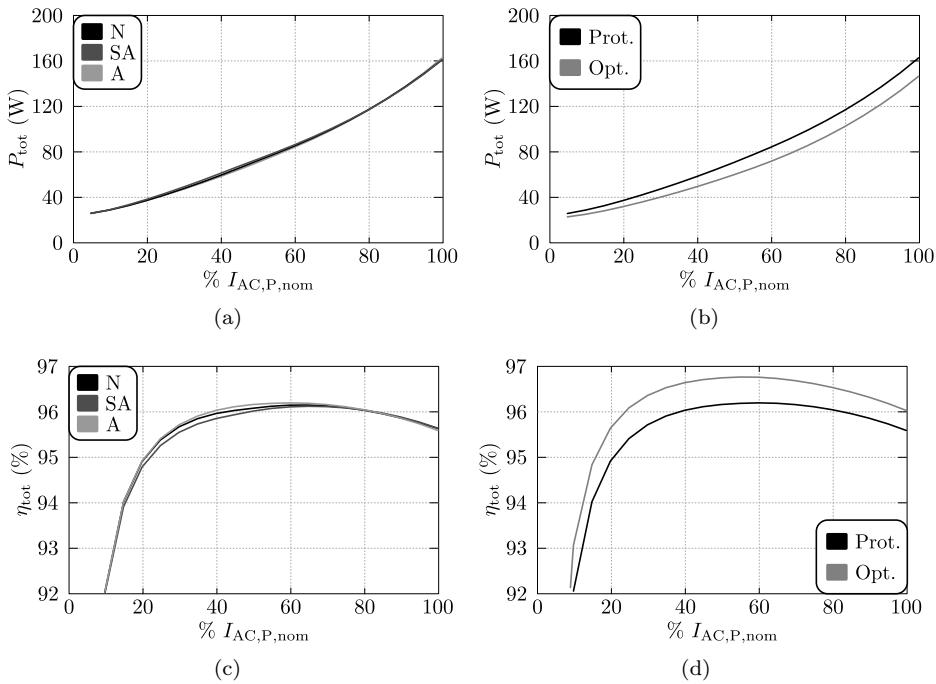


Figure 5.31: (a)-(b) Total losses of the investigated DAB AC–DC converter, (a) according to scenarios 1(a), 1(b), and 1(c); (b) according to scenarios 1(b) and 2(a). (c)-(d) Calculated efficiency of the investigated DAB AC–DC converter, (c) according to scenarios 1(a), 1(b), and 1(c); (d) according to scenarios 1(b) and 2(a).

(a) Analytically derived ZVS modulation scheme (cf. Section 4.2).

Scenarios 1(a), 1(b), and 1(c) allow to objectively compare the three different DAB modulation schemes proposed in Chapter 4 with regard to the total converter losses and efficiency. Furthermore, scenario 2(a) can be compared with scenario 1(b) in order to investigate the performance improvement that is possible by replacing converter design A (prototype) by the further optimized design B. The different quantities on the y-axes of Figure 5.31 are depicted as function of the active AC input current $I_{\mathrm{AC,P}}$ (x-axes) which is expressed as percentage of the nominal (active) AC input current $I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$. The figure is obtained for the nominal AC input voltage of $V_{\mathrm{AC}} = V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$ and the nominal DC output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. In order to meet the power factor requirement specified in Table 1.1 of Section 1.3, the applied power factor (PF) is calculated with (5.21).

Figure 5.31(a) shows the total converter losses regarding scenarios 1(a), 1(b), and 1(c). It can be seen that there is no substantial difference between the three modulation schemes with regard to the total converter losses. From Figure 5.31(b), regarding scenarios 1(b) and 2(a), it can be seen that when replacing converter design A (prototype, indicated by 'Prot.') by converter design B (further optimized, indicated by 'Opt.'), a substantial loss reduction is achieved, which mainly results from the improved design of the primary side commutation inductor L_{c1} and the HF AC-link transformer. Note that the calculated overall converter losses include the auxiliary power losses, which comprise the power consumption of the fans and of the control board. These losses are estimated to be approximately 7 W (see also Figure 5.32).

Figure 5.31(c) (scenarios 1(a), 1(b), and 1(c)) and Figure 5.31(d) (scenarios 1(b), 2(a)) show the system's conversion efficiency. From Figure 5.31(c) it can be seen that the applied modulation scheme ('N', 'A', or 'SA') has only a small impact on the efficiency, which is above 95 % for input powers higher than 20 % of the nominal input power, with a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is around 96.1 % and the efficiency at nominal input power approximately 95.6 %. However, from Figure 5.31(d) it is clear that, at all power levels, an important efficiency enhancement is feasible (up to around 0.8 %) when considering converter design B ('Opt.') instead of converter design A ('Prot.'). This results in a conversion efficiency that is above 95.6 % for input powers higher than 20 % of the nominal input power, with again a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is now around 96.75 % and the efficiency at nominal input power approximately 96 %.

Figure 5.32 shows the loss contribution of the different converter components for both converter designs A (dark gray bars) and B (light gray bars), calculated using the analytically derived ZVS modulation scheme. Figure 5.32(a) corresponds with the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, the nominal input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, a power factor of PF = 0.999, and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V, while Figure 5.32(b) corresponds with the same voltage conditions but is calculated for a reduced input power: $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$ and PF = 0.983.

The loss reduction achieved by using converter design B ('Opt', light gray bars) instead of converter design A ('Prot.', dark gray bars) is 16.1 W at the nominal input power (see Figure 5.32(a)) and 5.3 W at 20% of the nominal input power (see Figure 5.32(b)). This reduction is mainly the result of the improved design of the primary side commutation inductor L_{c1} and the HF AC-link transformer. It is also clear that the semiconductor power switches are the biggest contributors to the overall losses.

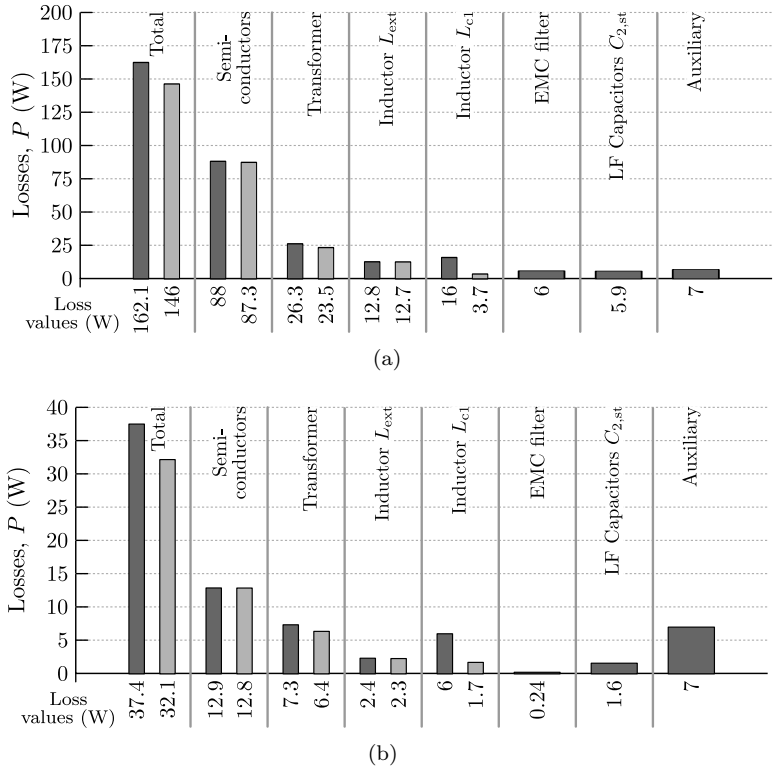


Figure 5.32: Loss contribution of the different converter components for both converter designs A (dark gray bars) and B (light gray bars), calculated using the analytically derived ZVS modulation scheme. (a) Conditions: $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, PF = 0.999, and $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V. (b) Same voltage conditions but now $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$ and PF = 0.983.

5.6.2 Converter Volume and Power Density

Figure 5.33 shows the volume contribution of the different converter components for both converter designs A (dark gray bars) and B (light gray bars), calculated using the boxed component volumes derived in the previous sections. The bars 'total, excl. other' represent the summation of the component volumes listed in Figure 5.33, while the bars 'total, incl. other' represent the total boxed volume of the complete converter system, including the 'dead space' and the volume of the remaining electronic components such as the measurement circuits, the PCBs, and the gate drive units. As the outer dimensions of the optimized heat sinks, the optimized main inductor L_{ext}, and the optimized HF AC-link transformer (i.e.

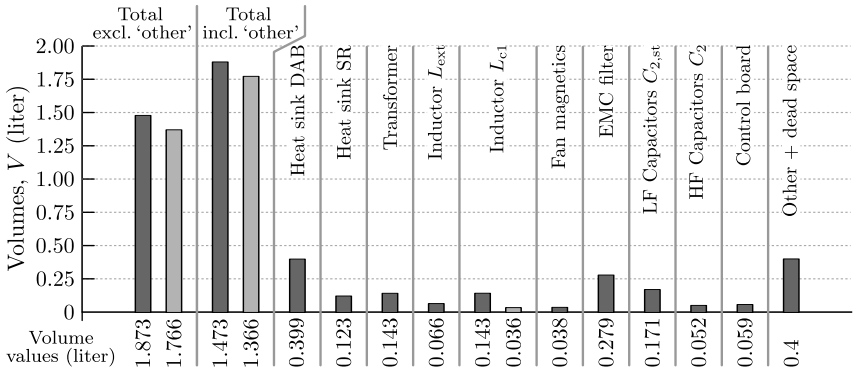


Figure 5.33: Volume contribution of the different converter components for both converter designs A (dark gray bars) and B (light gray bars).

	Design A (Prot.)		Design B (Opt.)	
	V (liter)	ρ (kW/liter)	V (liter)	ρ (kW/liter)
Incl. 'other + dead space'	1.87	2	1.76	2.1
Excl. 'other + dead space'	1.47	2.5	1.36	2.7
Packing factor f_{pack}	1.47/1.87 = 0.79		1.36/1.76 = 0.77	

Table 5.11: Converter power density values (at 3.7 kW, nominal input power).

regarding converter design B) are the same as for converter design A (prototype converter), the volume reduction achieved for the improved converter design B only results from the smaller size of the (improved) primary side commutation inductor L_{c1}, leading to a volume reduction of 0.107 liter.

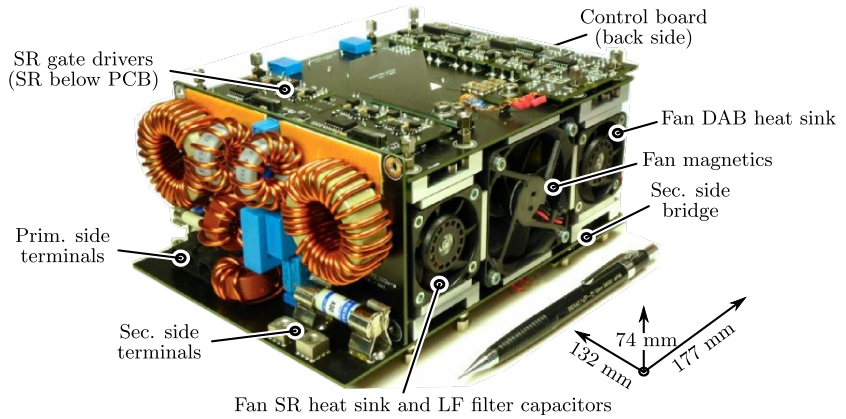
The power density values (ρ) that correspond with the total volumes in Figure 5.33, calculated for the nominal input power of 3.7 kW, are listed in Table 5.11. A high power density of approximately 2 kW/liter is achieved for the prototype converter (i.e. design A) while the power density of the improved converter design (i.e. design B) is around 2.1 kW/liter. When only considering the volume occupied by the main converter components, i.e. neglecting the 'dead space' and the volume occupied by the measurement circuits, PCBs, and gate drive units, the power densities are respectively 2.5 and 2.7 kW/liter. This means that there is still room for reducing the total volume of the system by a more effective assembly of the components. By dividing the volume value 'total, excl. other' by the volume value 'total, incl. other', the packing factor f_{pack} is obtained, being a measure of how 'good' the different components are assembled. The packing factors for converter designs A and B are respectively $f_{\text{pack,A}} = 0.786$ and $f_{\text{pack,B}} = 0.774$ (see Table 5.11), being rather average.

5.6.3 Prototype Converter Realization

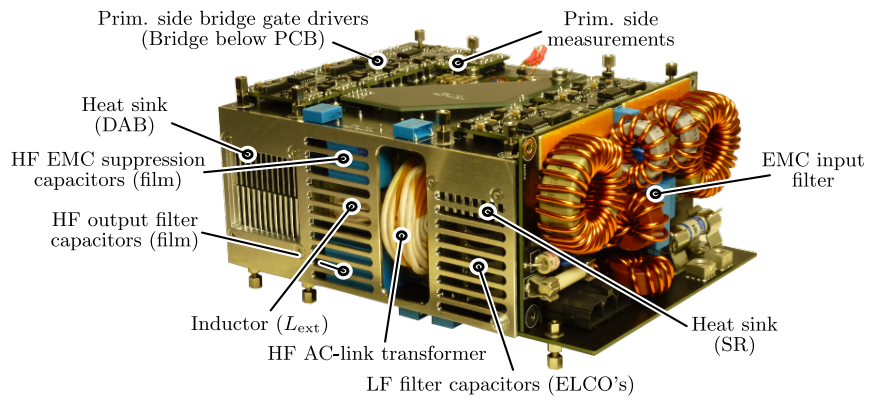
The 3.7 kW, single-phase, single-stage, bidirectional and isolated DAB AC–DC converter prototype system developed in this work, being realized in accordance with converter design A, is shown in Figure 5.34. Figure 5.34(c) depicts the pre-developed 3D CAD model of the system.

As mentioned in Section 5.2.3, the primary side commutation inductance L_{c1} (see Figure 5.11, left inset) was originally not included in the hardware design, but is added in a later phase in order to enable full-operating-range CDCB ZVS operation according to the ZVS verification method proposed in Section 3.3.2 and using the CDCB ZVS modulation schemes subsequently derived in Chapter 4. Although not shown in Figure 5.34, during testing L_{c1} was connected to the prototype converter with the screws that are located on the top power PCB (i.e. using the connection terminals of the HF AC-link transformer and the main inductor L_{ext}). Also, the volume of this inductor is included in the results for the system's volume and power density, which are listed in Table 5.11.

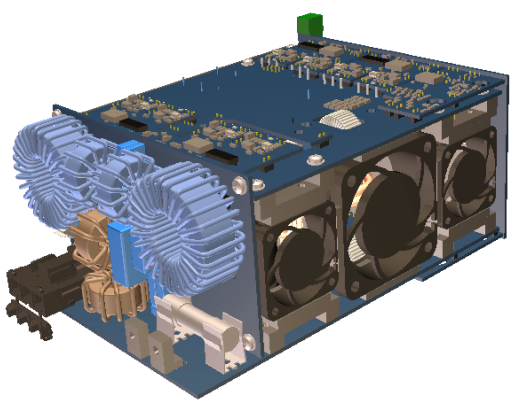
Lastly, in Figures 5.35 and 5.36 the converter losses and the corresponding conversion efficiencies (calculated) of the prototype DAB AC–DC converter (i.e. regarding converter design A), at different output voltages (nominal AC input voltage of $V_{\mathrm{AC}} = V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$), are shown. Figure 5.35 is obtained using the numerically derived ZVS modulation scheme (cf. Section 4.1) while Figure 5.36 is obtained using the semi-analytically derived ZVS modulation scheme (cf. Section 4.3). Only a minor difference (around 0.25 % at maximum) can be noticed between the efficiency curves at different output voltages, i.e. the efficiency is highest for the lowest output voltage and lowest for the highest output voltage. In Section 6.2.2 of Chapter 6 these (calculated) efficiency curves are compared with the efficiencies obtained (measured) from the 3.7 kW DAB AC–DC converter prototype shown in Figure 5.34, as well as with the efficiency curves of several (similar) state-of-the-art dual-stage prototype systems reported in literature (see Section 6.2.3).



(a)



(b)



(c)

Figure 5.34: 3.7 kW, single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter prototype system.

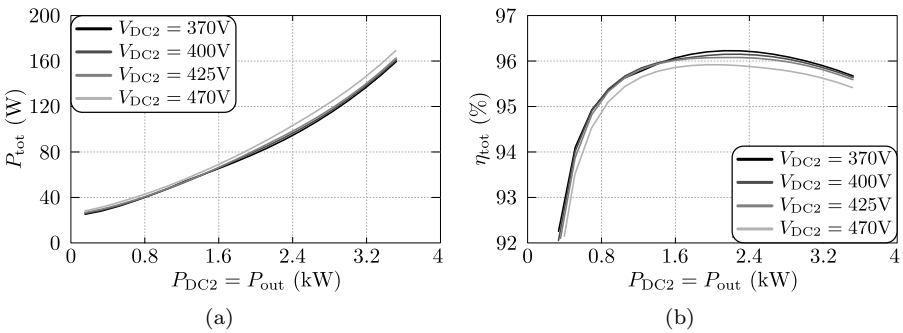


Figure 5.35: (a) Total losses and (b) the corresponding conversion efficiencies (calculated) of the prototype DAB AC–DC converter, at different output voltages (nominal AC input voltage of $V_{\text{AC}} = V_{\text{AC,nom}} = 230\ \text{V}_{\text{rms}}$), obtained using the numerically derived ZVS modulation scheme (cf. Section 4.1).

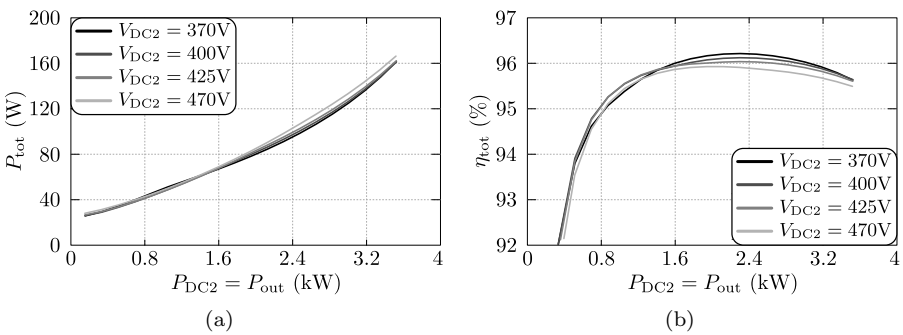


Figure 5.36: (a) Total losses and (b) the corresponding conversion efficiencies (calculated) of the prototype DAB AC–DC converter, at different output voltages (nominal AC input voltage of $V_{\text{AC}} = V_{\text{AC,nom}} = 230\ \text{V}_{\text{rms}}$), obtained using the semi-analytically derived ZVS modulation scheme (cf. Section 4.3).

5.7 Conclusion

Based on the values for the circuit level variables L, L_{c1}, L_{c2}, and n_1/n_2, and based on the CDCB ZVS modulation schemes derived in Chapter 4 (i.e. according to the numerical, the analytical, and the semi-analytical approach), in this chapter the main functional elements of the investigated single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter are designed. As explained in the introduction of this chapter, thereby the partial converter functions are separated and outer (global) optimization loops, i.e. with regard to the circuit level variables and the switching frequency, are omitted. Nevertheless, state-of-the art design methods/procedures, models for the component losses, and volume models are combined with custom developed (local) optimization algorithms in order to obtain a high-efficiency and high-power-density converter design that is in compliance with the system requirements specified in Table 1.1 of Section 1.3.

The summation of the losses and volumes of the individual converter components, which are designed in the different sections of this chapter, leads to the overall performance (i.e. with regard to the conversion efficiency and the power density) of the investigated single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter. The prototype converter system developed in this work is realized in accordance with converter design A, which is implemented using heat sink designs A (see Section 5.1) and using inductor/transformer designs A (see Section 5.2), resulting in:

- A high (calculated) conversion efficiency, which is above 95 % for input powers higher than 20 % of the nominal input power, with a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is around 96.1 % and the efficiency at nominal input power approximately 95.6 %;
- A high power density of approximately 2 kW/liter. When only considering the volume occupied by the main converter components, i.e. neglecting the 'dead space' and the volume occupied by the measurement circuits, PCBs, and gate drive units, the power density is 2.5 kW/liter, resulting in a packing factor of $f_{\text{pack}} = 0.786$, being rather average. This means that there is still room for reducing the total volume of the system and thus increasing the power density by a more effective assembly of the components.

An improved converter design (referred to as converter design B) is possible by using further optimized heat sink designs (i.e. heat sink designs B; see Section 5.1) and further optimized inductor/transformer designs (i.e. inductor/transformer designs B; see Section 5.2), resulting in:

- A conversion efficiency that is above 95.6 % for input powers higher than 20 % of the nominal input power, with again a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is now around 96.75 % and the efficiency at nominal input power approximately 96 %;
- A power density of approximately 2.1 kW/liter, and 2.7 kW/liter when only considering the volume occupied by the main converter components. The packing factor for converter design B is $f_{\text{pack}} = 0.774$.

As for converter design B the outer dimensions of the adjusted components, i.e. the heat sinks and the DAB's magnetic components, stay the same (except for the dimensions of the primary side commutation inductor L_{c1}), these adjustments do not imply a complete redesign of the mechanical assembly, enabling simple replacement. Note that the efficiency enhancement that is achieved for converter design B is mainly the result of the improved design of the primary side commutation inductor L_{c1} and the HF AC-link transformer.

In order to comply with the CISPR 22 Class B standard for conducted emission (CE), an electromagnetic compatibility (EMC) filter is designed. Since the initial design of the differential mode (DM) filter part is based on an inadequate current-based (CB) ZVS DAB modulation scheme, the attenuation provided by the DM input filter used in the final prototype converter is slightly too low for complying with the standard. This can be overcome through a minor filter modification, which does not imply a substantial increase of the filter volume, neither it has a noticeable effect on the other filter characteristics and the achievable power factor. Regarding the CM filter, the selection of the filter architecture and the determination of the CM component values are based on intuition, rather than on modeling and optimization. Therefore it cannot be assured that the CM filter complies with the standard.

Further conclusions are:

- The applied modulation scheme (i.e. the numerically, the analytically, and the semi-analytically derived schemes) has a negligible impact on the total converter losses and thus on the efficiency of the system;
- The semiconductor power switches are the biggest contributors to the overall losses, confirming the assumption made in Section 4.1.1 of Chapter 4, regarding the determination of the cost function applied for the numerical approach used to determine an optimal CDCB ZVS modulation scheme for the DAB;
- Only a minor difference (around 0.25 % at maximum) can be noticed between the efficiency curves at different output voltages, i.e. the efficiency is highest for the lowest output voltage and lowest for the highest output voltage;

- The required DM filter attenuation is slightly lower for the numerically derived ZVS modulation scheme than for the analytically and the semi-analytically derived schemes. This can be explained by the fact that for the numerically derived scheme switching frequency modulation is applied at high v_{DC1}, which is not the case for the other schemes;
- The simulated low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard for Class A equipment are well below the limits.

As far as the calculations/simulations presented in this chapter are correct, at this point the converter requirements specified in Table 1.1 of Section 1.3 are achieved, though there are still uncertainties regarding the EMC compliance. In the next chapter the (calculated) efficiency curves are compared with the efficiencies obtained (measured) from the 3.7 kW DAB AC–DC converter prototype, as well as with the efficiency curves of several (similar) state-of-the-art dual-stage prototype systems reported in literature (see Section 6.2.3).

6

Measurement Setup and Experimental Results

In the previous chapter, the different functional elements of the investigated single-phase, single-stage, bidirectional and isolated DAB AC–DC converter are designed, the realization of the converter prototype is detailed, and the global performance of the system is calculated. This chapter presents the results of an extensive system characterization whereby it is experimentally verified whether the predicted performance is effectively reached. In order to validate the theoretical analysis, i.e. the steady-state converter model and the ZVS analysis presented in Chapter 3, as well as the CDCB ZVS modulation schemes proposed in Chapter 4, first a DC–DC system characterization is performed, which allows to investigate if the measured HF AC-link voltages and currents are in agreement with the calculated waveforms and, consequently, if ZVS operation is achieved as predicted. Subsequently, an AC–DC system characterization is presented, allowing to evaluate the performance of the prototype converter with regard to the reached efficiency and with regard to the quality of the AC input power. Lastly, the system is briefly compared with several (similar) state-of-the-art dual-stage prototype systems reported in literature. The chapter starts with detailing the implementation of the measurement setup that is used to perform above characterizations.

6.1 Measurement Setup

In order to be able to test the prototype system in a flexible way, a dedicated measurement setup is developed. This setup allows to perform DC–DC as well as AC–DC measurements. In order to evaluate the efficiency and the power quality of the AC input power, during DC–DC and AC–DC operation, the input side (AC-side) and the output side (DC-side) of the DAB AC–DC converter are connected to the voltage and current input terminals of a high-precision power analyzer (see Section 6.2).

6.1.1 Setup for DC–DC Testing

Figure 6.1 shows the principle schematic of the test setup used to perform DC–DC measurements on the prototype converter. Thereby, a 15 kVA KEB COMBIVERT frequency inverter [140] is used in order to realize two buck-boost DC–DC converters with controllable DC output voltage. The DC-bus capacitance C_{bus} of the KEB inverter is charged to a bus voltage of about 600 V by a motor-generator group that is connected to the input terminals of the inverter's diode bridge rectifier. Using two bridge legs of the 3-leg inverter bridge, and using two external inductors $L_{\text{bb},1}$ and $L_{\text{bb},2}$ combined with two electrolytic DC-bus capacitor banks $C_{\text{bb},1}$ and $C_{\text{bb},2}$, the two mentioned bidirectional buck-boost DC–DC converters are realized.

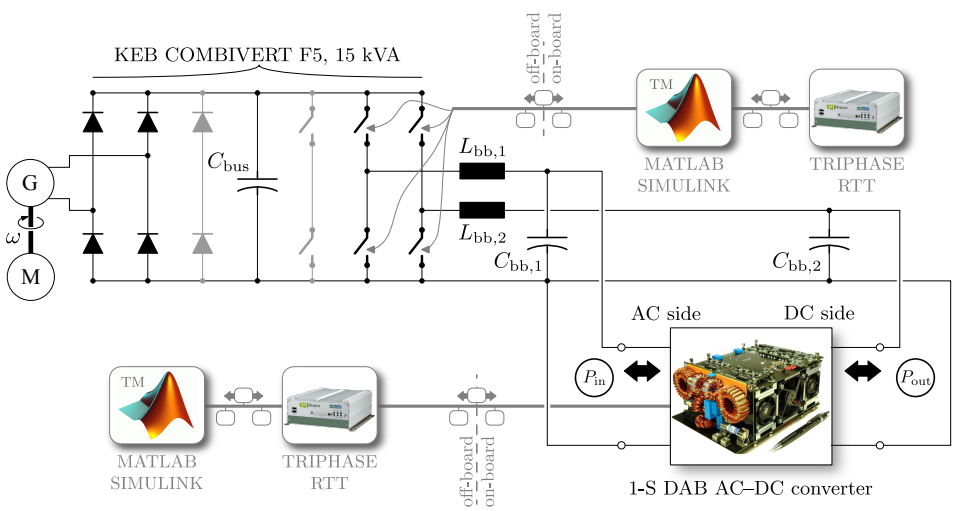


Figure 6.1: Test setup for DC–DC testing of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter.

The input terminals and the output terminals of the DAB AC–DC converter under test are connected to the terminals of respectively $C_{\mathrm{bb},1}$ and $C_{\mathrm{bb},2}$. The voltages across these capacitor banks can be precisely controlled by PWM modulation of the corresponding bridge legs of the KEB inverter. This is done using a dedicated control board developed by Triphase NV [139], which communicates over Ethernet with an off-board PC-based Real-Time Target (RTT). The latter is programmed and operated through Matlab/Simulink$^{\mathrm{TM}}$ where the PI controllers for the two buck-boost DC–DC converters are implemented (i.e. by means of an inner current control loop and an outer voltage control loop). As explained in Section 5.5, and as can be seen from Figure 6.1, the DAB AC–DC converter under test is controlled using the same platform. Consequently, two Matlab/Simulink$^{\mathrm{TM}}$ models (one for the buck-boost DC–DC converters and one for the DAB AC–DC converter under test) are required, which run on one single design PC. During testing, energy circulates from the inverter's DC-bus, via one of the two buck-boost DC–DC converters, towards the DAB AC–DC converter, and back to the inverter's DC-bus via the second buck-boost DC–DC converter. In a similar way, energy can also flow in the opposite direction and thus the setup allows for bidirectional power flow. As a result, a very flexible test setup is realized, enabling DC–DC characterization of the DAB AC–DC converter, in both power flow directions, and with DC voltages that can easily be adjusted. Note that, due to the energy circulation, only the loss energy has to be provided by the motor-generator group.

6.1.2 Setup for AC–DC Testing

For AC–DC testing of the DAB AC–DC converter, the test setup shown in Figure 6.1 is slightly modified. As can be seen from Figure 6.2, the AC input terminals of the DAB AC–DC converter are now connected to a California Instruments 3 x 3001 iX general purpose AC power source [141] instead of to capacitor bank $C_{\mathrm{bb},1}$, while the DC output terminals are still connected to capacitor bank $C_{\mathrm{bb},2}$. The AC power source thus provides AC power to the AC input port of the DAB AC–DC converter. The energy that leaves the converter at its DC output port flows to the KEB inverter's DC-bus via the buck-boost DC–DC converter that still controls the voltage across $C_{\mathrm{bb},2}$. The second buck-boost DC–DC converter is now controlled in order to provide the converted energy to a resistive load, which is connected to capacitor bank $C_{\mathrm{bb},1}$. The motor-generator group is still connected to the input terminals of the inverter's diode bridge rectifier in order to keep the voltage across C_{bus} high enough for the two buck-boost DC–DC converters to work properly. Note that the California Instruments general purpose AC power source does not allow to sink energy, and therefore only unidirectional power flow is possible (i.e. from the AC input port of the DAB AC–DC converter to its DC output port). The test setup described above is depicted in Figure 6.3(a), while Figure 6.3(b) shows the California Instruments 3 x 3001 iX AC power source.

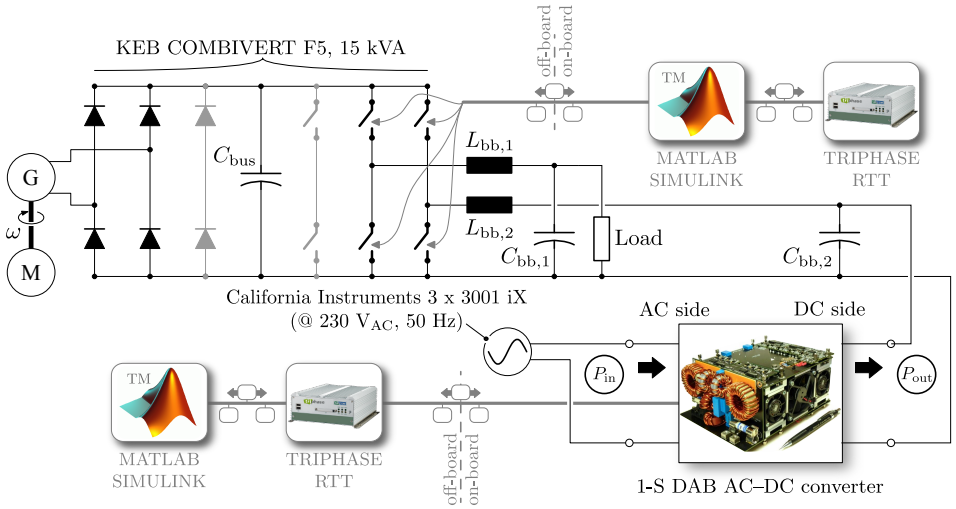


Figure 6.2: Test setup for AC–DC testing of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter.

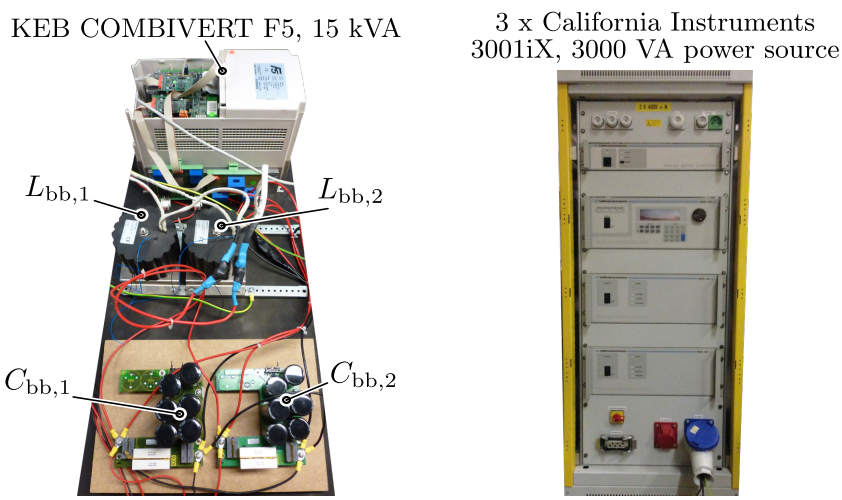


Figure 6.3: (a) Picture of the test setup. (b) California Instruments 3 x 3001 iX general purpose AC power source, providing AC power to the input terminals of the DAB AC–DC converter during AC–DC testing.

6.2 Experimental Results

Below, the results of a DC–DC and an AC–DC characterization of the prototype DAB AC–DC converter system at room temperature ($T_{\mathrm{Am}} \approx 22$ °C) are presented. The DC–DC system characterization has the goal to validate the theoretical analyses outlined in the previous chapters, i.e. the steady-state converter model and the ZVS analysis presented in Chapter 3, as well as the CDCB ZVS modulation schemes proposed in Chapter 4. The goal of the AC–DC characterization is to evaluate the performance of the converter prototype with regard to the reached efficiency and with regard to the quality of the AC input power. Consequently, in this section the following questions are answered:

- Section 6.2.1, DC–DC characterization:
  - Are the steady-state converter model and the ZVS analysis presented in Chapter 3 correct?
  - Are the CDCB ZVS modulation schemes proposed in Chapter 4 valid?
- Section 6.2.2, AC–DC characterization:
  - Is the prototype converter in compliance with the system requirements specified in Table 1.1 of Section 1.3?
  - Is the performance predicted in Chapter 5 effectively reached?

It should be noted that the conversion efficiency and the converter's AC input power quality are evaluated using the Yokogawa WT3000 precision power analyzer, having a power accuracy reading of ±0.02 %. Furthermore, the converter prototype has only been tested using the numerically (acc. to Section 4.1) and the semi-analytically (acc. to Section 4.3) derived CDCB ZVS modulation schemes. This is due to the fact that the analytical approach (see Section 4.2) has been developed during the writing process of this thesis, and no time was left to perform additional measurements. Nevertheless, since the analytically derived scheme is based on the results obtained from the numerically derived scheme, and thus also relies on the CDCB ZVS verification method proposed in Section 3.3.2 (i.e. similar as for the two other schemes), it can be expected that the DAB converter behaves in the exact same way regarding ZVS operation.

6.2.1 DC–DC System Characterization

A first prototype characterization is performed applying DC voltages at both the input (AC-side) and at the output (DC-side) terminals of the DAB AC–DC converter. Figures 6.5-6.7 show the HF AC-link currents and voltages at three different operating points of the DAB:

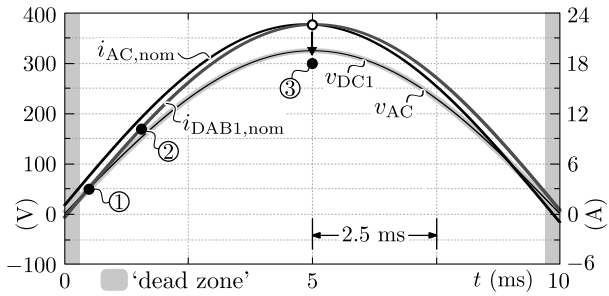


Figure 6.4: Three DAB operating points for which the HF AC-link currents and voltages shown in Figures 6.5-6.7 are captured during DC–DC operation.

- Figure 6.5; operating point 1:
  - $v_{\mathrm{DC1}} = 50$ V, $i_{\mathrm{DAB1}} = 3.05$ A, $V_{\mathrm{DC2}} = 370$ V;
  - $\tau_1 = 2.77$ rad., $\tau_2 = 0.35$ rad., $\phi = -0.7$ rad., $f_{\mathrm{s}} = 83.1$ kHz;
  - switching mode 5.
- Figure 6.6; operating point 2:
  - $v_{\mathrm{DC1}} = 150$ V, $i_{\mathrm{DAB1}} = 10.05$A, $V_{\mathrm{DC2}} = 370$ V;
  - $\tau_1 = 2.81$ rad., $\tau_2 = 1.11$ rad., $\phi = -0.1$ rad., $f_{\mathrm{s}} = 118.5$ kHz;
  - switching mode 5.
- Figure 6.7; operating point 3:
  - $v_{\mathrm{DC1}} = 325.27$ V, $i_{\mathrm{DAB1}} = 18$ A, $V_{\mathrm{DC2}} = 370$ V;
  - $\tau_1 = 3.11$ rad., $\tau_2 = 2.81$ rad., $\phi = 0.4$ rad., $f_{\mathrm{s}} = 116.2$ kHz;
  - switching mode 1^+.

These three DAB operating points are located on the AC trajectory[1] depicted in Figure 6.4, which corresponds with the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, the nominal AC input current of $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$, and a power factor of PF = 0.999. Furthermore, the worst case (i.e. regarding ZVS operation) output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V is used. Regarding operating point 3, it is not the point on the line $I_{\mathrm{AC,P}} = I_{\mathrm{AC,P,nom}} = 16\ \mathrm{A_{rms}}$ that is measured as here the power transfer would be as high as 7.4 kW. In continuous DC–DC operation this would cause an overtemperature, and therefore i_{DAB1} is limited to 18 A for operating point 3 (see Figure 6.4).

[1]Remind that the values for i_{DAB1} that are applied during the half cycle in order to achieve the requested AC line current and PF, are calculated using control equation (3.12).

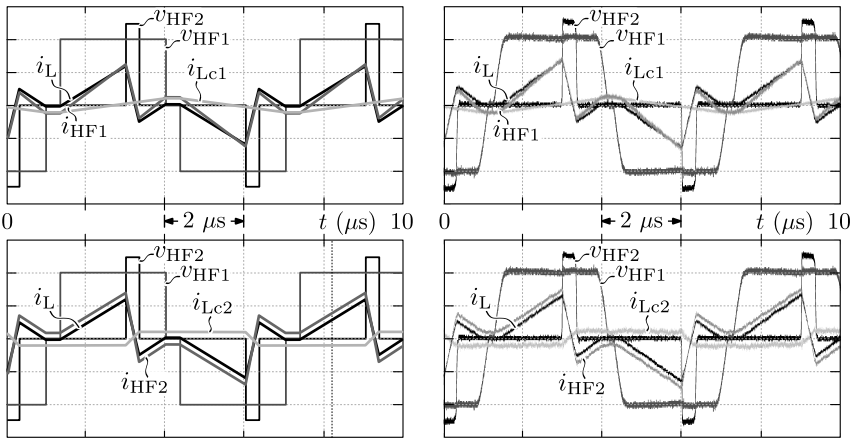


Figure 6.5: Calculated and measured HF AC-link currents and voltages at one particular point (i.e. operating point 1) of the AC-trajectory depicted in Figure 6.4. Voltage and current scale, v_{HF1}: 25 V/div., v_{HF2}: 150 V/div., i_x: 10 A/div.

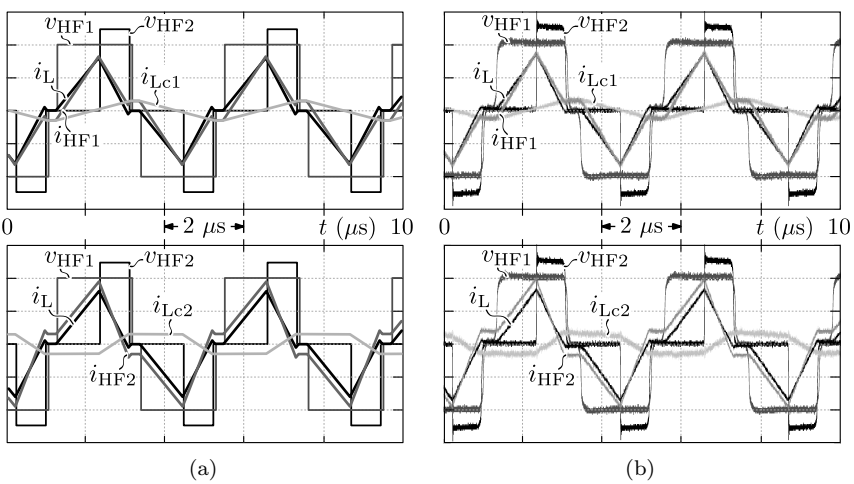


Figure 6.6: Calculated and measured HF AC-link currents and voltages at one particular point (i.e. operating point 2) of the AC-trajectory depicted in Figure 6.4. Voltage and current scale, v_{HF1}: 75 V/div., v_{HF2}: 150 V/div., i_x: 15 A/div.

The left insets of Figures 6.5-6.7 show the simulated waveforms while the right insets depict the measured waveforms[2]. The top insets of the figures correspond

[2]Noted that, for illustration, the presented waveforms are obtained using the numerically derived CDCB ZVS modulation scheme (see Section 4.1), and for positive power flow. Similar

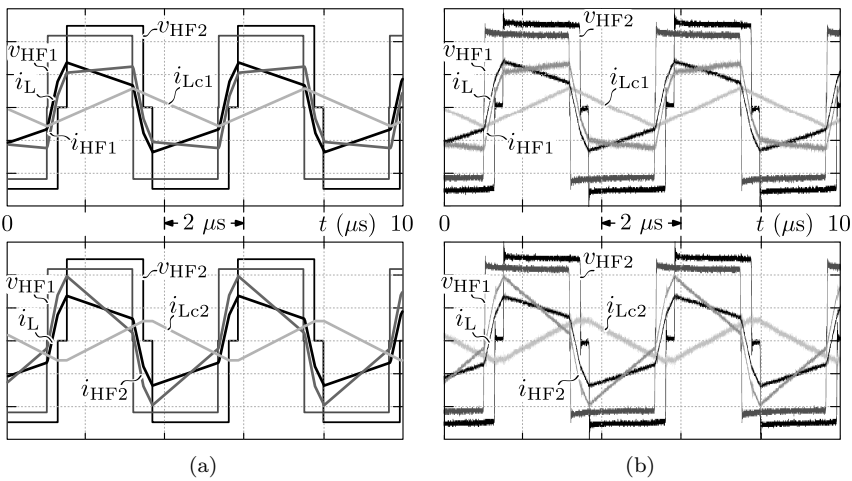


Figure 6.7: Calculated and measured HF AC-link currents and voltages at one particular point (i.e. operating point 3) of the AC-trajectory depicted in Figure 6.4. Voltage and current scale, v_{HF1}: 150 V/div., v_{HF2}: 150 V/div., i_x: 20 A/div.

with the primary side bridge quantities (voltages and currents) while the bottom insets correspond with the secondary side bridge quantities. It can be seen that the measured HF AC-link voltages and currents are in very good agreement with the calculated waveforms. The values of the HF AC-link currents (i_{HF1} and i_{HF2}) at the different switching instances are quasi equal to the calculated values. The same goes for the modulation angles and the switching frequency. It can also been seen that the commutation currents i_{Lc1} and i_{Lc2} are injected into the active bridges, proving the effectiveness of the addition of commutation inductances L_{c1} and L_{c2} in the HF AC-link of the DAB converter. In a similar way, more waveforms are captured at distinct points within the whole operating range (i.e. according to Figure 3.6) of the DAB, and CDCB ZVS operation is successfully verified by visual inspection of these waveforms. Therewith, the correctness of the steady-state converter model and the CDCB ZVS verification method presented in Chapter 3, the validity of the CDCB ZVS modulation schemes proposed in Chapter 4, and the successful implementation of the converter hardware components and the control unit designed in Chapter 5, is proven.

Although not representative for AC–DC power conversion, in addition, the conversion efficiency (see Figure 6.8) is evaluated at all inspected operating points. Very high efficiencies of up to 97 % are measured in DC–DC operation of the complete DAB AC-DC converter (positive power range), excluding the auxiliary

results are obtained for the semi-analytically derived modulation scheme, as also for negative power flow.

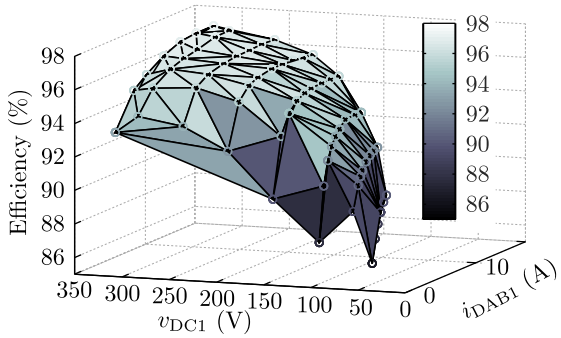


Figure 6.8: Measured efficiency in DC–DC operation of the 1-S DAB AC–DC converter. The measurements are taken at the nominal DC output voltage $V_{DC2} = V_{DC2,nom} = 400$ V, at different DAB input currents i_{DAB1} and input voltages v_{DC1}.

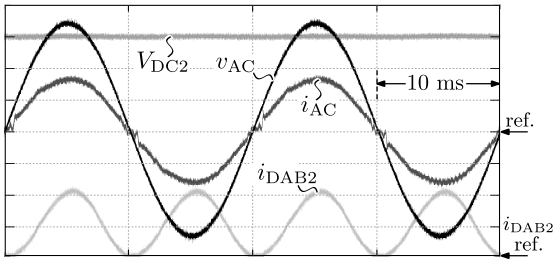
losses related to the gate drive units, the fans, and the control board. Note that these measurements also include the losses in the synchronous rectifier and the EMC input filter. Consequently, the efficiency of the DAB converter only is even higher.

6.2.2 AC–DC System Characterization

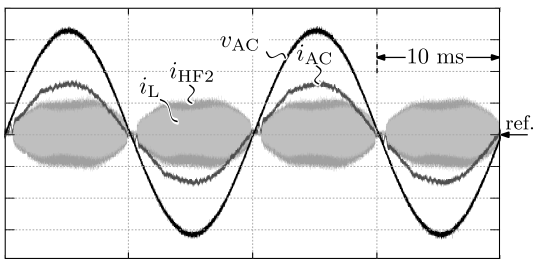
For the AC–DC characterization of the DAB AC–DC converter, the nominal AC input voltage $V_{AC} = 230$ V_{rms} is provided to the input (AC-side) of the converter while at its output (DC-side) a DC voltage is applied. Figure 6.9 depicts the measured AC waveforms (AC-side and DC-side) at different AC input currents and DC output voltages:

- Figure 6.9(a); operating point 1:
  - $V_{AC} = 230$ V_{rms}, $V_{DC2} = 450$ V, $I_{AC,P} = I_{AC,P,nom} = 16$ A_{rms}.
- Figure 6.9(b); operating point 2:
  - $V_{AC} = 230$ V_{rms}, $V_{DC2} = 370$ V, $I_{AC,P} = 0.6 \cdot I_{AC,P,nom} = 9.6$ A_{rms}.
- Figure 6.9(c); operating point 3:
  - $V_{AC} = 230$ V_{rms}, $V_{DC2} = 425$ V, $I_{AC,P} = 0.2 \cdot I_{AC,P,nom} = 3.2$ A_{rms}.

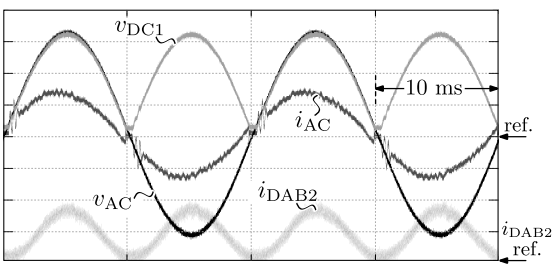
The system is successfully tested within the full power range (up until an output power of 3.7 kW), showing waveforms with little distortion (see Figure 6.9), and which are in very good agreement with the waveforms obtained from simulations.



(a) Voltage and current scale: v_{AC}: 100 V/div., i_{AC}: 12.5 A/div., V_{DC2}: 150 V/div., i_{DAB2}: 7.5 A/div.



(b) Voltage and current scale: v_{AC}: 100 V/div., i_{AC}: 7.5 A/div., i_L: 30 A/div., i_{HF2}: 30 A/div.



(c) Voltage and current scale: v_{AC}: 100 V/div., i_{AC}: 3 A/div., v_{DC1}: 100 V/div., i_{DAB2}: 2 A/div.

Figure 6.9: Measured waveforms in AC–DC operation of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter prototype, at different AC input currents and DC output voltages, and at the nominal AC input voltage of $V_{AC} = V_{AC,nom} = 230\ V_{rms}$.

Figure 6.10 shows the measured performance of the converter prototype with regard to the reached efficiency and with regard to the quality of the AC input power. Note that Figure 6.10(a) is obtained using the numerically derived CDCB ZVS modulation scheme (acc. to Section 4.1) while Figure 6.10(b) is obtained using the semi-analytically derived CDCB ZVS modulation scheme (acc. to Section 4.3).

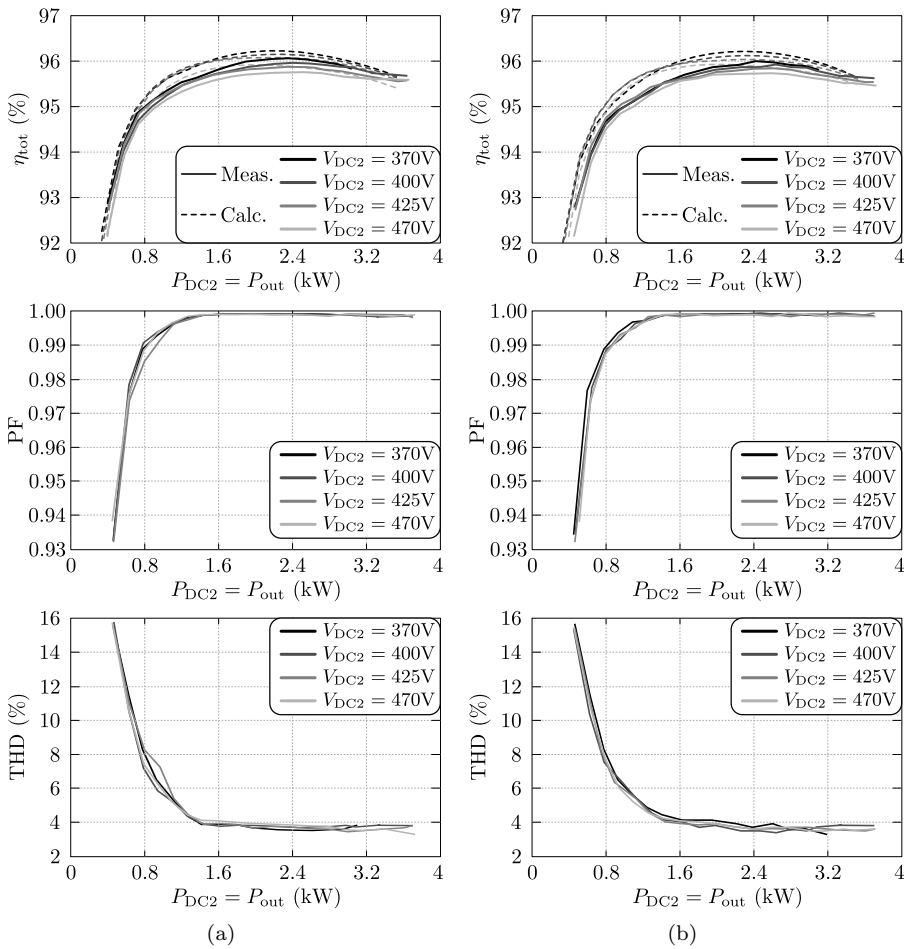


Figure 6.10: Measured efficiency, total harmonic distortion THD, and (true) power factor PF in AC–DC operation, (a) applying the numerically derived CDCB ZVS modulation scheme according to Section 4.1 and (b) applying the semi-analytically derived CDCB ZVS modulation scheme according to Section 4.3. The measurements are taken at the nominal AC input voltage of $V_{\mathrm{AC}} = V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$, in the complete power range (up to 3.7 kW output power), and at different DC output voltages.

The measured efficiency (see solid lines) is depicted in the top figure inset and corresponds well with the efficiency calculated in Chapter 5 (see dashed lines). Although the trends match very well, a slight discrepancy (mostly less than 0.4 %) can be noticed between the calculated and the measured efficiencies. This

might require further refinement of the loss models employed in Chapter 5. For the numerically derived modulation scheme (see Figure 6.10(a)), the measured efficiencies are higher than 95 % within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96 % and the efficiency at nominal output power approximately 95.6 % (curve for the nominal output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400$ V). As predicted by the calculations, only a minor difference (around 0.25-0.3 % at maximum) can be noticed between the efficiency curves at different output voltages, i.e. the efficiency is highest for the lowest output voltage and lowest for the highest output voltage. The measured efficiencies more than meet the requirements defined in Table 1.1 of Section 1.3, goaling for a conversion efficiency of $\eta > 95$ % at the nominal operating point and $\eta > 93$ % within reasonable voltage and current ranges. Note that for the semi-analytically derived modulation scheme (see Figure 6.10(b)), the efficiency is slightly lower than for the numerically derived modulation scheme. As not predicted by the calculations, this phenomenon needs to be further investigated but, however, might relate to the way the on-board measurement circuits are implemented, i.e. timing issues can occur due to the use of sample-based measurements. Therefore, it would be better to use Delta-Sigma measurements or to apply moving average filtering on the samples. Furthermore, for both modulation schemes, a (true) power factor (PF) close to unity, and a low total harmonic distortion (THD) of the AC input current of around 4 %, are obtained within the major part of the output power range and within the whole output voltage range. Note that, although the power source did not allow to sink energy, and therefore only positive power flow could be applied, the results for negative power flow would be similar since the DAB is completely symmetric. An improved THD would be achieved by replacement of the on-board sample-based measurements circuit by Delta-Sigma measurements.

This makes that, regarding conversions efficiency, system power density, PF, and THD, the converter requirements specified in Table 1.1 of Section 1.3 are achieved. It should be reminded (see Chapter 5) that a considerable efficiency and power density enhancement can be obtained by using slightly modified heat sink designs (i.e. heat sink designs B; see Section 5.1) and inductor/transformer designs (i.e. inductor/transformer designs B; see Section 5.2). The low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [57] for Class A equipment, have not been measured. Nevertheless, in simulation the harmonics are well below the limits (see Figure 5.26 in Section 5.4.1 of Chapter 5). Furthermore, electromagnetic compatibility (EMC) compliance with the CISPR 22 Class B standard [56] could not be experimentally verified due to the unavailability of the required measurement equipment.

6.2.3 Comparison with the State-of-the-Art

For convenience, in this section the performance of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter developed in this work is briefly compared (i.e. with regard to the conversion efficiency and power density) with the performance of two (similar) state-of-the-art dual-stage prototype systems reported in literature. This comparison, however, is rather illustrative since Performance Indices of different power electronic converters can only be used for objective comparison when the systems are similar with regard to the type of energy conversion, the system specifications (i.e. the input and output voltage ranges, power ranges, EMC and PF requirements, etc.), the applied design and optimization methods/procedures, the considered component technologies and cooling concept, etc.

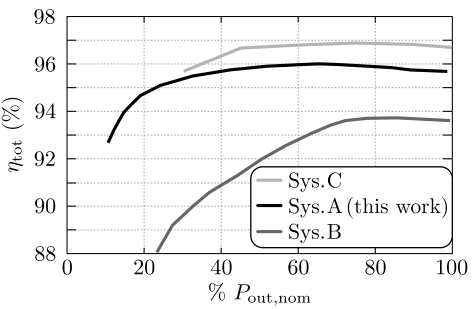
Below the performance of the following three AC–DC converter systems is given:

- System A, see Figure 6.11(a): the single-phase, single-stage, 3.7 kW, **bidirectional** on-board battery charger (1-S DAB AC–DC converter) developed in this work:
  - Nominal input voltage: $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$;
  - Nominal output voltage: $V_{\mathrm{DC2,nom}} = 400$ V;
  - Nominal power: $P = 3.7$ kW.
- System B, see Figure 6.11(b): the single-phase, dual-stage, 3.33 kW, **unidirectional** on-board battery charger (input stage: interleaved boost-type PFC rectifier system with 2 phase-shifted branches, output stage: phase-shift, isolated, ZVS full-bridge DC–DC converter) presented in [20]:
  - Nominal input voltage: $V_{\mathrm{AC,nom}} = 240\ \mathrm{V_{rms}}$;
  - Nominal output voltage: $V_{\mathrm{DC2,nom}} = 400$ V;
  - Nominal power: $P = 3.33$ kW.
- System C, see Figure 6.11(c): the single-phase, dual-stage, 3.33 kW, **unidirectional** telecom power supply module (input stage: resonant transition mode boost-type PFC rectifier system with 3 phase-shifted branches, output stage: phase-shift, isolated, ZVS full-bridge DC–DC converter) presented in [108]:
  - Nominal input voltage: $V_{\mathrm{AC,nom}} = 230\ \mathrm{V_{rms}}$;
  - Nominal output voltage: $V_{\mathrm{DC2,nom}} = 48$ V;
  - Nominal power: $P = 3.33$ kW.

(a) System A (this work)

(b) System B

(c) System C



(d)

Figure 6.11: (a) Demonstrator of system A (this work), (b) demonstrator of system B [20], (c) demonstrator of system C [108], (d) Efficiency curves of the three systems.

Remind that system B [20] is taken as a benchmark for the AC–DC converter developed in this work (see Section 1.3), while system C [108] is the absolute state-of-the-art. Note that the system developed in this work is bidirectional while systems B and C only allow for unidirectional power flow.

The efficiency, expressed as percentage of the nominal output power, and measured at nominal voltage conditions (see above), of the three systems is shown in Figure 6.11(d). The efficiencies obtained with system A (this work) are substantially higher than the efficiencies of the reference converter (system B) presented in [20], while system C (state-of-the-art, [108]) has the highest conversion efficiency. Both systems A and C have a very flat efficiency curve and thus a high partial-load efficiency, while this is not the case for system B.

The power density reached with system A (2 kW/liter, this work) is substantially higher than the 0.66 kW/liter power density of the reference converter (system B) presented in [20], while system C (state-of-the-art, [108]) has the highest power density of 2.5 kW/liter.

6.3 Conclusion

After providing a detailed description of the measurement setup in Section 6.1 of this chapter, in the next section (i.e. Section 6.2) the results of a DC–DC and an AC–DC characterization of the prototype DAB AC–DC converter system at room temperature ($T_{\mathrm{Am}} \approx 22$ °C) are presented. The prototype has only been tested using the numerically (acc. to Section 4.1) and the semi-analytically (acc. to Section 4.3) derived CDCB ZVS modulation schemes. This is due to the fact that the analytical approach (see Section 4.2) has been developed during the writing process of this thesis, and no time was left to perform additional measurements. Nevertheless, since the analytically derived scheme is based on the results obtained from the numerically derived scheme, and thus also relies on the CDCB ZVS verification method proposed in Section 3.3.2 (i.e. similar as for the two other schemes), it can be expected that the DAB converter behaves in the exact same way regarding ZVS operation.

In the **first part** of Section 6.2, the theoretical analyses presented in the previous chapters is validated using a DC–DC system characterization in which DC voltages are applied at both the input (AC-side) and at the output (DC-side) terminals of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter. This allows to investigate if the measured HF AC-link voltages and currents are in agreement with the calculated waveforms and, consequently if ZVS operation is achieved as predicted. It is shown that the measurements are in very good agreement with the simulations. Moreover, CDCB ZVS operation is successfully verified by visual inspection of the waveforms that are captured at distinct operating points within quasi the whole operating range of the DAB. Although not representative for AC–DC power conversion, in addition, the conversion efficiency is evaluated at all inspected 'DC to DC' operating points. Very high efficiencies of more than 97 % are measured in DC–DC operation of the complete DAB AC–DC converter (positive power range), excluding auxiliary (i.e. gate drivers, fans, and control board) losses. Therewith, the correctness of the steady-state converter model and the ZVS analysis presented in Chapter 3, the validity of the CDCB ZVS modulation schemes proposed in Chapter 4, and the successful implementation of the converter components and the control unit designed in Chapter 5, is proven.

In the **second part** of Section 6.2, an AC–DC system characterization is performed in order to evaluate the performance of the prototype converter with regard to the reached efficiency and with regard to the input power quality. The system is successfully tested within the full power range (up until an output power of 3.7 kW), showing waveforms with little distortion, and which are in very good agreement with the waveforms obtained from simulations. Moreover, the measured efficiency corresponds well with the efficiency calculated in Chapter 5. Although the trends match very well, a slight discrepancy (mostly less than 0.4%) can be noticed between the calculated and the measured efficiencies. This might require

further refinement of the loss models employed in Chapter 5. Furthermore, the measured efficiencies are higher than 95 % within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96 % and the efficiency at nominal output power approximately 95.6 %. As predicted by the calculations, only a minor difference (around 0.25-0.3 % at maximum) can be noticed between the efficiency curves at different output voltages, i.e. the efficiency is highest for the lowest output voltage and lowest for the highest output voltage. For the semi-analytically derived modulation scheme, the efficiency is slightly lower than for the numerically derived modulation scheme. As not predicted by the calculations, this phenomenon needs to be further investigated but, however, might relate to the way the on-board measurement circuits are implemented, i.e. timing issues can occur due to the use of sample-based measurements. Lastly, a (true) power factor (PF) close to unity, and a low total harmonic distortion (THD) of the AC input current of around 4 %, are obtained within the major part of the output power range and within the whole output voltage range. This makes that, regarding conversions efficiency, system power density, PF, and THD, the converter requirements specified in Table 1.1 of Section 1.3 are achieved. It should be reminded (see Chapter 5) that a considerable efficiency and power density enhancement can be obtained by using slightly modified heat sink designs and inductor/transformer designs. The low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [57] for Class A equipment, have not been measured. Nevertheless, in simulation the harmonics are well below the limits (see Figure 5.26 in Section 5.4.1 of Chapter 5). Furthermore, electromagnetic compatibility (EMC) compliance with the CISPR 22 Class B standard [56] could not be experimentally verified due to the unavailability of the required measurement equipment.

In the **third part** of Section 6.2, the performance of the single-phase, single-stage, bidirectional, and isolated DAB AC–DC converter is briefly compared (i.e. with regard to the conversion efficiency and power density) with the performance of two (similar) state-of-the-art dual-stage AC–DC converters reported in literature. This comparison, however, is rather illustrative since Performance Indices of different power electronic converters can only be used for objective comparison when the systems are similar with regard to the type of energy conversion, the system specifications (i.e. the input and output voltage ranges, power ranges, EMC and PF requirements, etc.), the applied design and optimization methods/procedures, the considered component technologies and cooling concept, etc. The system developed is this work performs substantially (i.e. with regard to the achieved efficiency and power density) better than the system presented in [20], which is taken as a benchmark (see Section 1.3 of Chapter 1), while a performance close to the absolute state-of-the-art (AC–DC converter presented in [108]) is achieved. Note that the system developed in this work is bidirectional while the benchmark systems only allow for unidirectional power flow.

7

Conclusions and Outlook

7.1 Introduction

Main objective of the thesis— In the presented work, the feasibility and suitability of a single-stage (1-S) dual active bridge (DAB) AC–DC converter for the realization of single-phase, utility interfaced, bidirectional, and isolated energy conversions, is investigated. Thereby, the converter requirements specified in Table 1.1 of Section 1.3, which relate to an on-board, 3.7 kW, EV battery charger, are to be fulfilled.

Main challenge of the work— The selection of the 1-S DAB AC–DC converter topology as the core topic of this thesis is the direct result of a collaboration with industry. Within the course of this collaboration, several major shortcomings in the existing analyses and circuit implementations of DAB converters have come into light, i.e. failures of the converter's semiconductor switching devices were experienced when operating the DAB using (soft-switching) modulation schemes that are available in literature. It is the principle goal of this thesis to tackle the causes of these failures, and to provide solutions for the major shortcomings in the existing analyses of DAB converters. The **main focus** of this work is put on the (re)development of the DAB (soft-switching) modulation schemes and on the provision of essential DAB circuit modifications, rather than on subjecting a set

of preselected topologies with given modulation schemes to the multi-objective optimization (MOO) procedure outlined in Section 1.1.4. In order to validate the presented modeling approach, a **second objective** is to design, build, and test a high-efficiency, high-power-density converter prototype system that is designed in order to meet the requirements specified in Table 1.1 of Section 1.3 and that is developed using state-of-the art design methods/procedures. To some extent, i.e. using local rather than global optimization algorithms, the hardware prototype should be optimized with respect to efficiency and power density. Below, the main results obtained in the course of this Ph.D., and the new contribution of the work are organized per chapter.

7.2 Chapter Overview, and Conclusions per Chapter

7.2.1 Chapter 2: The Dual Active Bridge (DAB) DC–DC Converter

In order to provide the main context of the presented work and in order to motivate the focus of the performed research, in a separate chapter (i.e. Chapter 2), an introduction to the working principle of the soft-switching dual active bridge (DAB) DC–DC converter, which is the main building block of the investigated single-stage (1-S) DAB AC–DC converter, is given. By means of a brief introductory discussion, the shortcomings of the original modulation strategy (i.e. phase-shift modulation, PSM) and soft-switching conditions, and the need for improvements are summarized. Furthermore, a comprehensive overview of the most relevant publications on improved (soft-switching) modulation schemes for DAB converters that have the goal to deal with the deficiencies of the conventional PSM is presented. These publications are classified according their ZVS considerations. It is concluded that regardless their objective, all DAB modulation schemes so far presented are based on 'theoretical' current-based (CB) or energy-based (EB) ZVS analyses. The crucial disadvantage of the CB ZVS modulation schemes is that substantial parts of the calculated ZVS regions involve incomplete bridge commutations due to the presence of parasitic switch capacitances (i.e. the nonlinear output capacitances of the semiconductor power devices), which are not taken into account in the CB ZVS analysis. This inevitably leads to hard-switching operation, reduced conversion efficiency, and, in all probability, destruction of the semiconductor switching devices. The EB ZVS modulation schemes try to deal with this deficiency but, however, still involve difficulties, in particular concerning implementability and accuracy. Furthermore, EB ZVS modulation schemes encompass discontinuous steps in the modulation parameter trajectories, being highly undesirable. This problem relates to the way the HF AC-link of the traditional DAB converter is implemented (i.e. without commutation inductances). Especially when the DAB is operated within

wide input and/or output voltage ranges, such as is the case for the investigated single-stage DAB AC–DC converter, where the input voltage of the DAB is a rectified (folded) sine-wave voltage, the above deficiencies are problematic and lead to significantly increased losses for most operating points. Lastly, after a brief discussion of the different DAB variants, the full bridge - full bridge (FBFB) DAB implementation is selected as the most suitable candidate for the realization of the investigated 1-S DAB AC–DC converter.

7.2.2 Chapter 3: Steady-State Operation of the DAB AC–DC Converter

Chapter 3 consists of three major parts. In the **first part**, the general operating principle of the investigated single-stage (1-S) DAB AC–DC converter is discussed. Based on the equivalent circuit of the converter's AC input side, the operating range (i.e. with regard to the operating conditions specified in Section 1.3) of the DAB DC–DC converter, which is the main building block of the AC–DC converter, is derived. Furthermore, a control equation for the averaged DAB input current that is required in order to achieve a certain requested AC line current is presented. Thereby, the reactive power consumption of the EMC input filter is taken into account, requiring a certain reactive power transfer capability of the DAB. The obtained operating range is the starting point for the calculation procedures outlined in Chapter 4, regarding the derivation of full-operating-range ZVS modulation schemes, and regarding the determination of the DAB's circuit level variables such as the transformer's turns ratio, the inductances values, and the applied switching frequency. In the **second part**, the steady-state analysis of the FBFB DAB is presented, i.e. the fundamental mode equations are derived based on the lossless DAB model while referring to the general considerations regarding the traditional phase-shift modulation (PSM) presented in Chapter 2. All possible degrees of freedom available for controlling the DAB's active bridges are exploited by considering dual-sided duty-cycle modulation (DSPWM) instead of PSM and by including all twelve switching modes that are possible with the (FBFB) DAB converter, providing the highest flexibility regarding the search toward optimal, full-operating-range ZVS modulation schemes in Chapter 4. Furthermore, after reevaluation of the theoretical current-based (CB) ZVS conditions, 'commutation inductance(s)' are introduced which, using a simple calculation example, are shown to be an essential HF AC-link modification in order to achieve full-operating-range ZVS. The effect of commutation inductances on the ZVS operating range is further investigated in Chapter 4. In order to deal with the deficiencies of the CB and EB ZVS considerations, in the **third part**, a novel current-dependent charge-based (CDCB) ZVS verification method is proposed. Thereby the charge that is required to reset the nonlinear, parasitic output capacitances of the semiconductor devices during commutation of the bridge legs, as well as the time dependency of the currents

available for commutation, are taken into account. This results in a more accurate description of the DAB's ZVS conditions, assuring that soft-switching operation with quasi zero switching losses is obtained within the calculated ZVS regions. The presented CDCB ZVS verification method is experimentally verified and is translated into a set of constraints which are used in the calculation procedures presented in Chapter 4. The main contributions presented in Chapter 3 are:

- A new method for the description of the soft-switching (i.e. by virtue of zero voltage switching, ZVS) behavior of DAB converters and a corresponding method which allows to verify whether, for a given set of modulation parameters and circuit variables, ZVS is obtained in all semiconductor power devices of the DAB. This method is named the 'current-dependent charge-based (CDCB) ZVS verification method';
- A complete analysis of all (twelve) switching modes that are possible with the FBFB DAB converter;
- The introduction of 'commutation inductances', which are shown to be an essential HF AC-link modification in order to achieve full-operating-range (CDCB) ZVS of a DAB converter.

7.2.3 Chapter 4: ZVS Modulation Schemes

Chapter 4 is devoted to the derivation of full-operating-range ZVS modulation schemes for the FBFB DAB used in the investigated 1-S DAB AC–DC converter. Three different approaches are presented, all relying on the CDCB ZVS verification method proposed in Section 3.3. After explaining why closed-form solutions, such as presented in [92], for the calculation of the modulation parameters of the DAB are not directly feasible, in a first step a **numerical approach** is introduced, involving an optimization procedure which is based on a constrained numerical minimum search. The numerical nature of the proposed optimization algorithm allows users to freely define the cost function to be minimized. Thereby converter related losses, but also requirements concerning system volume, weight, control, EMC,... can be included. The CDCB ZVS verification method is implemented in the optimization algorithm in the form of constraint functions. Furthermore, the algorithm examines all twelve switching modes that are possible with the (FBFB) DAB converter. Using several calculation examples it is shown that:

- Generally used CB ZVS modulation schemes result in hard-switching operation within large regions of the DAB's operating range;
- Efficient, full-operating-range CDCB ZVS modulation schemes which involve continuous modulation parameter trajectories cannot be obtained with the traditional HF AC-link implementation of the DAB;

- 'Commutation inductance(s)', which benefit the ZVS conditions due to the injection of small reactive currents in the active bridges, are absolutely essential in order to obtain a full-operating-range (CDCB) ZVS modulation scheme that involves continuous modulation parameter trajectories;
- For each power flow direction only two out of the twelve possible switching modes are feasible for efficient ZVS operation. These are mode 1 (high power mode) and mode 5 (low power mode), i.e. conform Chapter 3, forming the basis of all derived ZVS modulation schemes.

Based on the results acquired from the numerical approach, in a second step an **analytical approach** is proposed, providing a general, directly employable closed-form analytical solution for the calculation of the modulation parameters which lead to full-operating-range CDCB ZVS operation. Therewith, the direct application to a given (FBFB) DAB converter is facilitated, provided that commutation inductors with appropriate inductance value are present in the HF AC-link. Thereafter, a **semi-analytical approach** is presented as an alternative method to derive a full-operating-range CDCB ZVS modulation scheme for the DAB. This approach is named the 'semi-analytical approach' since it combines analytical equations for the modulation parameters with an inner, numerical optimization algorithm.

A comparison of the three approaches shows a minor deviation of the calculated cost functions, and of the RMS and peak values of the resulting HF AC-link currents. From the different optimization examples it is concluded that:

- The DAB's ZVS constraint functions are the determining factor for the final values of the modulation parameters and, consequently, the cost function is of less importance in the determination of a ZVS modulation scheme;
- The previous conclusion promotes the use of the analytical approach as it is directly implementable and requires the least computational power;
- At low DAB input voltages, the switching frequency has to be lowered in order to obtain ZVS. If not doing so, very low commutation inductance values are required, resulting in unacceptably high HF AC-link currents.

Furthermore, this chapter also provides guidelines for the effective selection of the circuit level variables (transformer's turns ratio, the inductances values,...) and of the switching frequency pattern to be applied. The impact of the three calculation approaches on the losses in the different converter components and on the EMC input filter requirements is further investigated in Chapter 5. The main contributions presented in Chapter 4 are:

- A generally applicable, numerical calculation procedure for the derivation of optimal, full-operating-range CDCB ZVS modulation schemes for DAB

converters. Contrary to the DAB analyses reported in literature, the proposed numerical optimization algorithm examines all twelve switching modes that are possible with the (FBFB) DAB converter;

- A generally applicable, directly employable analytical solution for the calculation of full-operating-range CDCB ZVS modulation schemes for DAB converters;
- A generally applicable, semi-analytical calculation procedure for the derivation of full-operating-range CDCB ZVS modulation schemes for DAB converters;
- Guidelines for the effective selection of the circuit level variables (transformer's turns ratio, the inductances values,...) and of the switching frequency pattern to be applied.

7.2.4 Chapter 5: Modeling of the Main Converter Components

Based on the values for the circuit level variables and based on the CDCB ZVS modulation schemes derived in Chapter 4, in Chapter 5 the main functional elements of the DAB AC–DC converter are designed. Thereby the partial converter functions are separated and outer (global) optimization loops (i.e. with regard to the circuit level variables and switching frequency) are omitted. Nevertheless, state-of-the art design methods/procedures, models for the component losses, and volume models are combined with custom developed (local) optimization algorithms in order to obtain a high-efficiency and high-power-density converter design that is in compliance with the system requirements specified in Table 1.1 of Section 1.3. The summation of the losses and volumes of the individual converter components, which are designed in the different chapter sections, leads to the overall performance of the DAB AC–DC converter, resulting in:

- A high (calculated) conversion efficiency, which is above 95 % for input powers higher than 20 % of the nominal power, with a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is around 96.1 % and the efficiency at nominal power approximately 95.6 %;
- A high power density of approximately 2 kW/liter. Note that there is still room for reducing the total volume of the system and thus increasing the power density by a more effective assembly of the components.

Furthermore, it is shown that an improved converter design is possible by using further optimized heat sink designs and further optimized inductor/transformer designs, yielding:

- A conversion efficiency that is above 95.6 % for input powers higher than 20 % of the nominal power, with a very flat efficiency curve and thus a high partial-load efficiency over the power range. The peak efficiency is around 96.75 % and the efficiency at nominal power approximately 96 %;
- A power density of approximately 2.1 kW/liter.

As for the improved converter design the outer dimensions of the adjusted components stay the same (except for the dimensions of the primary side commutation inductor), these adjustments do not imply a complete redesign of the mechanical assembly, enabling simple replacement.

In order to comply with the CISPR 22 Class B standard for conducted emission (CE), an electromagnetic compatibility (EMC) filter is designed. Since the initial design of the differential mode (DM) filter part is based on an inadequate current-based (CB) ZVS DAB modulation scheme, the attenuation provided by the DM input filter used in the final prototype converter is slightly too low for complying with the standard. This can be overcome through a minor filter modification, which does not imply a substantial increase of the filter volume, neither it has a noticeable effect on the other filter characteristics and the achievable power factor. Regarding the CM filter, the selection of the filter architecture and the determination of the CM component values are based on intuition, rather than on modeling and optimization. Therefore it cannot be assured that the CM filter complies with the standard.

Further conclusions are:

- The applied modulation scheme (i.e. the numerically, the analytically, and the semi-analytically derived schemes) has a negligible impact on the total converter losses and thus on the efficiency of the system;
- The semiconductor power switches are the biggest contributors to the overall losses;
- Only a minor difference (around 0.25 % at maximum) can be noticed between the efficiency curves at different output voltages;
- The required DM filter attenuation is slightly lower for the numerically derived ZVS modulation scheme than for the analytically and the semi-analytically derived schemes. This can be explained by the fact that for the numerically derived scheme switching frequency modulation is applied at high v_{DC1}, which is not the case for the other schemes;
- The simulated low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard for Class A equipment are well below the limits.

As far as the calculations/simulations presented in this chapter are correct, at this point the converter requirements specified in Table 1.1 of Section 1.3 are achieved, though there are still uncertainties regarding the EMC compliance. The main contributions presented in Chapter 5 are:

- A guideline for the design, the optimization, and the realization of single-phase, single-stage, bidirectional, and isolated DAB AC–DC converters;
- A framework that includes detailed loss and volume models for the investigated DAB AC–DC converter, enabling local and global system optimizations regarding efficiency and power density, as well as comprehensive comparisons with alternative topology candidates;
- A multi-objective (i.e. with respect to the losses and/or the volume) optimization procedure for the design of magnetic components (i.e. inductors and transformers).

7.2.5 Chapter 6: Measurement Setup and Experimental Results

After providing a detailed description of the measurement setup, the results of a DC–DC and an AC–DC characterization of the prototype DAB AC–DC converter system at room temperature ($T_{\mathrm{Am}} \approx 22$ °C) are presented.

The theoretical analyses presented in the previous chapters are validated using a DC–DC system characterization in which DC voltages are applied at both the input (AC-side) and at the output (DC-side) terminals of the DAB AC–DC converter prototype. It is shown that the measured HF AC-link voltages and currents are in very good agreement with the calculated waveforms and, consequently, that ZVS operation is achieved as predicted. Although not representative for AC–DC power conversion, in addition, the conversion efficiency is evaluated at all inspected 'DC to DC' operating points. Very high efficiencies of more than 97 % are measured in DC–DC operation. Therewith, the correctness of the steady-state converter model and the ZVS analysis presented in Chapter 3, the validity of the CDCB ZVS modulation schemes proposed in Chapter 4, and the successful implementation of the converter components and the control unit designed in Chapter 5, is proven.

An AC–DC system characterization is performed in order to evaluate the performance of the prototype converter with regard to the reached efficiency and with regard to the quality of the input power. The main conclusions are:

- The system is successfully tested within the full power range (up until an output power of 3.7 kW), showing waveforms with little distortion, and which are in very good agreement with the waveforms obtained from simulations;

- Although the trends match very well, a slight discrepancy (mostly less than 0.4%) can be noticed between the calculated and the measured efficiencies. This might require further refinement of the loss models employed in Chapter 5 (see below: 'Outlook and Future Work');
- The measured efficiencies are higher than 95 % within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96 % and the efficiency at nominal output power approximately 95.6 %;
- As predicted by the calculations, only a minor difference (around 0.25-0.3 % at maximum) can be noticed between the efficiency curves at different output voltages;
- A (true) power factor (PF) close to unity, and a low total harmonic distortion (THD) of the AC input current of around 4 %, are obtained within the major part of the output power range and within the whole output voltage range.

This makes that, regarding conversions efficiency, system power density, PF, and THD, the converter requirements specified in Table 1.1 of Section 1.3 are achieved. It should be reminded (see Chapter 5) that a considerable efficiency and power density enhancement can be obtained by using slightly modified heat sink designs and inductor/transformer designs. The low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [57] for Class A equipment, have not been measured. Nevertheless, in simulation the harmonics are well below the limits. Furthermore, electromagnetic compatibility (EMC) compliance with the CISPR 22 Class B standard [56] could not be experimentally verified due to the unavailability of the required measurement equipment.

The performance of the DAB AC–DC converter developed in this work is briefly compared (i.e. with regard to the conversion efficiency and power density) with the performance of two (similar) state-of-the-art dual-stage AC–DC converters reported in literature. Although the comparison is rather illustrative, the system developed is this work performs substantially better than the system presented in [20], which was taken a benchmark (see Section 1.3 of Chapter 1), while a performance close to the absolute state-of-the-art (AC–DC converter presented in [108]) is achieved. The main contribution presented in Chapter 6 is:

- A fully operational, successfully tested, high-efficiency and high-power-density converter prototype that is in compliance with the requirements specified in Section 1.3, being the first ever reported single-stage DAB AC–DC converter that is operated under full-operating-range ZVS.

7.3 Overall Conclusion

The overall conclusion of the presented work is that a single-stage (1-S) dual active bridge (DAB) AC–DC converter is suitable for the realization of single-phase, bidirectional, and isolated energy conversions, and for fulfilling the converter requirements specified Table 1.1 of Section 1.3, which relate to an on-board, 3.7 kW, EV battery charger. Thereby, absolutely essential are:

- A correct description of the DAB's zero voltage switching (ZVS) conditions, including the parasitic output capacitances of the semiconductor switches;
- A modulation scheme which relies on the previous ZVS conditions;
- A HF AC-link in which commutation inductance(s) are present.

On the condition that, in addition, the different converter components and the control unit are correctly designed and implemented, a performance that is similar to the performance of a state-of-the-art dual-stage system is feasible. Furthermore, the proposed methods are applicable for any application where a full bridge - full bridge (FBFB) DAB converter is used. This can be DC–DC converters, single-stage AC–DC converters, dual-stage AC–DC converters, single-stage AC–AC converters (solid state transformers [142]), etc. Note that with minor adjustments, the methods are also applicable for other DAB implementations such as for example the half bridge - full bridge (HBFB) DAB whereby, however, ZVS operation is much harder to obtain due to the reduced degree of freedom available to modulate the active bridges.

7.4 Outlook and Future Work

7.4.1 MOO and Objective System Comparison

This work shows that, with due observance of the proposed modeling approach, the single-stage DAB AC–DC converter topology can be considered as a valuable competitor for the traditional dual-stage AC–DC converter architectures. Although a performance that is close to the absolute state-of-the-art is reported, no statement can be made about which architecture/topology is the 'best'. This would require an objective and comprehensive comparative evaluation of the different systems, based on multi-objective optimizations (MOO) which provide a clear picture of the performance (i.e. by means of the Pareto Front) achievable through the individual concepts. By considering state-of-the-art technologies, the MOOs then enable the full exploitation of the inherent potential of the technology, and the state of the technology for the considered converter class with reference to the envelope of

the Pareto Fronts of the various circuit concepts can be determined. This work provides a framework that enables to perform such a system comparison, which could be the subject of further research.

7.4.2 Unfinished Converter Characterizations

The low-frequency mains current harmonics, which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [57] for Class A equipment, have not been measured. Furthermore, electromagnetic compatibility (EMC) compliance with the CISPR 22 Class B standard [56] could not be experimentally verified due to the unavailability of the required measurement equipment. These measurements could be performed in future.

7.4.3 Model Refinement

A slight discrepancy is noticed between the calculated and the measured efficiencies. It might be verified what exactly the origin is of this loss underestimation. From the loss modeling perspective, the following improvements might be considered:

- Improved models for the optimization of the heat sinks, such as the ones recently presented in [143], would enable a more accurate estimation of the junction temperatures, and consequently the losses, of the semiconductors;
- Regarding the semiconductor switching devices, accurate measurements of the switching losses under realistic operation conditions would allow to verify if the converter is effectively operated with quasi zero switching losses, and would (if necessary) allow to establish corresponding loss functions;
- A detailed thermal model for the magnetic elements (e.g. based on nodal thermal networks [116, 129]) would allow to include the temperature dependency of the losses in the magnetic elements. The same goes for the capacitors and the EMC input filter;
- The design of the EMC input filter may be performed with respect to the optimization of a certain Performance Index, e.g. maximum power density;
- The impact of component tolerances on the reliable converter operation and on the converter's efficiency could be investigated.

7.4.4 Further Remarks on the Practical Realization

Throughout the text, several hardware improvements have been suggested:

- Converter design: in Chapter 5 it is indicated how the efficiency and power density of the system can be enhanced by using further optimized heat sink designs and further optimized inductor/transformer designs. The required modifications do not imply a complete redesign of the mechanical assembly, enabling simple replacement;
- HF AC-link: the subject of further investigation/optimization might be to consider a T-type instead of a Pi-type equivalent circuit of the HF AC-link, which allows integration of the main inductor L_{ext} and the primary side commutation inductor L_{c1} by effectively using/tailoring the transformer's leakage inductances in order to obtain the same circuit behavior [102–104, 128];
- Controller: lookup table entries are dedicated results for one particular DAB converter. In practice, the system may be sensitive to changes of inductance values, and care should be taken when using high-performance MOSFET's. Loss of ZVS can easily cause device destruction. The DAB inductances, however, could be considered as another dimension of the lookup table;
- On-board measurements: an improved THD can be achieved by replacement of the on-board sample-based measurements circuits by Delta-Sigma measurements.

7.4.5 Dynamic DAB Model

As not considered in this work, investigation of the dynamic converter behavior such as in [144–146] forms a further possibility regarding future research.

A

Supplement to Chapter 3: Steady-State Operation of the DAB AC–DC Converter

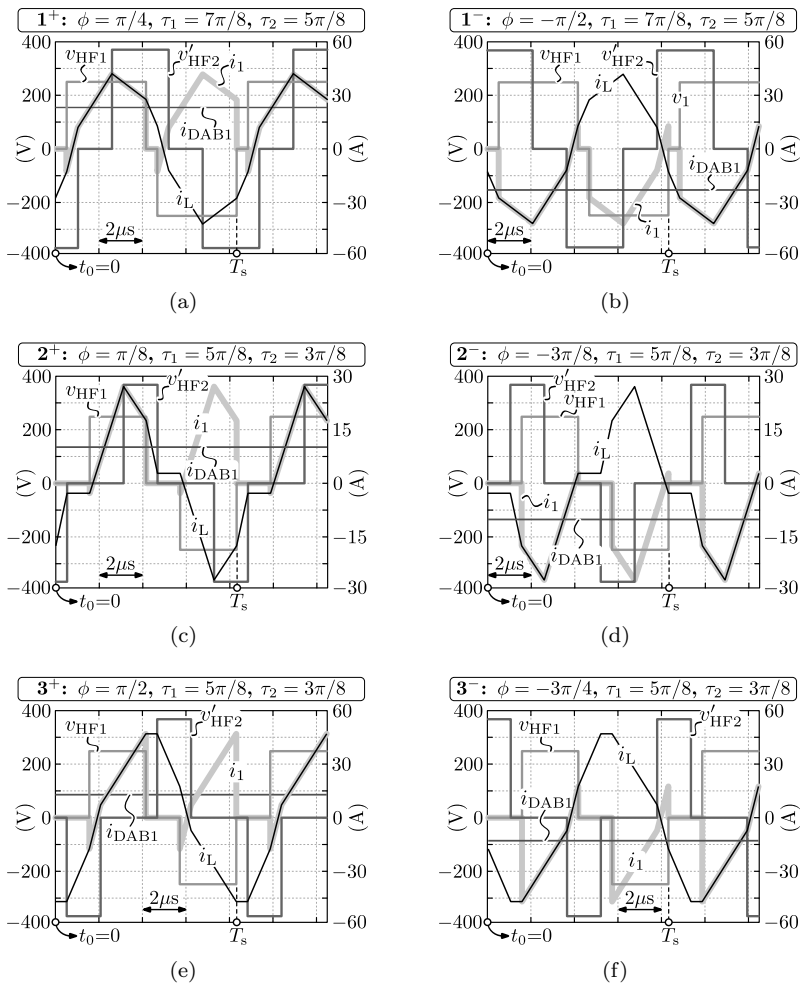
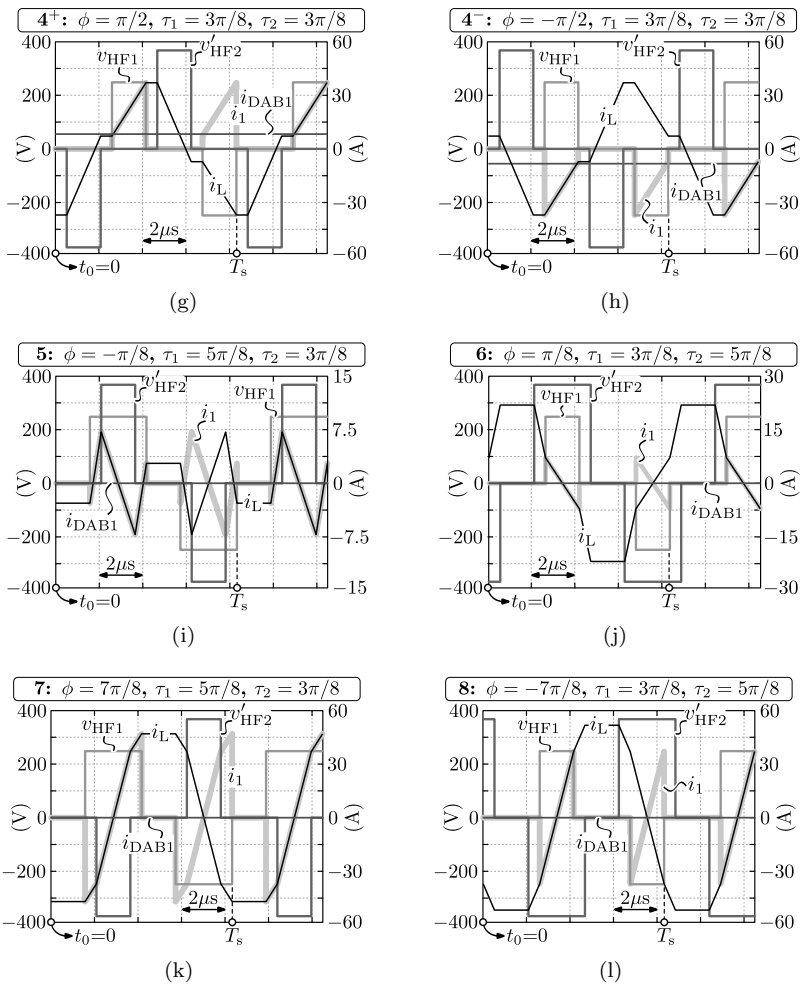


Figure A.1: Examples of the twelve switching modes that can be generated with the FBFB DAB shown in Fig. 3.7 (continued on the next page).



Cont. Figure A.1: Examples of the twelve switching modes that can be generated with the FBFB DAB shown in Fig. 3.7. The depicted waveforms are derived using: $v_{\mathrm{DC1}} = 250$ V, $V_{\mathrm{DC2}} = 370$ V, $n_1/n_2 = 1$, $L = 13$ μH, $L_{\mathrm{c1}} = L_{\mathrm{c2}} = \infty$, and $f_{\mathrm{s}} = 120$ kHz. Positive power flow only: modes $1^+ \ldots 4^+$; negative power only: modes $1^- \ldots 4^-$; positive and negative power flow: modes $5 \ldots 8$.

Modes for positive power flow only		Modes for negative power flow only	
Mode	*Condition*	*Mode*	*Condition*
1^+	$-\tau_1+\pi \leqslant \phi \leqslant \tau_2$	1^-	$-\tau_1 \leqslant \phi \leqslant \tau_2-\pi$
2^+	$0 \leqslant \phi \leqslant -\tau_1+\pi$ $\tau_2-\tau_1 \leqslant \phi \leqslant \tau_2$	2^-	$\tau_2-\pi \leqslant \phi \leqslant 0$ $-\tau_1 \leqslant \phi \leqslant \tau_2-\tau_1$
3^+	$\tau_2 \leqslant \phi \leqslant \pi$ $-\tau_1+\pi \leqslant \phi \leqslant \tau_2-\tau_1+\pi$	3^-	$-\pi \leqslant \phi \leqslant -\tau_1$ $\tau_2-\tau_1-\pi \leqslant \phi \leqslant \tau_2-\pi$
4^+	$\tau_2 \leqslant \phi \leqslant -\tau_1+\pi$	4^-	$\tau_2-\pi \leqslant \phi \leqslant -\tau_1$

Modes for both positive and negative power flow			
Mode	*Condition*	*Mode*	*Condition*
5	$\tau_2-\tau_1 \leqslant \phi \leqslant 0$	6	$0 \leqslant \phi \leqslant \tau_2-\tau_1$
7	$\tau_2-\tau_1+\pi \leqslant \phi \leqslant \pi$	8	$-\pi \leqslant \phi \leqslant \tau_2-\tau_1-\pi$

Table A.1: Mode boundary conditions for the FBFB DAB.

(a) Mode 1

	mode 1^+	mode 1^-
t_0	0	0
t_1	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_2	$\frac{\phi}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_3	$\frac{\pi + \phi - \tau_2}{\omega_s}$	$\frac{2\pi + \phi - \tau_2}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$

(b) Mode 2

	mode 2^+	mode 2^-
t_0	0	0
t_1	$\frac{\phi}{\omega_s}$	$\frac{\pi + \phi - \tau_2}{\omega_s}$
t_2	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_3	$\frac{\pi + \phi - \tau_2}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$

(c) Mode 3

	mode 3^+	mode 3^-
t_0	0	0
t_1	$\frac{\phi - \tau_2}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_2	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_3	$\frac{\phi}{\omega_s}$	$\frac{2\pi + \phi - \tau_2}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$

(d) Mode 4

	mode 4^+	mode 4^-
t_0	0	0
t_1	$\frac{\phi - \tau_2}{\omega_s}$	$\frac{\pi + \phi - \tau_2}{\omega_s}$
t_2	$\frac{\phi}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_3	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$

(e) Modes 5, 6, 7, 8

	mode 5	mode 6	mode 7	mode 8
t_0	0	0	0	0
t_1	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\phi}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\pi + \phi}{\omega_s}$
t_2	$\frac{\pi + \phi - \tau_2}{\omega_s}$	$\frac{\pi + \phi - \tau_2}{\omega_s}$	$\frac{\phi - \tau_2}{\omega_s}$	$\frac{2\pi + \phi - \tau_2}{\omega_s}$
t_3	$\frac{\pi + \phi}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$	$\frac{\phi}{\omega_s}$	$\frac{\pi - \tau_1}{\omega_s}$
t_4	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$	$\frac{\pi}{\omega_s} = \frac{T_s}{2}$

Table A.2: Switching instances $t_0 \dots t_4$ for all possible switching modes of the FBFB DAB, choosing the negative rising edge of $v_{\mathrm{HF1}}(t)$ as the time reference t_0 ($= 0$ s).

Systems of equations required for the calculation of $i_\mathrm{L}(t_\mathrm{i})$ regarding all possible switching modes of the FBFB DAB converter:

Mode 1^+:

$$\begin{aligned}
i_\mathrm{L}(t_1) &= i_\mathrm{L}(t_0) + \frac{(\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(\pi-\tau_1)}{\omega_\mathrm{s}} && \text{: interval I,}\\
i_\mathrm{L}(t_2) &= i_\mathrm{L}(t_1) + \frac{(v_\mathrm{DC1}+\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(-\pi+\phi+\tau_1)}{\omega_\mathrm{s}} && \text{: interval II,}\\
i_\mathrm{L}(t_3) &= i_\mathrm{L}(t_2) + \frac{v_\mathrm{DC1}}{L}\cdot\frac{(\pi-\tau_2)}{\omega_\mathrm{s}} && \text{: interval III,}\\
i_\mathrm{L}(t_4) &= i_\mathrm{L}(t_3) + \frac{(v_\mathrm{DC1}-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(-\phi+\tau_2)}{\omega_\mathrm{s}} && \text{: interval IV,}\\
i_\mathrm{L}(t_4) &= -i_\mathrm{L}(t_0).
\end{aligned} \tag{A.1}$$

Mode 1^-:

$$\begin{aligned}
i_\mathrm{L}(t_1) &= i_\mathrm{L}(t_0) + \frac{(-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(\pi-\tau_1)}{\omega_\mathrm{s}} && \text{: interval I,}\\
i_\mathrm{L}(t_2) &= i_\mathrm{L}(t_1) + \frac{(v_\mathrm{DC1}-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(\phi+\tau_1)}{\omega_\mathrm{s}} && \text{: interval II,}\\
i_\mathrm{L}(t_3) &= i_\mathrm{L}(t_2) + \frac{v_\mathrm{DC1}}{L}\cdot\frac{(\pi-\tau_2)}{\omega_\mathrm{s}} && \text{: interval III,}\\
i_\mathrm{L}(t_4) &= i_\mathrm{L}(t_3) + \frac{(v_\mathrm{DC1}+\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(-\pi-\phi+\tau_2)}{\omega_\mathrm{s}} && \text{: interval IV,}\\
i_\mathrm{L}(t_4) &= -i_\mathrm{L}(t_0).
\end{aligned} \tag{A.2}$$

Mode 2^+:

$$\begin{aligned}
i_\mathrm{L}(t_1) &= i_\mathrm{L}(t_0) + \frac{(\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{\phi}{\omega_\mathrm{s}} && \text{: interval I,}\\
i_\mathrm{L}(t_2) &= i_\mathrm{L}(t_1) && \text{: interval II,}\\
i_\mathrm{L}(t_3) &= i_\mathrm{L}(t_2) + \frac{v_\mathrm{DC1}}{L}\cdot\frac{(\phi+\tau_1-\tau_2)}{\omega_\mathrm{s}} && \text{: interval III,}\\
i_\mathrm{L}(t_4) &= i_\mathrm{L}(t_3) + \frac{(v_\mathrm{DC1}-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(-\phi+\tau_2)}{\omega_\mathrm{s}} && \text{: interval IV,}\\
i_\mathrm{L}(t_4) &= -i_\mathrm{L}(t_0).
\end{aligned} \tag{A.3}$$

Mode 2^-:

$$\begin{aligned}
i_\mathrm{L}(t_1) &= i_\mathrm{L}(t_0) && \text{: interval I,}\\
i_\mathrm{L}(t_2) &= i_\mathrm{L}(t_1) + \frac{(-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(-\phi-\tau_1+\tau_2)}{\omega_\mathrm{s}} && \text{: interval II,}\\
i_\mathrm{L}(t_3) &= i_\mathrm{L}(t_2) + \frac{(v_\mathrm{DC1}-\frac{n_1}{n_2}\cdot V_\mathrm{DC2})}{L}\cdot\frac{(\phi+\tau_1)}{\omega_\mathrm{s}} && \text{: interval III,}\\
i_\mathrm{L}(t_4) &= i_\mathrm{L}(t_3) + \frac{v_\mathrm{DC1}}{L}\cdot\frac{-\phi}{\omega_\mathrm{s}} && \text{: interval IV,}\\
i_\mathrm{L}(t_4) &= -i_\mathrm{L}(t_0).
\end{aligned} \tag{A.4}$$

Mode 3$^+$:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) + \frac{(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(\pi-\phi-\tau_1+\tau_2)}{\omega_{\mathrm{s}}} && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{(v_{\mathrm{DC1}}+\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(-\pi+\phi+\tau_1)}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(\pi-\phi)}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.5}$$

Mode 3$^-$:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) + \frac{(-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(\pi+\phi)}{\omega_{\mathrm{s}}} && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(\pi+\phi+\tau_1-\tau_2)}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{(v_{\mathrm{DC1}}+\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(-\pi-\phi+\tau_2)}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.6}$$

Mode 4$^+$:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) + \frac{(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{\tau_2}{\omega_{\mathrm{s}}} && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{\tau_1}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.7}$$

Mode 4$^-$:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) + \frac{(-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{\tau_2}{\omega_{\mathrm{s}}} && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{\tau_1}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.8}$$

Mode 5:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) + \frac{v_{\mathrm{DC1}}}{L} \cdot \frac{(\phi + \tau_1 - \tau_2)}{\omega_{\mathrm{s}}} && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{(v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\tau_2}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{v_{\mathrm{DC1}}}{L} \cdot \frac{-\phi}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.9}$$

Mode 6:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) + \frac{(\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\phi}{\omega_{\mathrm{s}}} && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{(-\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(-\phi - \tau_1 + \tau_2)}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{(v_{\mathrm{DC1}} - \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\tau_1}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.10}$$

Mode 7:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) + \frac{v_{\mathrm{DC1}}}{L} \cdot \frac{(-\pi + \phi + \tau_1 - \tau_2)}{\omega_{\mathrm{s}}} && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{(v_{\mathrm{DC1}} + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\tau_2}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{v_{\mathrm{DC1}}}{L} \cdot \frac{(\pi - \phi)}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.11}$$

Mode 8:

$$\begin{aligned}
&i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) + \frac{(-\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(\pi + \phi)}{\omega_{\mathrm{s}}} && : \text{interval I},\\
&i_{\mathrm{L}}(t_2) = i_{\mathrm{L}}(t_1) && : \text{interval II},\\
&i_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{(\frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{(-\pi - \phi - \tau_1 + \tau_2)}{\omega_{\mathrm{s}}} && : \text{interval III},\\
&i_{\mathrm{L}}(t_4) = i_{\mathrm{L}}(t_3) + \frac{(v_{\mathrm{DC1}} + \frac{n_1}{n_2} \cdot V_{\mathrm{DC2}})}{L} \cdot \frac{\tau_1}{\omega_{\mathrm{s}}} && : \text{interval IV},\\
&i_{\mathrm{L}}(t_4) = -i_{\mathrm{L}}(t_0).
\end{aligned} \tag{A.12}$$

(a) $i_\mathrm{L}(t_\mathrm{i})$ for mode 1^+

$i_\mathrm{L}(t_0)$	$-\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\pi - 2\frac{n_1}{n_2}V_\mathrm{DC2}\tau_1 - 2\frac{n_1}{n_2}V_\mathrm{DC2}\phi + \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 - v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{2v_\mathrm{DC1}\pi - v_\mathrm{DC1}\tau_1 - 2v_\mathrm{DC1}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{-2v_\mathrm{DC1}\tau_2 + v_\mathrm{DC1}\tau_1 + 2v_\mathrm{DC1}\phi + \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$

(b) $i_\mathrm{L}(t_\mathrm{i})$ for mode 1^-

$i_\mathrm{L}(t_0)$	$\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\pi + 2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 - v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\tau_1 + 2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 - v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$\dfrac{2v_\mathrm{DC1}\phi + v_\mathrm{DC1}\tau_1 - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{2v_\mathrm{DC1}\pi - 2v_\mathrm{DC1}\tau_2 + 2v_\mathrm{DC1}\phi + v_\mathrm{DC1}\tau_1 - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$-\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\pi + 2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 - v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$

(c) $i_\mathrm{L}(t_\mathrm{i})$ for mode 2^+

$i_\mathrm{L}(t_0)$	$-\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{-\frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{-\frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{2v_\mathrm{DC1}\phi - 2v_\mathrm{DC1}\tau_2 + v_\mathrm{DC1}\tau_1 + \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{2\frac{n_1}{n_2}V_\mathrm{DC2}\phi - \frac{n_1}{n_2}V_\mathrm{DC2}\tau_2 + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s}L}$

Table A.3: Expressions for the inductor current $i_\mathrm{L}(t)$ at the different switching instances $t_0 \dots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(d) $i_\mathrm{L}(t_\mathrm{i})$ for mode 2^-

$i_\mathrm{L}(t_0)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$\dfrac{2\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_1 + 2\frac{n_1}{n_2}V_{\mathrm{DC2}}\phi - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 - v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{2v_{\mathrm{DC1}}\phi + v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$

(e) $i_\mathrm{L}(t_\mathrm{i})$ for mode 3^+

$i_\mathrm{L}(t_0)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$\dfrac{2\frac{n_1}{n_2}V_{\mathrm{DC2}}\pi - 2\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_1 - 2\frac{n_1}{n_2}V_{\mathrm{DC2}}\phi + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 - v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$-\dfrac{2v_{\mathrm{DC1}}\pi - v_{\mathrm{DC1}}\tau_1 - 2v_{\mathrm{DC1}}\phi - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$

(f) $i_\mathrm{L}(t_\mathrm{i})$ for mode 3^-

$i_\mathrm{L}(t_0)$	$\dfrac{2\frac{n_1}{n_2}V_{\mathrm{DC2}}\pi - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + 2\frac{n_1}{n_2}V_{\mathrm{DC2}}\phi - v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{2v_{\mathrm{DC1}}\pi - 2v_{\mathrm{DC1}}\tau_2 + 2v_{\mathrm{DC1}}\phi + v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$-\dfrac{2\frac{n_1}{n_2}V_{\mathrm{DC2}}\pi - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + 2\frac{n_1}{n_2}V_{\mathrm{DC2}}\phi - v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$

Cont. Table A.3: Expressions for the inductor current $i_\mathrm{L}(t)$ at the different switching instances $t_0 \dots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(g) $i_\mathrm{L}(t_\mathrm{i})$ for mode 4^+

$i_\mathrm{L}(t_0)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{-\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$-\dfrac{-\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{v_{\mathrm{DC1}}\tau_1 + \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$

(h) $i_\mathrm{L}(t_\mathrm{i})$ for mode 4^-

$i_\mathrm{L}(t_0)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$-\dfrac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2 + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{v_{\mathrm{DC1}}\tau_1 - \frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L}$

(i) $i_\mathrm{L}(t_\mathrm{i})$ for mode 5

$i_\mathrm{L}(t_0)$	$-\dfrac{-\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}} + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{-\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}} + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_2)$	$\dfrac{2v_{\mathrm{DC1}}\phi - 2v_{\mathrm{DC1}}\tau_2 + v_{\mathrm{DC1}}\tau_1 + \tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_3)$	$\dfrac{-\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}} + 2v_{\mathrm{DC1}}\phi + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{-\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}} + v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L}$

Cont. Table A.3: Expressions for the inductor current $i_\mathrm{L}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(j) $i_\mathrm{L}(t_\mathrm{i})$ for mode 6

$i_\mathrm{L}(t_0)$	$-\dfrac{\tau_1 v_\mathrm{DC1} + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{\tau_1 v_\mathrm{DC1} - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{\tau_1 v_\mathrm{DC1} - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_3)$	$\dfrac{2\frac{n_1}{n_2} V_\mathrm{DC2}\tau_1 + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2 - \tau_1 v_\mathrm{DC1}}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{\tau_1 v_\mathrm{DC1} + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$

(k) $i_\mathrm{L}(t_\mathrm{i})$ for mode 7

$i_\mathrm{L}(t_0)$	$-\dfrac{\tau_2 \frac{n_1}{n_2} V_\mathrm{DC2} + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{\tau_2 \frac{n_1}{n_2} V_\mathrm{DC2} + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{2v_\mathrm{DC1}\pi - v_\mathrm{DC1}\tau_1 - 2v_\mathrm{DC1}\phi + 2v_\mathrm{DC1}\tau_2 + \tau_2 \frac{n_1}{n_2} V_\mathrm{DC2}}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_3)$	$-\dfrac{-\tau_2 \frac{n_1}{n_2} V_\mathrm{DC2} + 2v_\mathrm{DC1}\pi - v_\mathrm{DC1}\tau_1 - 2v_\mathrm{DC1}\phi}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$\dfrac{\tau_2 \frac{n_1}{n_2} V_\mathrm{DC2} + v_\mathrm{DC1}\tau_1}{2\omega_\mathrm{s} L}$

(l) $i_\mathrm{L}(t_\mathrm{i})$ for mode 8

$i_\mathrm{L}(t_0)$	$\dfrac{-\tau_1 v_\mathrm{DC1} + 2\frac{n_1}{n_2} V_\mathrm{DC2}\pi + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_1)$	$-\dfrac{\tau_1 v_\mathrm{DC1} + \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_2)$	$-\dfrac{\tau_1 v_\mathrm{DC1} + \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_3)$	$-\dfrac{2\frac{n_1}{n_2} V_\mathrm{DC2}\pi + 2\frac{n_1}{n_2} V_\mathrm{DC2}\tau_1 + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2 + \tau_1 v_\mathrm{DC1}}{2\omega_\mathrm{s} L}$
$i_\mathrm{L}(t_4) = -i_\mathrm{L}(t_0)$	$-\dfrac{-\tau_1 v_\mathrm{DC1} + 2\frac{n_1}{n_2} V_\mathrm{DC2}\pi + 2\frac{n_1}{n_2} V_\mathrm{DC2}\phi - \frac{n_1}{n_2} V_\mathrm{DC2}\tau_2}{2\omega_\mathrm{s} L}$

Cont. Table A.3: Expressions for the inductor current $i_\mathrm{L}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter.

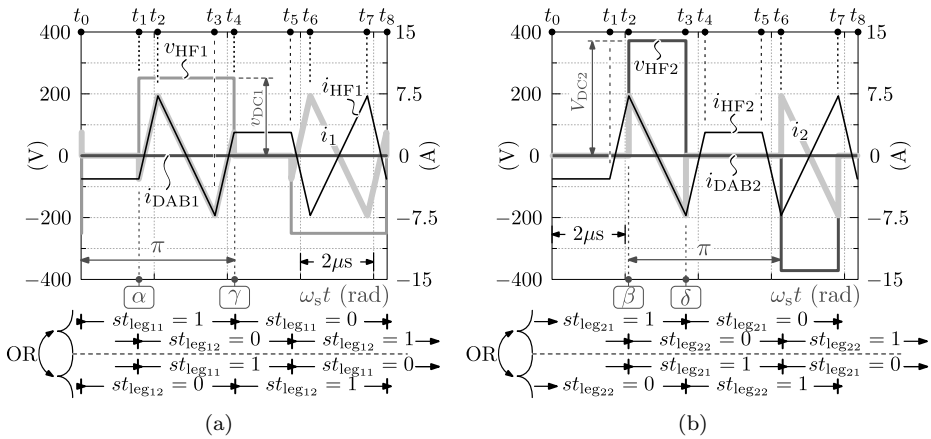


Figure A.2: (a) Primary side and (b) secondary side bridge quantities (voltages and currents) that correspond with the example in Figure 3.9(b) (i.e. mode 5).

Predefined terms		
$K = \frac{\frac{n_1}{n_2}V_{DC2}}{2\omega_s L\pi}$	$e_2 = (\phi - \tau_2)^2 - e_1$	$e_5 = \pi(\pi - 2(\tau_1 + \phi))$
	$e_3 = (\phi + \tau_1)^2 - e_1$	$e_6 = \tau_2^2 - e_1 - 2\tau_2\phi$
$e_1 = \tau_1\tau_2$	$e_4 = \pi(\pi - 2(\tau_2 - \phi))$	$e_7 = \tau_1^2 - e_1 + 2\tau_1\phi$

Modes for positive power flow only	Modes for negative power flow only
$i_{DAB1,1^+} = -K(e_1 + e_2 + e_3 + e_5)$	$i_{DAB1,1^-} = K(e_1 + e_2 + e_3 + e_4)$
$i_{DAB1,2^+} = -Ke_2$	$i_{DAB1,2^-} = Ke_3$
$i_{DAB1,3^+} = -K(e_3 + e_5)$	$i_{DAB1,3^-} = K(e_2 + e_4)$
$i_{DAB1,4^+} = Ke_1$	$i_{DAB1,4^-} = -Ke_1$

Modes for both positive and negative power flow	
$i_{DAB1,5} = -Ke_6$	$i_{DAB1,6} = Ke_7$
$i_{DAB1,7} = K(e_6 + 2\tau_2\pi)$	$i_{DAB1,8} = -K(e_7 + 2\tau_1\pi)$

Table A.4: Expressions for the averaged DAB input current i_{DAB1} regarding all possible switching modes of the FBFB DAB converter.

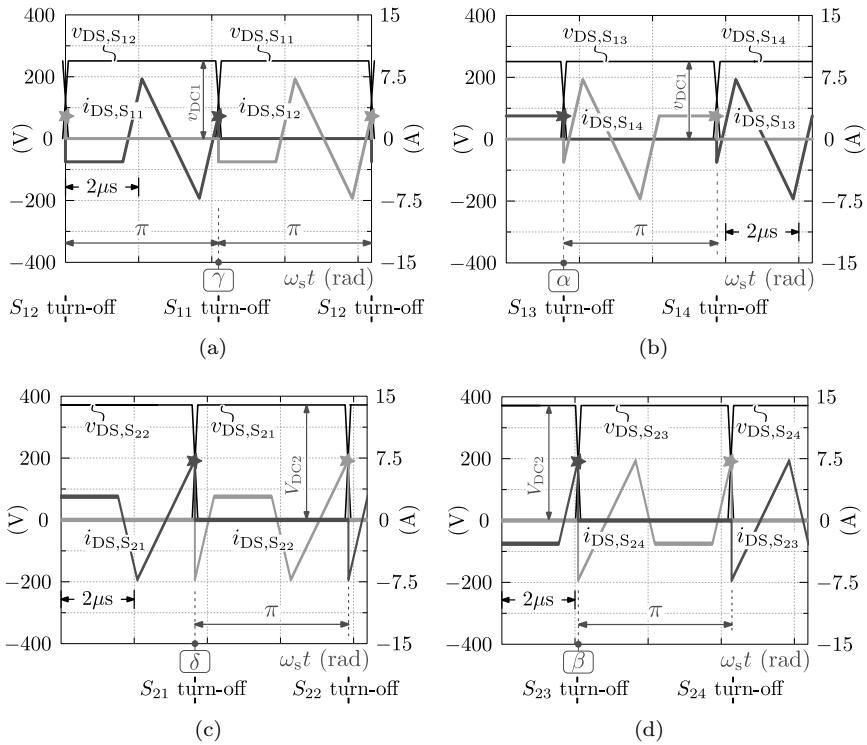


Figure A.3: Drain to source currents $i_{\mathrm{DS,S_{xx}}}$ and corresponding drain to source voltages $v_{\mathrm{DS,S_{xx}}}$ of all the switches S_{xx} of the FBFB DAB regarding mode 5 operation according to the example in Figure 3.9(b), and calculated based on the primary side and secondary side bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ in Figure A.2. (a)-(b) Switches $S_{1\mathrm{x}}$ of the primary side active bridge: (a) bridge leg_{11}, (b) bridge leg_{12}. (c)-(d) Switches $S_{2\mathrm{x}}$ of the secondary side active bridge: (c) bridge leg_{21}, (d) bridge leg_{22}.

(a) Mode 1

	mode 1^+		mode 1^-	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$
β	$t_\beta = t_3$	$i_{\mathrm{HF}2}(t_3)$	$t_\beta = t_7$	$i_{\mathrm{HF}2}(t_7) = -i_{\mathrm{HF}2}(t_3)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_6$	$i_{\mathrm{HF}2}(t_6) = -i_{\mathrm{HF}2}(t_2)$	$t_\delta = t_2$	$i_{\mathrm{HF}2}(t_2)$

(b) Mode 2

	mode 2^+		mode 2^-	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_2$	$i_{\mathrm{HF}1}(t_2)$	$t_\alpha = t_2$	$i_{\mathrm{HF}1}(t_2)$
β	$t_\beta = t_3$	$i_{\mathrm{HF}2}(t_3)$	$t_\beta = t_1$	$i_{\mathrm{HF}2}(t_1)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_5$	$i_{\mathrm{HF}2}(t_5) = -i_{\mathrm{HF}2}(t_1)$	$t_\delta = t_3$	$i_{\mathrm{HF}2}(t_3)$

(c) Mode 3

	mode 3^+		mode 3^-	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_2$	$i_{\mathrm{HF}1}(t_2)$	$t_\alpha = t_2$	$i_{\mathrm{HF}1}(t_2)$
β	$t_\beta = t_5$	$i_{\mathrm{HF}2}(t_5) = -i_{\mathrm{HF}2}(t_1)$	$t_\beta = t_7$	$i_{\mathrm{HF}2}(t_7) = -i_{\mathrm{HF}2}(t_3)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_7$	$i_{\mathrm{HF}2}(t_7) = -i_{\mathrm{HF}2}(t_3)$	$t_\delta = t_1$	$i_{\mathrm{HF}2}(t_1)$

(d) Mode 4

	mode 4^+		mode 4^-	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_3$	$i_{\mathrm{HF}1}(t_3)$	$t_\alpha = t_3$	$i_{\mathrm{HF}1}(t_3)$
β	$t_\beta = t_5$	$i_{\mathrm{HF}2}(t_5) = -i_{\mathrm{HF}2}(t_1)$	$t_\beta = t_1$	$i_{\mathrm{HF}2}(t_1)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_6$	$i_{\mathrm{HF}2}(t_6) = -i_{\mathrm{HF}2}(t_2)$	$t_\delta = t_2$	$i_{\mathrm{HF}2}(t_2)$

(e) Mode 5, 6

	mode 5		mode 6	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$	$t_\alpha = t_3$	$i_{\mathrm{HF}1}(t_3)$
β	$t_\beta = t_2$	$i_{\mathrm{HF}2}(t_2)$	$t_\beta = t_2$	$i_{\mathrm{HF}2}(t_2)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_3$	$i_{\mathrm{HF}2}(t_3)$	$t_\delta = t_5$	$i_{\mathrm{HF}2}(t_5) = -i_{\mathrm{HF}2}(t_1)$

(f) Mode 7, 8

	mode 7		mode 8	
θ_i	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$	t_{θ_i}	$i_\mathrm{HF}(t_{\theta_\mathrm{i}})$
α	$t_\alpha = t_1$	$i_{\mathrm{HF}1}(t_1)$	$t_\alpha = t_3$	$i_{\mathrm{HF}1}(t_3)$
β	$t_\beta = t_6$	$i_{\mathrm{HF}2}(t_6) = -i_{\mathrm{HF}2}(t_2)$	$t_\beta = t_6$	$i_{\mathrm{HF}2}(t_6) = -i_{\mathrm{HF}2}(t_2)$
γ	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$	$t_\gamma = t_4$	$i_{\mathrm{HF}1}(t_4)$
δ	$t_\delta = t_7$	$i_{\mathrm{HF}2}(t_7) = -i_{\mathrm{HF}2}(t_3)$	$t_\delta = t_1$	$i_{\mathrm{HF}2}(t_1)$

Table A.5: Switching instances $t_{\theta_\mathrm{i}} = \{t_\alpha, t_\beta, t_\gamma, t_\delta\}$ and bridge currents $i_{\mathrm{HF}1}(t_{\theta_\mathrm{i}})$ and $i_{\mathrm{HF}2}(t_{\theta_\mathrm{i}})$ required to evaluate (3.44) for all possible switching modes of the FBFB DAB converter.

Systems of equations required for the calculation of $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ regarding switching modes 1^+ and 5 of the FBFB DAB converter:

Mode 1^+, $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$:

$$\begin{aligned}
&i_{\mathrm{L_{c1}}}(t_1) = i_{\mathrm{L_{c1}}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L_{c1}}}(t_2) = i_{\mathrm{L_{c1}}}(t_1) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(-\pi+\phi+\tau_1)}{\omega_\mathrm{s}} && : \text{interval II},\\
&i_{\mathrm{L_{c1}}}(t_3) = i_{\mathrm{L_{c1}}}(t_2) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(\pi-\tau_2)}{\omega_\mathrm{s}} && : \text{interval III},\\
&i_{\mathrm{L_{c1}}}(t_4) = i_{\mathrm{L_{c1}}}(t_3) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(-\phi+\tau_2)}{\omega_\mathrm{s}} && : \text{interval IV},\\
&i_{\mathrm{L_{c1}}}(t_4) = -i_{\mathrm{L_{c1}}}(t_0).
\end{aligned} \tag{A.13}$$

Mode 5, $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$:

$$\begin{aligned}
&i_{\mathrm{L_{c1}}}(t_1) = i_{\mathrm{L_{c1}}}(t_0) && : \text{interval I},\\
&i_{\mathrm{L_{c1}}}(t_2) = i_{\mathrm{L_{c1}}}(t_1) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{(\phi+\tau_1-\tau_2)}{\omega_\mathrm{s}} && : \text{interval II},\\
&i_{\mathrm{L_{c1}}}(t_3) = i_{\mathrm{L_{c1}}}(t_2) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{\tau_2}{\omega_\mathrm{s}} && : \text{interval III},\\
&i_{\mathrm{L_{c1}}}(t_4) = i_{\mathrm{L_{c1}}}(t_3) + \frac{v_{\mathrm{DC1}}}{L}\cdot\frac{-\phi}{\omega_\mathrm{s}} && : \text{interval IV},\\
&i_{\mathrm{L_{c1}}}(t_4) = -i_{\mathrm{L_{c1}}}(t_0).
\end{aligned} \tag{A.14}$$

Mode 1^+, $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$:

$$\begin{aligned}
&i'_{\mathrm{L_{c2}}}(t_1) = i'_{\mathrm{L_{c2}}}(t_0) + \frac{(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(\pi-\tau_1)}{\omega_\mathrm{s}} && : \text{interval I},\\
&i'_{\mathrm{L_{c2}}}(t_2) = i'_{\mathrm{L_{c2}}}(t_1) + \frac{(\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(-\pi+\phi+\tau_1)}{\omega_\mathrm{s}} && : \text{interval II},\\
&i'_{\mathrm{L_{c2}}}(t_3) = i'_{\mathrm{L_{c2}}}(t_2) && : \text{interval III},\\
&i'_{\mathrm{L_{c2}}}(t_4) = i'_{\mathrm{L_{c2}}}(t_3) + \frac{(-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{(-\phi+\tau_2)}{\omega_\mathrm{s}} && : \text{interval IV},\\
&i'_{\mathrm{L_{c2}}}(t_4) = -i'_{\mathrm{L_{c2}}}(t_0).
\end{aligned} \tag{A.15}$$

Mode 5, $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$:

$$\begin{aligned}
&i'_{\mathrm{L_{c2}}}(t_1) = i'_{\mathrm{L_{c2}}}(t_0) && : \text{interval I},\\
&i'_{\mathrm{L_{c2}}}(t_2) = i'_{\mathrm{L_{c2}}}(t_1) && : \text{interval II},\\
&i'_{\mathrm{L_{c2}}}(t_3) = i'_{\mathrm{L_{c2}}}(t_2) + \frac{(-\frac{n_1}{n_2}\cdot V_{\mathrm{DC2}})}{L}\cdot\frac{\tau_2}{\omega_\mathrm{s}} && : \text{interval III},\\
&i'_{\mathrm{L_{c2}}}(t_4) = i'_{\mathrm{L_{c2}}}(t_3) && : \text{interval IV},\\
&i'_{\mathrm{L_{c2}}}(t_4) = -i'_{\mathrm{L_{c2}}}(t_0).
\end{aligned} \tag{A.16}$$

(a) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 1^+

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\pi-2\tau_1-2\phi+\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\,(2\pi-\tau_1-2\phi)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\,(-2\tau_2+\tau_1+2\phi)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(b) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 1^-

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\pi+2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\tau_1+2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$\frac{v_{\mathrm{DC1}}\,(2\phi+\tau_1)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\,(2\pi-2\tau_2+2\phi+\tau_1)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\pi+2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(c) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 2^+

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\,(2\phi-2\tau_2+\tau_1)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\,(2\phi-\tau_2)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

Table A.6: Expressions for the commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(d) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 2^-

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\left(2\tau_1+2\phi-\tau_2\right)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\left(2\phi+\tau_1\right)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(e) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 3^+

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\left(2\pi-2\tau_1-2\phi+\tau_2\right)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$-\frac{v_{\mathrm{DC1}}\left(2\pi-\tau_1-2\phi\right)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(f) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 3^-

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\left(2\pi-\tau_2+2\phi\right)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\left(2\pi-2\tau_2+2\phi+\tau_1\right)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\left(2\pi-\tau_2+2\phi\right)}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

Cont. Table A.6: Expressions for the commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(g) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 4^+

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(h) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 4^-

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2}V_{\mathrm{DC2}}\tau_2}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

(i) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 5

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_2	$\frac{v_{\mathrm{DC1}}\left(2\phi-2\tau_2+\tau_1\right)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$-\frac{\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_3	$\frac{v_{\mathrm{DC1}}\left(2\phi+\tau_1\right)}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}}\tau_1}{2\omega_\mathrm{s}L_{\mathrm{c1}}}$	$\frac{\tau_2\frac{n_1}{n_2}V_{\mathrm{DC2}}}{2\omega_\mathrm{s}L'_{\mathrm{c2}}}$

Cont. Table A.6: Expressions for the commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter (continued on the next page).

(j) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 6

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_1	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} \tau_2}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_2	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} \tau_2}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_3	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\tau_1 + 2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_4	$\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$

(k) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 7

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{v_{\mathrm{DC1}} \tau_1}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\tau_2 \frac{n_1}{n_2} V_{\mathrm{DC2}}}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_1	$-\frac{v_{\mathrm{DC1}} \tau_1}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\tau_2 \frac{n_1}{n_2} V_{\mathrm{DC2}}}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_2	$-\frac{v_{\mathrm{DC1}} (2\pi - \tau_1 - 2\phi + 2\tau_2)}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\tau_2 \frac{n_1}{n_2} V_{\mathrm{DC2}}}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_3	$-\frac{v_{\mathrm{DC1}} (2\pi - \tau_1 - 2\phi)}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\tau_2 \frac{n_1}{n_2} V_{\mathrm{DC2}}}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_4	$\frac{v_{\mathrm{DC1}} \tau_1}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\tau_2 \frac{n_1}{n_2} V_{\mathrm{DC2}}}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$

(l) $i_{\mathrm{L_{c1}}}(t_\mathrm{i})$ and $i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$ for mode 8

	$i_{\mathrm{L_{c1}}}(t_\mathrm{i})$	$i'_{\mathrm{L_{c2}}}(t_\mathrm{i})$
t_0	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$-\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\pi + 2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_1	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} \tau_2}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_2	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} \tau_2}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_3	$-\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\pi + 2\tau_1 + 2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$
t_4	$\frac{\tau_1 v_{\mathrm{DC1}}}{2\omega_\mathrm{s} L_{\mathrm{c1}}}$	$\frac{\frac{n_1}{n_2} V_{\mathrm{DC2}} (2\pi + 2\phi - \tau_2)}{2\omega_\mathrm{s} L'_{\mathrm{c2}}}$

Cont. Table A.6: Expressions for the commutation currents $i_{\mathrm{L_{c1}}}(t)$ and $i'_{\mathrm{L_{c2}}}(t)$ at the different switching instances $t_0 \ldots t_4$ within $0 < t \leqslant T_\mathrm{s}/2$ for all possible switching modes of the FBFB DAB converter.

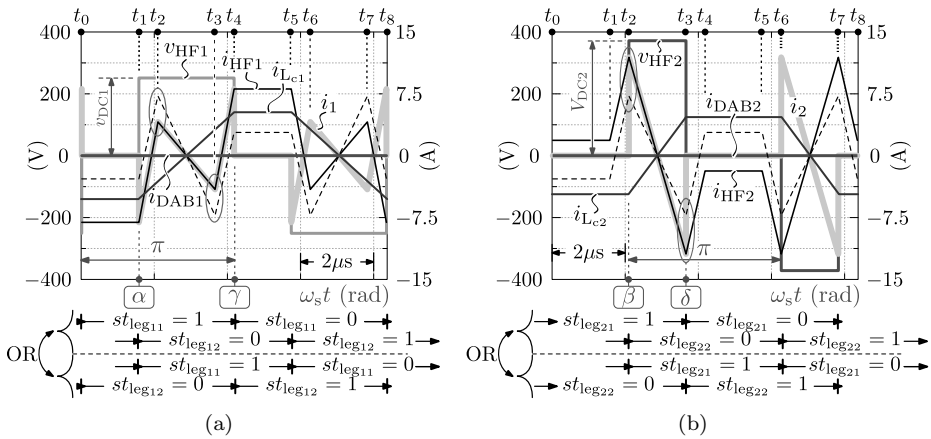


Figure A.4: Repetition of Figure A.2 (mode 5) with the difference that now commutation inductances L_{c1} and L_{c2} are added in the HF AC-link, i.e. $L_{c1} = L_{c2} = 62.1$ μH in this figure compared to $L_{c1} = L_{c2} = \infty$ for Figure A.2. (a) Primary side and (b) secondary side bridge quantities (voltages and currents).

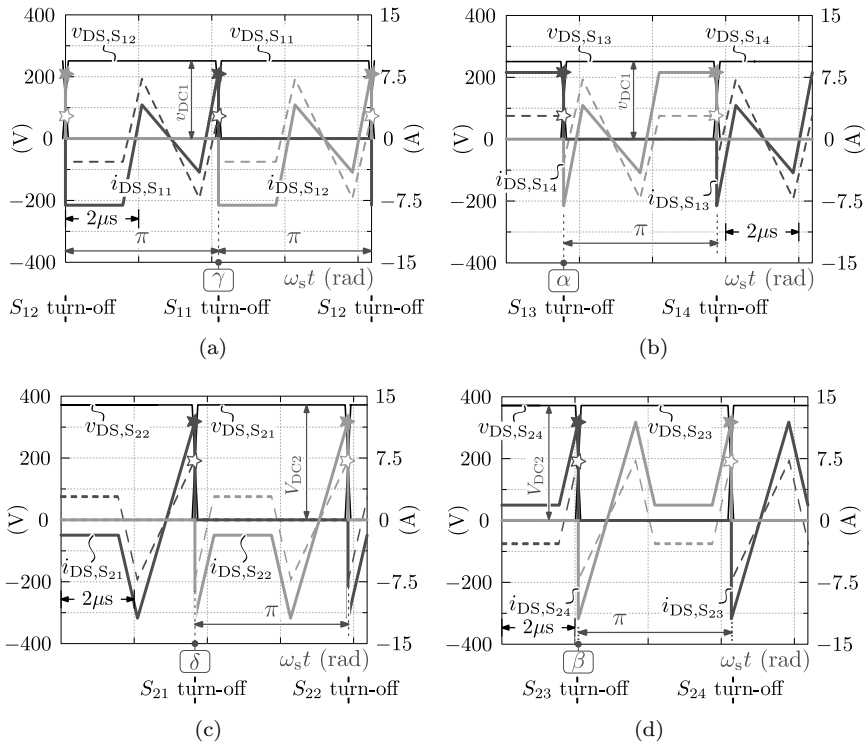


Figure A.5: Repetition of Figure A.3 (mode 5) with the difference that now commutation inductances L_{c1} and L_{c2} are added in the HF AC-link, i.e. $L_{c1} = L_{c2} = 62.1\ \mu$H in this figure compared to $L_{c1} = L_{c2} = \infty$ for Figure A.3. (a)-(b) Drain to source currents $i_{DS,S_{1x}}$ in switches S_{1x} of the primary side active bridge: (a) bridge leg$_{11}$, (b) bridge leg$_{12}$. (c)-(d) Drain to source currents $i_{DS,S_{2x}}$ in switches S_{2x} of the secondary side active bridge: (c) bridge leg$_{21}$, (d) bridge leg$_{22}$.

B

Supplement to Chapter 4: ZVS Modulation Schemes

B.1 Results of the Numerical Approach

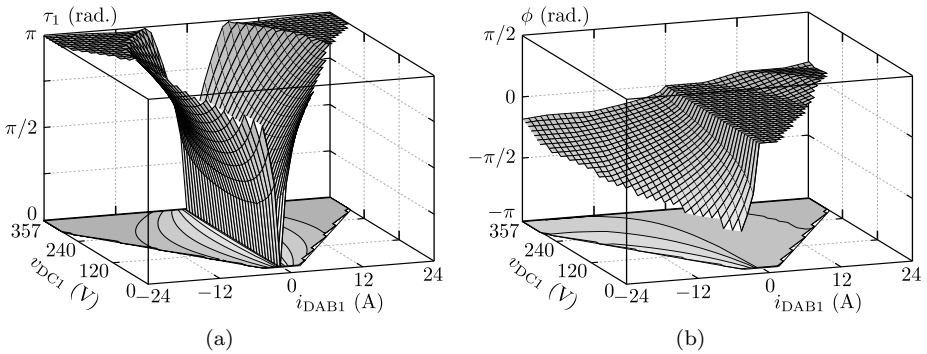


Figure B.1: Supplement to Figure 4.2: results of the numerical search for optimal modulation schemes according to simulation example 1 (1st run): no use of commutation inductances ($L_{c1} = L_{c2} = \infty$). The optimizer is subjected to the CB ZVS conditions, using all possible switching modes. The output voltage for this example is $V_{DC2} = V_{DC2,nom} = 400$ V.

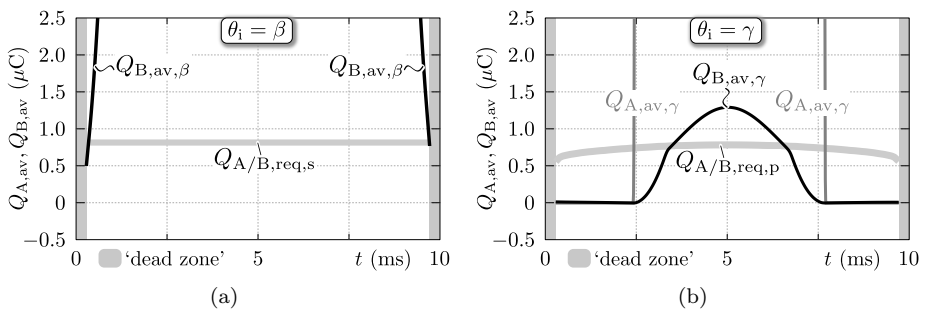


Figure B.2: Supplement to Figure 4.4: resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V. The applied conditions are conform simulation example 1, 1st run (all switching modes included in the optimizer).

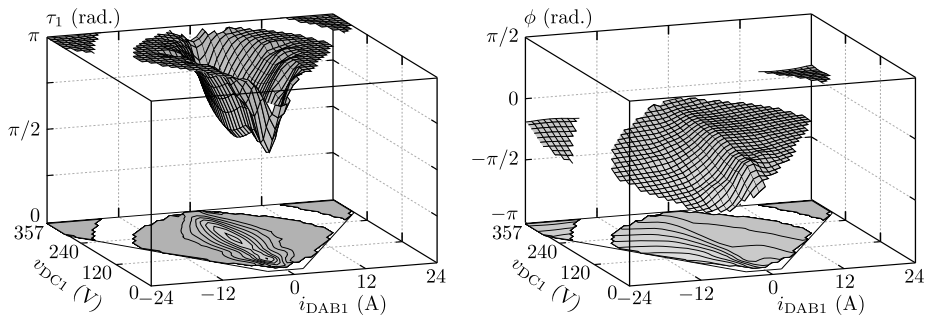


Figure B.3: Supplement to Figure 4.5: results of the numerical search for optimal modulation schemes according to simulation example 1 (2^{nd} run): no use of commutation inductances ($L_{c1} = L_{c2} = \infty$). The optimizer is subjected to the CDCB ZVS conditions, using mode 1 and mode 5 (efficient switching modes) only. The output voltage for this example is $V_{DC2} = V_{DC2,nom} = 400$ V.

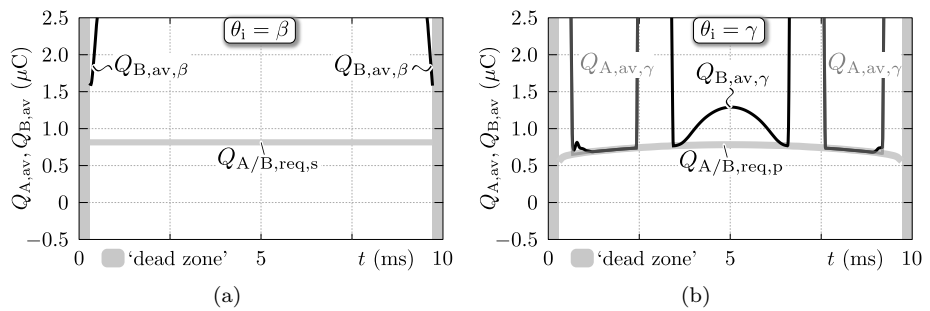


Figure B.4: Supplement to Figure 4.6: resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,nom} = 400$ V. The applied conditions are conform simulation example 1, 2^{st} run (all switching modes included in the optimizer).

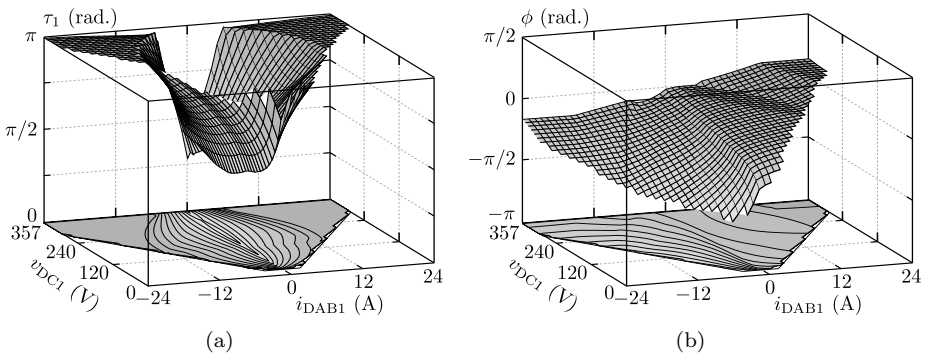


Figure B.5: Supplement to Figure 4.7: results of the numerical search for optimal modulation schemes according to simulation example 2: primary and secondary side commutation inductances included ($L_{c1} = L_{c2} = 62.1$ μH). The optimizer is subjected to the CDCB ZVS conditions, using all possible switching modes. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V.

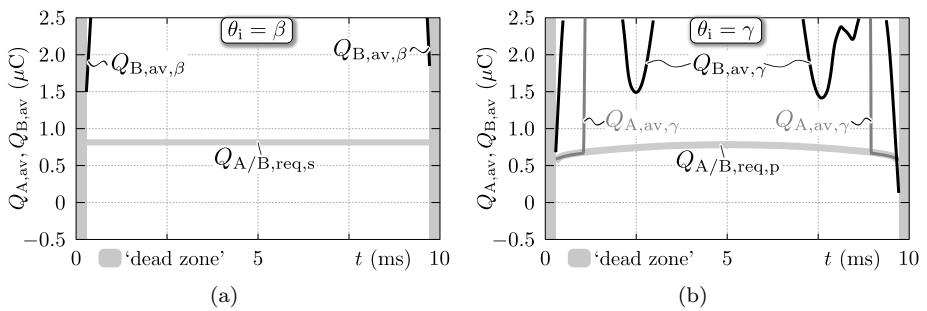


Figure B.6: Supplement to Figure 4.9: resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230$ V_{rms}, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16$ A_{rms}, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The applied conditions are conform simulation example 2 (all switching modes included in the optimizer).

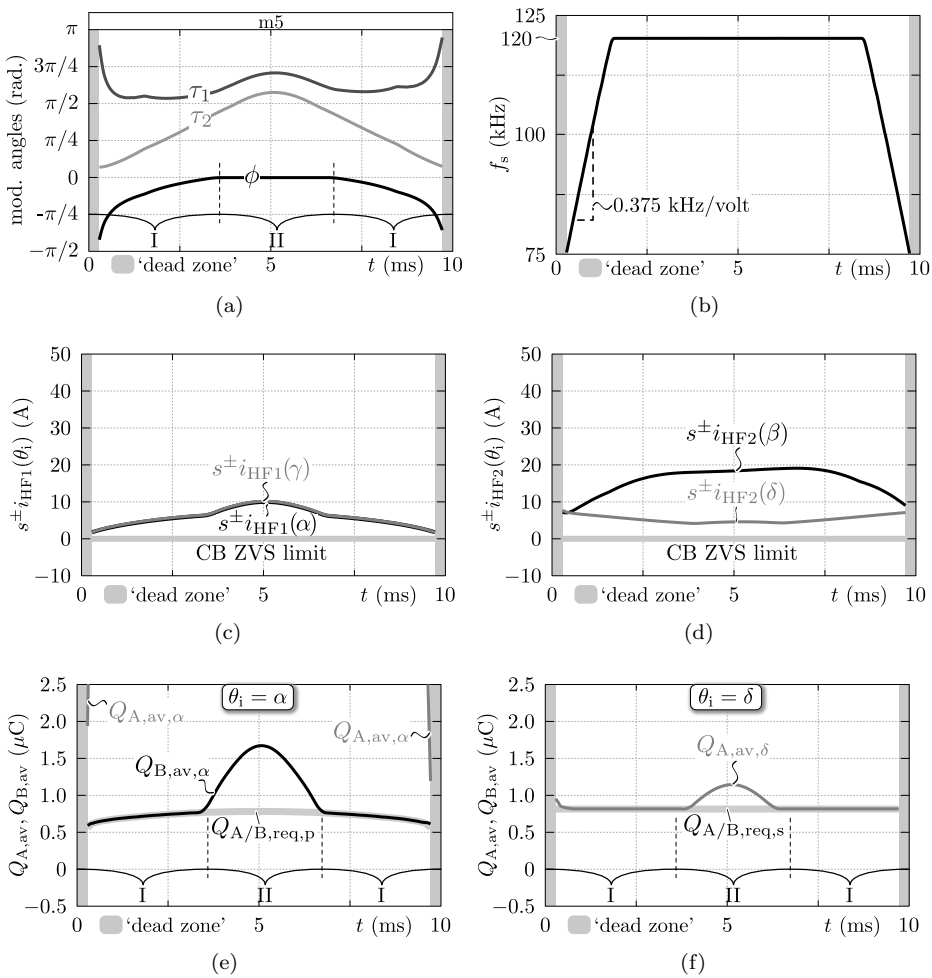


Figure B.7: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at an input current of $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.983$ (cf. Figure 4.3, $i_{\mathrm{DAB1,20\%}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V. The applied conditions are conform simulation example 2 (all switching modes included in the optimizer).

B.2 Results of the Analytical Approach

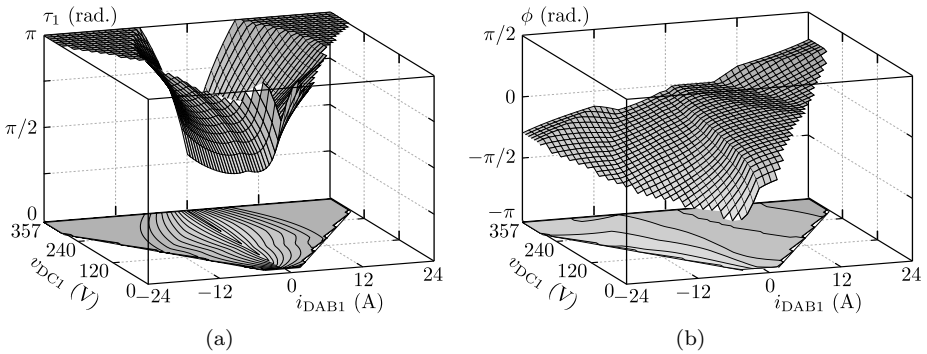


Figure B.8: Supplement to Figure 4.13: results of the analytical calculation of a CDCB ZVS modulation scheme using primary and secondary side commutation inductances $L_{c1} = L_{c2} = 62.1\ \mu$H. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V.

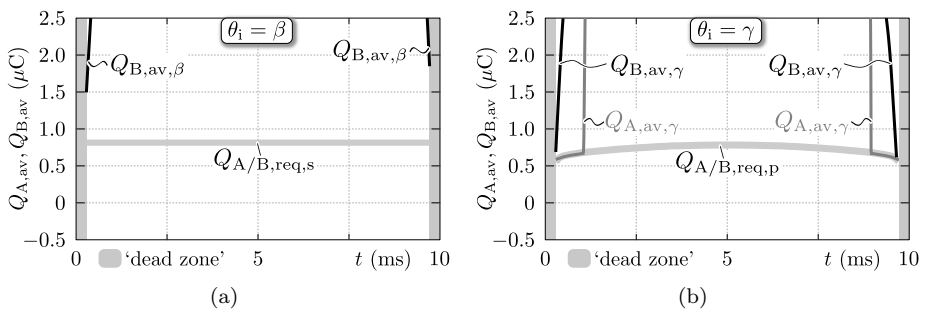


Figure B.9: Supplement to Figure 4.12: resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the analytical approach.

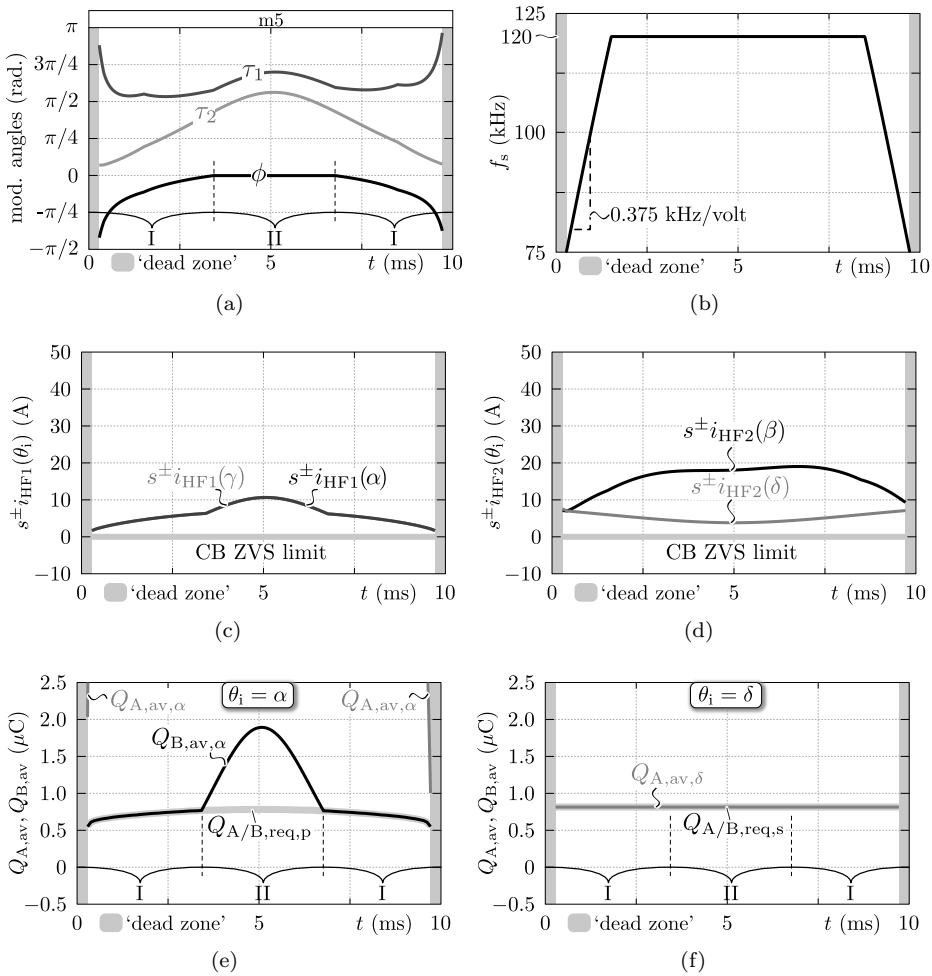


Figure B.10: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at an input current of $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$, a power factor of PF = 0.983 (cf. Figure 4.3, $i_{\mathrm{DAB1,20\%}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,min}} = 370$ V. The modulation parameters are calculated using the analytical approach.

B.3 Results of the Semi-Analytical Approach

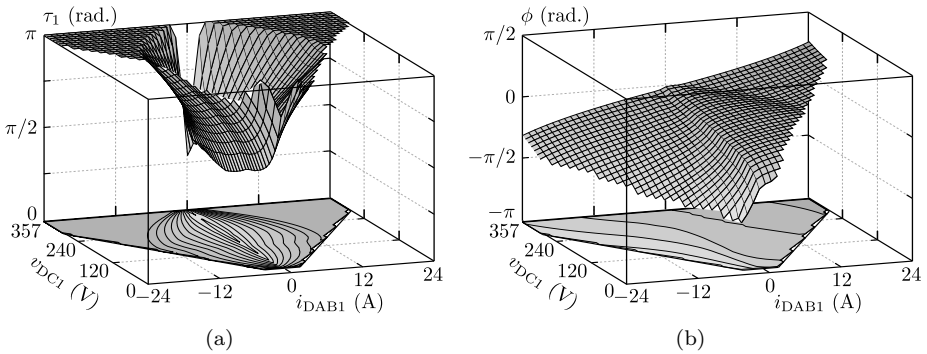


Figure B.11: Supplement to Figure 4.16: results of the semi-analytical calculation of a CDCB ZVS modulation scheme using primary and secondary side commutation inductances $L_{c1} = L_{c2} = 62.1\ \mu$H. The output voltage for this example is $V_{DC2} = V_{DC2,min} = 370$ V.

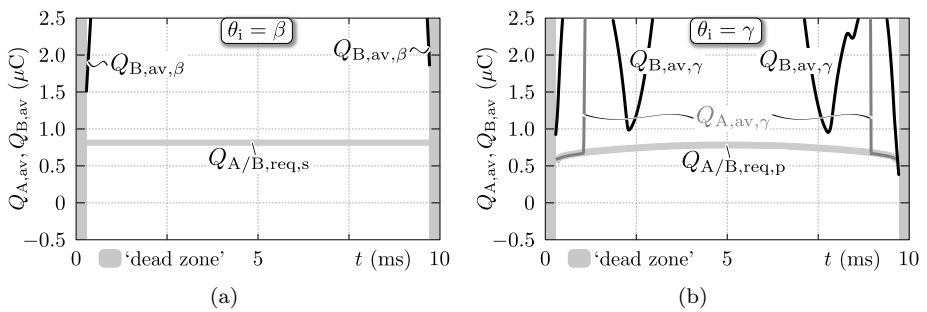


Figure B.12: Supplement to Figure 4.15: resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at the nominal input current of $I_{AC,P} = I_{AC,P,nom} = 16\ A_{rms}$, a power factor of PF = 0.999 (cf. Figure 4.3, $i_{DAB1,nom}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the semi-analytical approach.

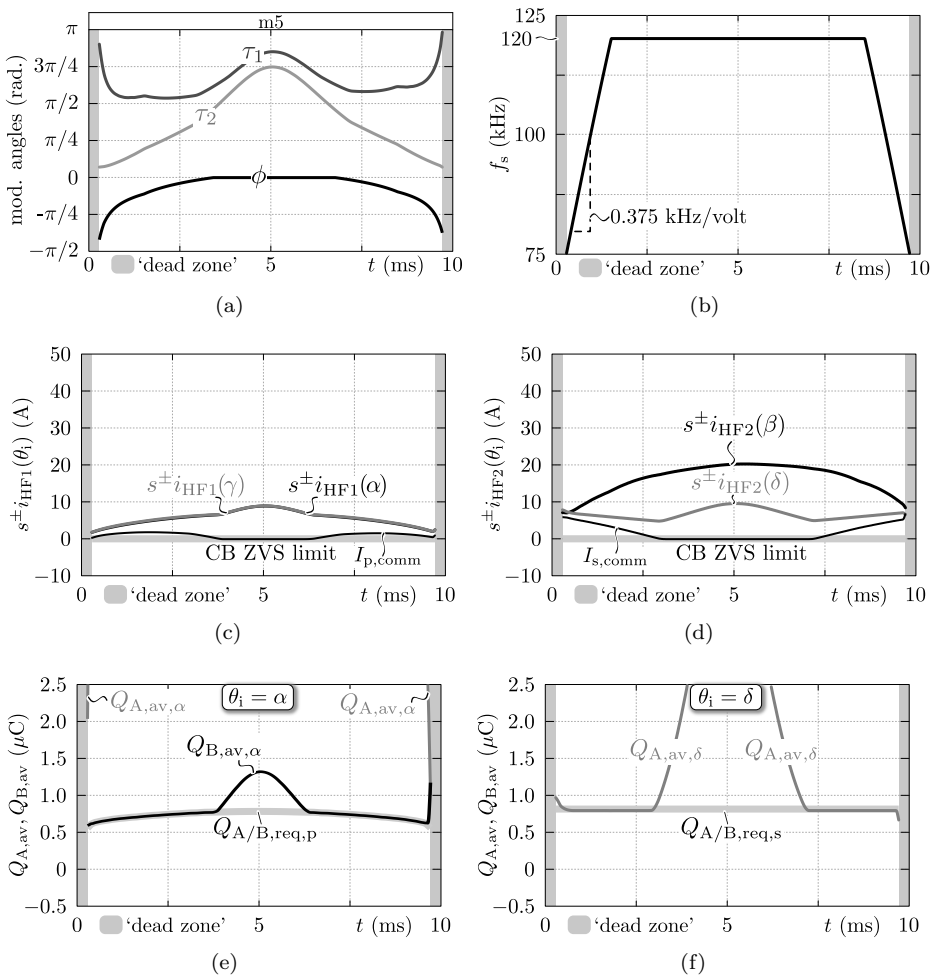


Figure B.13: Resulting value trajectories of several quantities calculated for a half cycle of the nominal AC input voltage of $V_{AC} = 230\ V_{rms}$, at an input current of $I_{AC,P} = 0.2 \cdot I_{AC,P,nom} = 3.2\ A_{rms}$, a power factor of PF = 0.983 (cf. Figure 4.3, $i_{DAB1,20\%}$-line), and an output voltage of $V_{DC2} = V_{DC2,min} = 370$ V. The modulation parameters are calculated using the semi-analytical approach.

B.4 Comparison

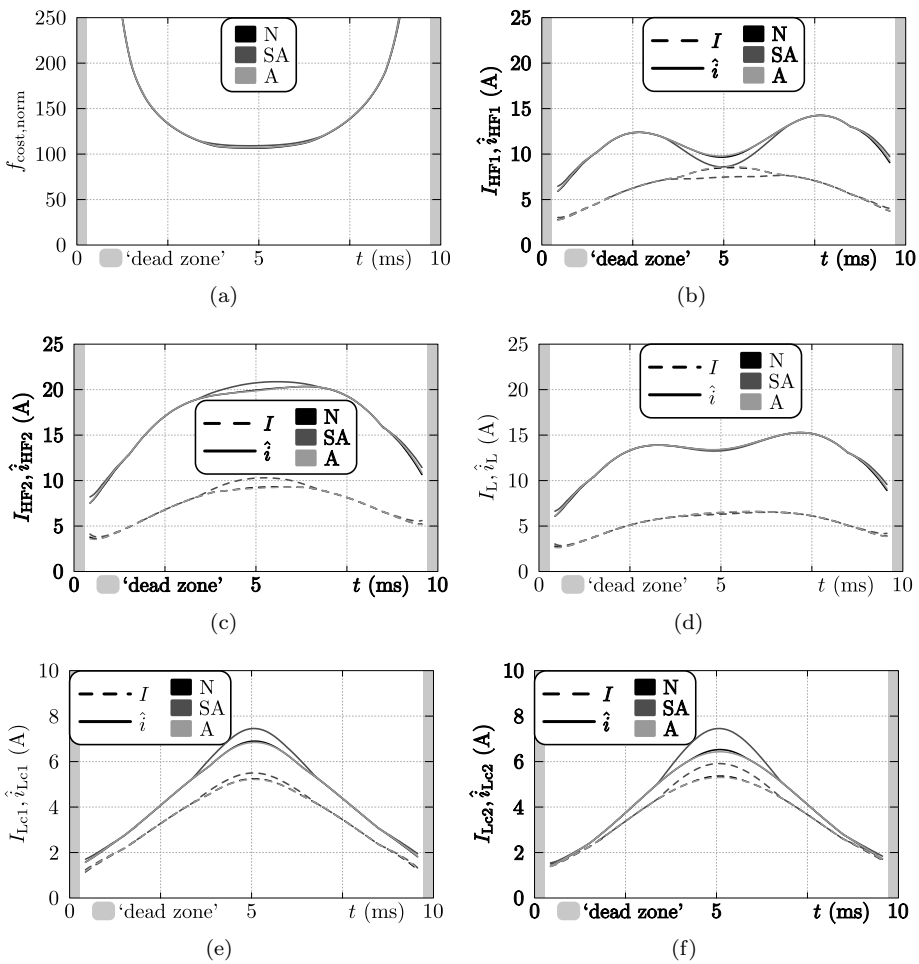


Figure B.14: Resulting value trajectories of several quantities calculated using the three proposed ZVS modulation schemes, for a half cycle of the nominal AC input voltage of $V_{\mathrm{AC}} = 230\ \mathrm{V_{rms}}$, at an input current of $I_{\mathrm{AC,P}} = 0.2 \cdot I_{\mathrm{AC,P,nom}} = 3.2\ \mathrm{A_{rms}}$, a power factor of $\mathrm{PF} = 0.983$ (cf. Figure 4.3, $i_{\mathrm{DAB1,20\%}}$-line), and an output voltage of $V_{\mathrm{DC2}} = V_{\mathrm{DC2,nom}} = 400\ \mathrm{V}$.

C

Supplement to Chapter 5: Modeling of the Main Converter Components

C.1 Heat Sink Optimization for Forced Convection Cooling

Autonomous air cooling by means of forced convection is one of the system requirements defined in Section 1.3, avoiding extension of the existing (typically) water cooling system of the (electric) vehicle. Thereby the heat generated by the power devices is subtracted via a finned heat sink in combination with a fan that blows air through the heat sink channels. For the two active bridges of the DAB, a heat sink geometry with dual-sided base plate, as shown in Figure C.2(a), is considered. The four switches of the primary side active bridge (i.e. active bridge 1, see Figure 3.7) are placed in a row and are mounted on the top-side base plate. As explained in Section 5.1.2, from the heat transfer perspective and regarding stationary heat transfer, they can be represented by an equivalent power source $P_{\mathrm{AB1,eq}}$, which has a power level that is equal to the average losses generated by the four switches during the mains period. The same goes for the four switches of the secondary side active bridge (i.e. active bridge 2, see Figure 3.7) which are mounted on the bottom-side base plate and can be represented by an equivalent power source $P_{\mathrm{AB2,eq}}$. For the synchronous rectifier (SR), a heat sink geometry with single-sided base plate is selected, as shown in Figure C.4(a). The four switches of the SR can once more be represented by an equivalent power source $P_{\mathrm{SR,eq}}$. The final heat sink - semiconductor assemblies for the DAB and for the SR are respectively depicted in Figures C.1(a) and C.1(b).

Optimization of a heat sink, employing forced convection, involves calculation of the thermal resistance of the heat sink material, the thermal resistance due to convection, and the temperature increase of the air flowing through the heat sink channels [16, 114, 115]. Generally, a pressure drop Δp_{CH} appears across these

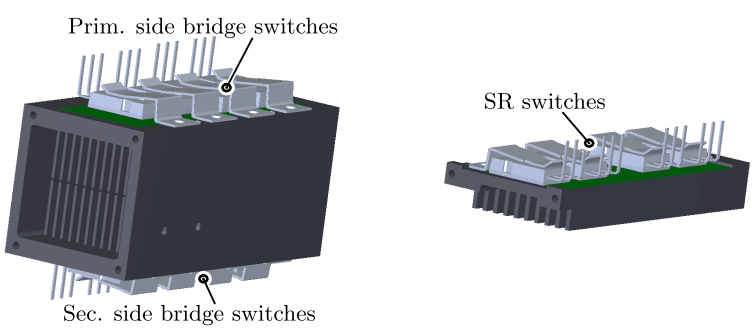


Figure C.1: Heat sink - semiconductor assemblies for (a) the DAB and (b) the SR.

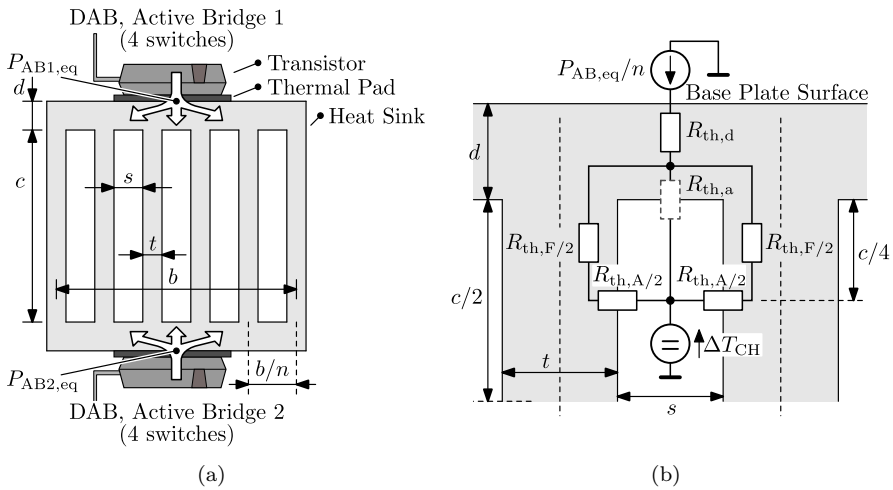


Figure C.2: (a) Heat sink geometry with dual-sided base plate, considered to cool the switches of the DAB's active bridges. (b) Thermal network describing stationary heat transfer between the surface of one of the two base plates and the air in the heat sink channel (temperature T_{CH}).

channels due to the airflow imposed by the fan. The exact operating point, i.e. the resulting channel pressure drop and the air flow rate, strongly depends on the fin geometry and on the fan characteristic (i.e. the pressure-flow curve), and can be calculated employing analytical and empirical equations. In addition, the relation between the total thermal resistance of the heat sink, the fin geometry, and the air flow rate (i.e. the operating point of the fan) can be analytically described, taking into account the properties of air, the properties of the heat sink material, and the type of airflow (i.e. laminar of turbulent). All equations can be numerically solved, enabling a systematic optimization of the fin geometry for a given fan. Below, such an optimization is performed for both the heat sink with double-sided base plate which is considered to cool the switches of the DAB, and the heat sink with single-sided base plate for cooling the switches of the SR. Thereby the detailed procedure described in [114, 115], which only considers stationary heat transfer, is followed.

C.1.1 Heat Sink with Dual-Sided Base Plate

For the heat sink geometry shown in Figure C.2(a), considered to cool the switches of the DAB, with an equivalent power source $P_{\mathrm{AB1,eq}}$ attached to the top-side base plate and an equivalent power source $P_{\mathrm{AB2,eq}}$ attached to the bottom-side

base plate, the heat transfer (i.e. a combination of conductive and convective heat transfer) from one of the two power sources (i.e. seen from one side) to the air in the heat sink channel, and regarding a single air channel, is modeled[1] according to Figure C.2(b). The thermal resistance from the base plate surface (index 'S': Surface) to the air in the channel (index AF: Air Flow) is calculated with:

$$R^{(n)}_{\text{th,S-AF}} = R_{\text{th,d}} + 0.5\,(R_{\text{th,F/2}} + R_{\text{th,A/2}}), \tag{C.1}$$

where

$$R_{\text{th,d}} = \frac{d}{\frac{1}{n}\,A_{\text{BP}}\,\lambda_{\text{HS}}}, \qquad R_{\text{th,F/2}} = \frac{\frac{1}{4}\,c}{\frac{1}{2}\,t\,L\,\lambda_{\text{HS}}}, \qquad R_{\text{th,A/2}} = \frac{1}{h\,L\,\frac{1}{2}\,c}. \tag{C.2}$$

Note that the convective thermal resistance $R_{\text{th,a}}$ (see Figure C.2(b)) is much larger than $R_{\text{th,A/2}}$ for geometries with $s << c$ and can thus be neglected. For n channels, the thermal resistance from the base plate surface to the ambient (index 'Am'), i.e. the air temperature at the heat sink inlet, is calculated with:

$$R_{\text{th,S-Am}} = \frac{1}{n}\,R^{(n)}_{\text{th,S-AF}} + R_{\text{th,AF-Am}}, \tag{C.3}$$

where $R_{\text{th,AF-Am}}$ relates to the average temperature rise of the air in the channel and is determined by:

$$R_{\text{th,AF-Am}} = \frac{0.5}{\rho_{\text{AIR}}\,c_{\text{p,AIR}}\,0.5\,\dot{V}_{\text{AF}}}. \tag{C.4}$$

$\dot{V}_{\text{AF}}$ is the total volume flow (air flow rate) of the air in the heat sink channels. The different variables[2] required to calculate the total thermal resistance $R_{\text{th,S-Am}}$ from the base plate surface to the ambient, i.e. according to (C.3), are listed and further declared in Table C.1. Thereby, the convective heat transfer coefficient h is calculated with:

$$h = \frac{Nu_{\text{avg}}\,\lambda_{\text{AIR}}}{d_{\text{h}}}, \tag{C.5}$$

[1] The heat transfer modeling is valid when the power levels of the equivalent power sources $P_{\text{AB1,eq}}$ and $P_{\text{AB2,eq}}$ are not substantially different (i.e. $P_{\text{AB1,eq}} \approx P_{\text{AB2,eq}}$). The same remark applies for the equivalent power sources of the individual switches (i.e. $P_{\text{AB1,eq}} \approx 4 \cdot P_{\text{S}_{1\text{x}},\text{eq}}$ and $P_{\text{AB2,eq}} \approx 4 \cdot P_{\text{S}_{2\text{x}},\text{eq}}$). This is the case due to the symmetry of the DAB and due to the fact that the currents flowing in the switches of an active bridge have equal RMS values (see Section 5.1.2).

[2] Pr, ρ_{AIR}, ν_{AIR}, and λ_{AIR} are slightly temperature dependent. In order to simplify the analysis, an average channel air temperature of $T_{\text{CH}} = 80°\text{C}$ is assumed.

which requires the hydraulic diameter d_h of one channel according to:

$$d_\mathrm{h} = \frac{2\,s\,c}{s+c}. \tag{C.6}$$

The calculation of the average Nusselt number Nu_avg, which is required in (C.5), depends on whether the airflow in the channels is laminar or turbulent. For laminar airflow Nu_avg is calculated with:

$$Nu_\mathrm{avg,lam} = \frac{3.657\,(\tanh(2.264\,X^{1/3} + 1.7\,X^{2/3}))^{-1} + \dfrac{0.0499}{X}\tanh(X)}{\tanh(2.432\,Pr^{1/6}\,X^{1/6})}, \tag{C.7}$$

while for turbulent airflow Nu_avg is determined by:

$$\begin{aligned} Nu_\mathrm{avg,turb} = & \frac{(8\,(0.79\,\ln(Re_\mathrm{avg}) - 1.64)^2))^{-1}\,(Re_\mathrm{avg} - 1000)\,Pr}{1 + 12.7\,\sqrt{(8\,(0.79\,\ln(Re_\mathrm{avg}) - 1.64)^2)^{-1}}\,(Pr^{2/3} - 1)} \\ & \cdot \left(1 + \left(\frac{d_\mathrm{h}}{L}\right)^{2/3}\right), \end{aligned} \tag{C.8}$$

with

$$X = \frac{L}{d_\mathrm{h}\,Re_\mathrm{avg}\,Pr}. \tag{C.9}$$

The type of airflow (laminar or turbulent) and thus the selection of the equation, (C.7) or (C.8), used to calculate Nu_avg, depends on the average Reynolds number according to:

$$Nu_\mathrm{avg} = \begin{cases} Nu_\mathrm{avg,lam} & \text{if } Re_\mathrm{avg} < 2300, \\ Nu_\mathrm{avg,turb} & \text{if } Re_\mathrm{avg} \geqslant 2300, \end{cases} \tag{C.10}$$

where the average Reynolds number Re_avg is calculated using:

$$Re_\mathrm{avg} = \frac{2\,\dot{V}_\mathrm{AF}}{n\,(s+c)\,\nu_\mathrm{AIR}}. \tag{C.11}$$

Given a certain heat sink geometry with predefined d, t, b, c, s, L, and n, the only quantity that is still required in order to evaluate the above equations and to calculate the total thermal resistance $R_\mathrm{th,S\text{-}Am}$ seen by one power source, is the

Variable	*Unit*	*Description*
d	m	base plate thickness
t	m	width of a fin
b	m	total width of all air channels
c	m	total height of the air channel (=height of the fins)
s	m	width of a single air channel
L	m	length of the air channels
n		number of channels
k		fin spacing ratio acc. to (C.16)
A_{BP}	m^2	area of the heat sink base plate ($A_{\mathrm{BP}} = L \cdot b$)
d_{h}	m	hydraulic diameter of one channel acc. to (C.6)
Δp_{CH}	$\mathrm{N/m}^2$	pressure drop across the heat sink channels
$\dot{V}_{\mathrm{AF}}$	m^3/s	total volume flow of the air in the heat sink channels
Re_{avg}		average Reynolds number acc. to (C.11)
$Pr \approx 0.71$		Prandtl number (air, 80°C)
Nu_{avg}		average Nusselt number acc. to (C.7) for laminar airflow or acc. to (C.8) for turbulent airflow
h	$\mathrm{W/m^2K}$	convective heat transfer coefficient acc. to (C.5)
λ_{HS}	W/mK	thermal conductivity of the heat sink material
$\rho_{\mathrm{AIR}} \approx 0.99$	$\mathrm{kg/m}^3$	air density (80°C)
$\nu_{\mathrm{AIR}} \approx 2.1\mathrm{e}^{-5}$	m^2/s	cinematic viscosity of air (80°C)
$c_{\mathrm{p,AIR}} \approx 1010$	J/kgK	specific thermal capacitance of air
$\lambda_{\mathrm{AIR}} \approx 0.03$	W/mK	thermal conductivity of air (80°C)

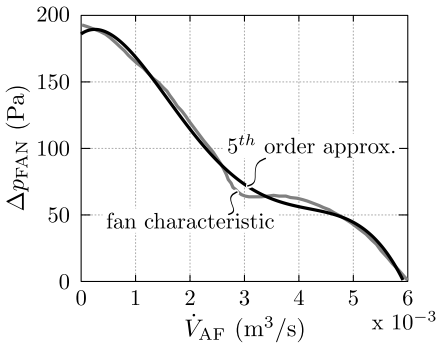
Table C.1: Declaration of the different variables required in the equations for the calculation of the thermal resistance of a finned heat sink with fan, and for the calculation of the air flow rate in, and the total pressure drop across the air channels of the heat sink. Source: [115].

total volume flow $\dot{V}_{\mathrm{AF}}$ of the air in the heat sink channels. $\dot{V}_{\mathrm{AF}}$ is determined by the operating point of the fan, which can be found by balancing the equations that describe the relation between the pressure drop Δp_{CH} across the channels, the heat sink geometry, and $\dot{V}_{\mathrm{AF}}$, with the pressure-flow curve (i.e. $\Delta p_{\mathrm{FAN}}(\dot{V}_{\mathrm{AF}})$) of the fan. For laminar airflow Δp_{CH} is calculated with:

$$\Delta p_{\mathrm{CH,lam}}(\dot{V}_{\mathrm{AF}}) = \frac{48\,\rho_{\mathrm{AIR}}\,\nu_{\mathrm{AIR}}\,L}{n\,s\,c\,d_{\mathrm{h}}^2} \cdot \dot{V}_{\mathrm{AF}}, \tag{C.12}$$

while for turbulent airflow Δp_{CH} is determined by:

$$\Delta p_{\mathrm{CH,turb}}(\dot{V}_{\mathrm{AF}}) = \frac{\frac{L}{d_{\mathrm{h}}}\,\rho_{\mathrm{AIR}}\,0.5\,(\frac{\dot{V}_{\mathrm{AF}}}{n\,s\,c})^2}{(0.79\,\ln\left(\frac{2\,\dot{V}_{\mathrm{AF}}}{n\,(s+c)\,\nu_{\mathrm{AIR}}}\right) - 1.64)^2}. \tag{C.13}$$



(a)

(b)

Figure C.3: (a) Datasheet pressure-flow curve (gray line), and 5^{th} order approximation (black line) of the characteristic, for the selected fan: SanAce40GA, type 9GA0412P7G001, 40x40x15 mm, 12 V DC. (b) Picture of the SanAce40GA.

The pressure-flow curve, $\Delta p_{\mathrm{FAN}}(\dot{V}_{\mathrm{AF}})$, of the selected fan[3] is depicted in Figure C.3(a) (gray line) and can be described by a 5^{th} order approximation (black line in Figure C.3(a)):

$$\begin{aligned}\Delta p_{\mathrm{FAN}}(\dot{V}_{\mathrm{AF}}) =& (5.38 \cdot 10^{13} \cdot \dot{V}_{\mathrm{AF}}^5 - 2.115 \cdot 10^{12} \cdot \dot{V}_{\mathrm{AF}}^4 + 1.96 \cdot 10^{10} \cdot \dot{V}_{\mathrm{AF}}^3 \\ & - 6.315 \cdot 10^{7} \cdot \dot{V}_{\mathrm{AF}}^2 + 2.828 \cdot 10^{4} \cdot \dot{V}_{\mathrm{AF}} + 185.7).\end{aligned} \tag{C.14}$$

Under the assumption of laminar airflow, $\dot{V}_{\mathrm{AF}}$ is found by balancing (C.14) with (C.12):

$$\begin{aligned} k\,\Delta p_{\mathrm{FAN}}(\dot{V}_{\mathrm{AF}}) &= \Delta p_{\mathrm{CH,lam}}(\dot{V}_{\mathrm{AF}}) \\ &\rightarrow\ \dot{V}_{\mathrm{AF}}, \end{aligned} \tag{C.15}$$

where k is the fin spacing ratio defined by:

$$k = \frac{s}{b/n}, \tag{C.16}$$

which is introduced in order to take into account the pressure losses at the channel inlet that are the result of a reduction (related to the fin thickness) of the cross

[3]The SanAce40GA fan (type 9GA0412P7G001, see Figure C.3(b)) has been selected due to its high static pressure, high air flow rate, and low sound pressure level, in combination with an ultra low power consumption.

section area available for airflow, i.e. $A_{\text{cross}} = k \cdot b \cdot c$, with $0 < k < 1$. If the Reynolds number calculated using the resulting $\dot{V}_{\text{AF}}$ is smaller than 2300, the airflow is laminar and $R_{\text{th,S-Am}}$ needs to be evaluated using the Nusselt number $Nu_{\text{avg,lam}}$ defined by (C.7). If the Reynolds number calculated using the resulting $\dot{V}_{\text{AF}}$ is higher than 2300, the air flow is turbulent and $\dot{V}_{\text{AF}}$ needs to be recalculated by solving:

$$\begin{aligned} k\,\Delta p_{\text{FAN}}(\dot{V}_{\text{AF}}) &= \Delta p_{\text{CH,turb}}(\dot{V}_{\text{AF}}) \\ &\rightarrow\ \dot{V}_{\text{AF}}. \end{aligned} \tag{C.17}$$

Subsequently, $R_{\text{th,S-Am}}$ needs to be reevaluated using the Nusselt number $Nu_{\text{avg,turb}}$ defined by (C.8). By repeating the above procedure for different heat sink geometries, an optimal set of parameters (d, t, b, c, s, L, and n) can be found which leads to the lowest thermal resistance $R_{\text{th,S-Am}}$ from the base plate surface to the ambient.

C.1.2 Heat Sink with Single-Sided Base Plate

For the heat sink geometry shown in Figure C.4(a), considered to cool the switches of the SR, with an equivalent power source $P_{\text{SR,eq}}$ attached to the base plate, the heat transfer (i.e. a combination of conductive and convective heat transfer) from the power source to the air in the heat sink channel, and regarding a single air channel, is modeled[4] according to Figure C.4(b). The calculation/optimization procedure outlined in Section C.1.1, for a heat sink geometry with dual-sided base plate, is still valid but the calculation of the conductive and convective heat transfer through the fins has to be adapted. According to Figure C.4(b), the thermal resistance from the base plate surface (index 'S': Surface) to the air in the channel (index AF: Air Flow) is now determined by:

$$R^{(n)}_{\text{th,S-AF}} = R_{\text{th,d}} + 0.5\,(R_{\text{th,F}} + R_{\text{th,A}}), \tag{C.18}$$

where

$$R_{\text{th,d}} = \frac{d}{\frac{1}{n}\,A_{\text{BP}}\,\lambda_{\text{HS}}}, \qquad R_{\text{th,F}} = \frac{\frac{1}{2}\,c}{\frac{1}{2}\,t\,L\,\lambda_{\text{HS}}}, \qquad R_{\text{th,A}} = \frac{1}{h\,L\,c}. \tag{C.19}$$

Note that the convective thermal resistance $R_{\text{th,a}}$ (see Figure C.4(b)) is again

[4]The heat transfer modeling is valid when the equivalent power sources of the individual switches are not substantially different (i.e. $P_{\text{SR,eq}} \approx 4 \cdot P_{\text{S}_{\text{SRx}},\text{eq}}$). This is the case due to the fact that the currents flowing in the switches of the SR have equal RMS values (see Section 5.1.2).

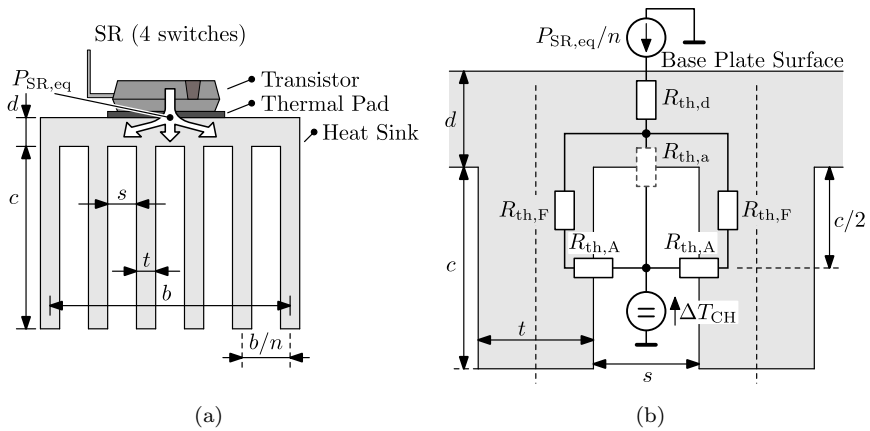


Figure C.4: (a) Heat sink geometry with single-sided base plate, considered to cool the switches of the SR. (b) Thermal network describing stationary heat transfer between the surface of the base plate and the air in the heat sink channel (temperature T_{CH}).

neglected as it is much larger than $R_{\mathrm{th,A}}$ for geometries with $s << c$. For n channels, the thermal resistance from the base plate surface to the ambient (i.e. the air temperature at the heat sink inlet) is calculated with:

$$R_{\mathrm{th,S\text{-}Am}} = \frac{1}{n} R^{(n)}_{\mathrm{th,S\text{-}AF}} + R_{\mathrm{th,AF\text{-}Am}}, \tag{C.20}$$

where $R_{\mathrm{th,AF\text{-}Am}}$ represents the average temperature rise of the air in the channel, which now is defined by:

$$R_{\mathrm{th,AF\text{-}Am}} = \frac{0.5}{\rho_{\mathrm{AIR}}\, c_{\mathrm{p,AIR}}\, \dot{V}_{\mathrm{AF}}}. \tag{C.21}$$

All the other equations presented in Section C.1.1 for the heat sink geometry with dual-sided base plate still hold and a geometry optimization for the heat sink with single-sided base plate can be performed accordingly.

C.1.3 Results of the Heat Sink Optimizations

Below, the optimization procedure is applied to the heat sink used to cool the switches of the DAB (heat sink geometry with dual-sided base plate, cf. Section C.1.1) and the heat sink used to cool the switches of the SR (heat sink geometry with single-sided base plate, cf. Section C.1.2).

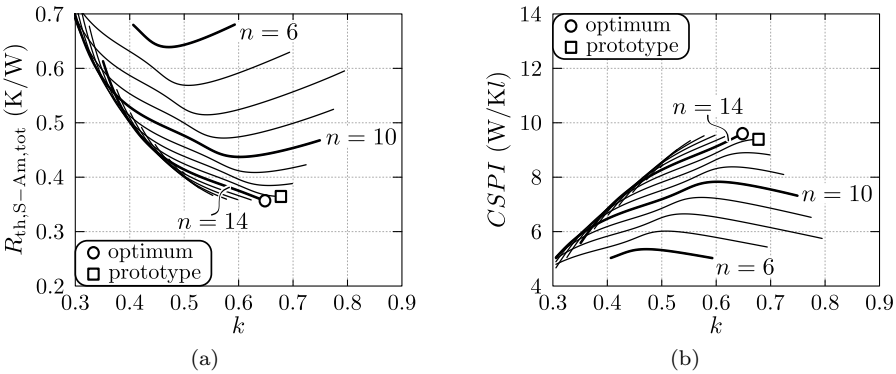


Figure C.5: Optimization result for the heat sink used to cool the switches of the DAB (heat sink geometry with dual-sided base plate, cf. Section C.1.1), assuming a minimum achievable fin thickness and a minimum achievable channel width of 1 mm (i.e. the optimization is performed under the '1 mm constraint'). (a) Total thermal resistance $R_{\text{th,S-Am,tot}}$ ($= 0.5 \cdot R_{\text{th,S-Am}}$) from the base plate surfaces to the ambient as function of the two geometric parameters n and k that are independently varied. (b) Cooling system performance index $CSPI$ as function of the two geometric parameters n and k.

Heat Sink of the DAB

The fan size defines the heat sink front geometry as only the fins that are facing the fan, and thus the airflow, contribute to the (forced) convective heat transfer. After thorough iteration of the mechanical design of the final prototype converter, a 40x40 mm fan turned out to be most feasible, leading to the selection of the SanAce40GA (see Figure C.3). Consequently, a heat sink geometry with $b = c = 40$ mm is most appropriate in order to fully utilize the fan. The length L of the heat sink channels must be large enough so that sufficient space is provided on the base plates to mount the switches. Assuming a minimum spacing of 5 mm between the packages of adjacent switches (remind that four switches are placed on each base plate), a minimum spacing of 10 mm between the base plate borders and a package, and a package width of approximately 16 mm (i.e. MOSFETs with TO-247 package are used for the DAB, see Section 5.1.1), the minimum base plate length becomes $L_{\text{min}} = 3 \cdot 5 \text{ mm} + 2 \cdot 10 \text{ mm} + 4 \cdot 16 \text{ mm} = 99 \text{ mm}$. Preferably the maximum base plate length should not be much higher than L_{min}, assuring homogeneous heat distribution across the base plate, which acts as a heat spreader. In order to fit into the final mechanical design and taking into account mounting restrictions, the resulting base plate length is $L = 99.8$ mm. The base plate thickness d is an important parameter regarding heat spreading and should be large enough to homogeneously distribute the heat (i.e. avoiding hot spots) and

small enough to limit the thermal resistance of the heat sink. The value $d = 6$ mm is selected as a good trade-off between these two considerations. As a result, the parameters that are varied during the optimization are the number of fins n and the fin spacing ratio k (this is equivalent to varying the fin width t and the channel width s). Figure C.5 shows the results of the optimization, applying the assumed (see above) outer heat sink dimensions and assuming a minimum achievable fin thickness and channel width of 1 mm (further referred to as the '1 mm constraint'). Fin thicknesses and channel widths in the range of 1 mm are enabled by for example using high-end milling machines. Furthermore, aluminium is considered for the heat sink material, defining the thermal conductivity value $\lambda_{\mathrm{HS}} = 210$ W/mK. Figure C.5(a) depicts the relation between $R_{\mathrm{th,S\text{-}Am,tot}}$ $(= 0.5 \cdot R_{\mathrm{th,S\text{-}Am}})$[5] and the two geometric parameters n and k that are independently varied. The performance indices and parameter values for the resulting (optimal) heat sink design (named design 'B', optimization performed under the '1 mm constraint') are given in the middle inset of Table C.2. V_{HS} is the boxed volume of the heat sink, excluding the fan and an additional airflow inlet between the fan and the heat sink. V_{CS} is the volume of the cooling system, including the heat sink, the fan, and an additional airflow inlet between the fan and the heat sink. $CSPI$ is the cooling system performance index [16, 114, 115], which is an objective measure that allows to compare different cooling system designs with regard to power density. For the cooling system of the DAB, with dual-sided base plate, $CSPI$ is defined as [114]:

$$CSPI = \frac{1}{R_{\mathrm{th,S\text{-}Am,tot}} \cdot V_{\mathrm{CS}}} = \frac{1}{0.5 \cdot R_{\mathrm{th,S\text{-}Am}} \cdot V_{\mathrm{CS}}}. \tag{C.22}$$

If a heat sink design shows a $CSPI$ that is two times higher than the $CSPI$ of another one, the cooling volume V_{CS} can be made two times smaller in order to achieve the same thermal resistance. Knowing that typical commercially available heat sink - fan combinations have a $CSPI$ of around 5 [114], the extensive heat sink optimization performed above is justified. The (boxed) volume $V_{\mathrm{CS,tot}}$, which besides the heat sink, the fan, and the airflow inlet also includes the semiconductor switching devices, is also listed in Table C.2. The bottom inset of Table C.2 shows the performance indices and design parameters of an even further optimized heat sink design (named design 'C'), resulting from an optimization in which a minimum achievable fin thickness and channel width of 0.3 mm (further referred to as the '0.3 mm constraint') are assumed. Fin thicknesses and channel widths in the range of 0.3 mm are enabled by for example using (expensive) electrical discharge machining. The top inset of Table C.2 shows the performance indices and design parameters of the heat sink used in the final prototype converter (named design 'A'), which in fact is a suboptimal design since the minimum achievable thickness of the heat sink fins and the minimum achievable channel width were restricted due to limitations of the in-house manufacturing machines/tools.

[5] The multiplication of $R_{\mathrm{th,S\text{-}Am}}$ with a factor '0.5' is required since $R_{\mathrm{th,S\text{-}Am}}$ is experienced from just one base plate of the heat sink and thus has to be divided by two in order to take both base plates (top and bottom) into account.

	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design A	99.8	37	6	40.3	13	2.1	1	0.6774
prototype	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{\mathrm{CS,tot}}$ (liter, l)		$R_{\mathrm{th,S\text{-}Am}}$ (K/W)	$R_{\mathrm{th,S\text{-}Am,tot}}$ (K/W)		$CSPI$ (W/K l)
	0.2279	0.2918	0.399		0.7298	0.3649		9.3907
	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design B	99.8	37	6	40.3	14	1.9	1	0.6482
'1 mm constr.'	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{\mathrm{CS,tot}}$ (liter, l)		$R_{\mathrm{th,S\text{-}Am}}$ (K/W)	$R_{\mathrm{th,S\text{-}Am,tot}}$ (K/W)		$CSPI$ (W/K l)
	0.2279	0.2918	0.399		0.7142	0.3571		9.5967
	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design C	99.8	37	6	40.3	24	1.4	0.304	0.8191
'0.3 mm constr.'	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{\mathrm{CS,tot}}$ (liter, l)		$R_{\mathrm{th,S\text{-}Am}}$ (K/W)	$R_{\mathrm{th,S\text{-}Am,tot}}$ (K/W)		$CSPI$ (W/K l)
	0.2279	0.2918	0.399		0.5510	0.2755		12.44

Table C.2: Performance indices and parameter values that result from the optimization of the heat sink used to cool the switches of the DAB (heat sink geometry with dual-sided base plate, cf. Section C.1.1). Bottom inset (design C): result of the optimization performed under the '0.3 mm constraint', middle inset (design B): result of the optimization performed under the '1 mm constraint', top inset (design A): heat sink used in the final prototype converter.

Heat Sink of the SR

For the heat sink of the SR, once more the 40x40 mm SanAce40GA fan (see Figure C.3) is selected. However, as the SR requires less cooling effort than the DAB, the heat sink's front geometry values are reduced from $b = c = 40$ mm (most appropriate in order to fully utilize the fan) to $b = 36$ mm and $c = 10$ mm. This allows to use part of the fan's airflow to cool other electronic components. The reduced airflow in the heat sink channels due to the area reduction of the heat sink's front geometry is taken into account by multiplying $\dot{V}_{\mathrm{AF}}$ with the heat-sink-front-area to fan-area ratio $(b \cdot c)/(40 \cdot 40)$. Furthermore, the length of the channel inlet is slightly reduced compared to the heat sink used to cool the switches of the DAB, leading to an increased total channel length of $L = 104$ mm. Furthermore, a base plate thickness of $d = 5$ mm is applied.

The performance indices and parameter values for the resulting (optimal) heat sink designs are given in Table C.3, where the bottom table inset (design C) corresponds with the optimization performed under the '0.3 mm constraint', the middle table inset (design B) with the optimization performed under the '1 mm constraint', and the top table inset (design A) with heat sink design used in the

	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design A	104	10	5	36	9	2.5	1.5	0.625
prototype	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{CS,tot}$ (liter, l)		$R_{th,S\text{-}Am}$ (K/W)	$R_{th,S\text{-}Am,tot}$ (K/W)		$CSPI$ (W/K l)
	0.0624	0.0767	0.1227		1.7264	1.7264		7.5542
	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design B	104	10	5	36	14	1.6	1	0.608
'1 mm constr.'	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{CS,tot}$ (liter, l)		$R_{th,S\text{-}Am}$ (K/W)	$R_{th,S\text{-}Am,tot}$ (K/W)		$CSPI$ (W/K l)
	0.0624	0.0767	0.1227		1.4372	1.4372		9.0741
	Predef. values				*Calc. optimal values*			
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Design C	104	10	5	36	21	1.4	0.301	0.8241
'0.3 mm constr.'	V_{HS} (liter, l)	V_{CS} (liter, l)	$V_{CS,tot}$ (liter, l)		$R_{th,S\text{-}Am}$ (K/W)	$R_{th,S\text{-}Am,tot}$ (K/W)		$CSPI$ (W/K l)
	0.0624	0.0767	0.1227		1.0634	1.0634		12.264

Table C.3: Performance indices and parameter values resulting from the optimization of the heat sink used to cool the switches of the SR (heat sink geometry with single-sided base plate, cf. Section C.1.2). Bottom inset (design C): result of the optimization performed under the '0.3 mm constraint', middle inset (design B): result of the optimization performed under the '1 mm constraint', top inset (design A): heat sink used in the final prototype converter.

final prototype converter which again is a suboptimal design since the minimum achievable thickness of the heat sink fins and the minimum achievable channel width were restricted due to limitations of the in-house manufacturing machines/tools. Remind that V_{HS} is the boxed volume of the heat sink, excluding the fan and an additional airflow inlet between the fan and the heat sink. V_{CS} is the volume of the cooling system, including the heat sink, the fan, and an additional airflow inlet between the fan and the heat sink. For the cooling system of the SR, with single-sided base plate, $CSPI$ is calculated with [115]:

$$CSPI = \frac{1}{R_{th,S\text{-}Am} \cdot V_{CS}}. \tag{C.23}$$

The (boxed) volume $V_{CS,tot}$, which besides the heat sink, the fan, and the airflow inlet also includes the semiconductor switching devices, is also listed in Table C.3. Note that the part of the fan that does not faces fins is not included in the calculation of $V_{CS,tot}$. The final heat sink - semiconductor assembly (DAB and SR) is shown in Figure 5.9 of Section 5.1.3 (see Chapter 5).

Bibliography

[1] European Commission. Energy Strategy for Europe: General website (last accessed: 23/07/2013). [Online]. Available: http://ec.europa.eu/energy/index_en.htm

[2] U.S. Department of Energy. Mission of the U.S. Energy Department: General Website (Last accessed: 23/07/2013). [Online]. Available: http://energy.gov/mission

[3] European Commission, Directorate-General for Research (Sustainable Energy Systems). (2005) Towards Smart Power Networks: Lessons Learned from European Research FP5 Projects (Last accessed: 23/07/2013). [Online]. Available: http://ec.europa.eu/research/energy/pdf/towards_smartpower_en.pdf

[4] U.S. Energy Information Administration (EIA). (2011) International Energy Outlook 2011 (Last accessed: 23/07/2013). [Online]. Available: http://www.eia.gov/forecasts/ieo/pdf/0484(2011).pdf

[5] United Nations Framework Convention on Climate Change (UNFCCC). (1998) Kyoto Protocol (Last accessed: 23/07/2013). [Online]. Available: http://unfccc.int/resource/docs/convkp/kpeng.pdf

[6] J. R. Wilson and G. Burgh, *Energizing Our Future: Rational Choices for the 21st Century*. Hoboken N.J.: John Wiley & Sons Inc., 2008.

[7] European Commission, Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions. (2011) Energy Roadmap 2050 (Last accessed: 23/07/2013). [Online]. Available: http://ec.europa.eu/energy/energy2020/roadmap/doc/com_2011_8852_en.pdf

[8] ——. (2011) Energy Roadmap 2050: Impact Assessment and Scenario Analysis (Last accessed: 23/07/2013). [Online]. Available: http://ec.europa.eu/energy/energy2020/roadmap/doc/roadmap2050_ia_20120430_en.pdf

[9] A. Ipakchi and F. Albuyeh, "Grid of the Future," *IEEE Power and Energy Magazine*, vol. 7, no. 2, pp. 52–62, March-April 2009.

[10] European Commission, Communication from the Commission to the Council and the European Parliament. (2007) Renewable Energy Road Map, Renewable Energies in the 21st Century: Building a more Sustainable Future (Last accessed: 23/07/2013). [Online]. Available: http://ec.europa.eu/energy/energy_policy/doc/03_renewable_energy_roadmap_en.pdf

[11] J. Beerten, *Modeling and Control of DC Grids*. Ph.D. dissertation, Katholieke Universiteit Leuven (KU Leuven), Belgium, 2013.

[12] Li, Y W and Kao, C.-N., "An Accurate Power Control Strategy for Power-Electronics-Interfaced Distributed Generation Units Operating in a Low-Voltage Multibus Microgrid," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2977–2988, Dec. 2009.

[13] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002–1016, June 2006.

[14] F. Blaabjerg, A. Consoli, J. A. Ferreira, and J. D. Van Wyk, "The Future of Electronic Power Processing and Conversion," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 715–720, May 2005.

[15] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez, "Control of Power Converters in AC Microgrids," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[16] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in *Power Conversion Conference (PCC 2007)*, April 2007, pp. P–9–P–29.

[17] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *6th International Conference on Integrated Power Electronics Systems (CIPS 2010)*, March 2010, pp. 1–20.

[18] Homepage of the European Center for Power Electronics (ECPE). (2013). [Online]. Available: www.ecpe.org

[19] M. Marz, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, "Power Electronics System Integration for Electric and Hybrid Vehicles," in *6th International Conference on Integrated Power Electronics Systems (CIPS 2010)*, March 2010, pp. 1–10.

[20] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An Automotive Onboard 3.3-kW Battery Charger for PHEV Application,"

IEEE Transactions on Vehicular Technology, vol. 61, no. 8, pp. 3466–3474, Oct. 2012.

[21] A. Emadi, Y.-J. Lee, and K. Rajashekara, "Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2237–2245, June 2008.

[22] M. Cacciato, A. Consoli, R. Attanasio, and F. Gennaro, "Soft-Switching Converter with HF Transformer for Grid-Connected Photovoltaic Systems," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 5, pp. 1678–1686, May 2010.

[23] S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo, and J. M. Carrasco, "Energy Storage Systems for Transport and Grid Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 3881–3895, Dec. 2010.

[24] K. Clement-Nyns, E. Haesen, and J. Driesen, "The Impact of Vehicle-to-Grid on the Distribution Grid," *Electric Power Systems Research, Elsevier*, vol. 81, no. 1, pp. 185–192, Jan. 2011.

[25] SMA, Germany. SMA Smart Home: The System Solution for more Independence (Last accessed: 23/07/2013). [Online]. Available: http://www.sma.de/fileadmin/content/global/Solutions/Documents/Smart_Home/SMART_HOME-KEN132741W.pdf

[26] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-Interface Bidirectional Converter for Residential DC Distribution Systems–Part One: High-Density Two-Stage Topology," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1655–1666, April 2013.

[27] X. Li and A. K. S. Bhat, "A Utility-Interfaced Phase-Modulated High-Frequency Isolated Dual LCL DC/AC Converter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 1008–1019, Feb. 2012.

[28] R. F. Coelho, L. Schimtz, and D. C. Martins, "Grid-Connected PV-Wind-Fuel Cell Hybrid System Employing a Supercapacitor Bank as Storage Device to Supply a Critical DC Load," in *IEEE 33rd International Telecommunications Energy Conference (INTELEC 2011)*, Oct. 2011, pp. 1–10.

[29] S. Haghbin, S. Lundmark, M. Alakula, and O. Carlson, "Grid-Connected Integrated Battery Chargers in Vehicle Applications: Review and New Solution," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 459–473, Feb. 2013.

[30] C. C. Chan, "The State of the Art of Electric, Hybrid, and Fuel Cell Vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 704–718, April 2007.

[31] M. Ehsani, Y. Gao, S. E. Gay, and A. Emadi, *Modern Electric, Hybrid Electric, and Fuel Cell Vehicles: Fundamentals, Theory, and Design.* Boca Raton, London, New York, Washington D.C.: CRC Press LLC, 2005.

[32] California Environmental Protection Agency: California Air Resources Board (ARB). Zero Emission Vehicle Program (Last accessed: 23/07/2013). [Online]. Available: http://www.arb.ca.gov/msprog/zevprog/zevprog.htm

[33] A Public Private Partnerships (PPP) of the European Economic Recovery Plan. European Green Cars Initiative (Last accessed: 23/07/2013). [Online]. Available: http://www.green-cars-initiative.eu/public/

[34] C. C. Chan, A. Bouscayrol, and K. Chen, "Electric, Hybrid, and Fuel-Cell Vehicles: Architectures and Modeling," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 2, pp. 589–598, Feb. 2010.

[35] A. Emadi, K. Rajashekara, S. S. Williamson, and S. M. Lukic, "Topological Overview of Hybrid Electric and Fuel Cell Vehicular Power System Architectures and Configurations," *IEEE Transactions on Vehicular Technology*, vol. 54, no. 3, pp. 763–770, May 2005.

[36] T. Franke, H. Glonner, D. Nowak, and F. Osterreicher, "Electrified Power Train - Challenges and Opportunities for the Electrical Industry," in *11th European Conference on Power Electronics and Applications (EPE 2005)*, Sept. 2005, pp. 1–12.

[37] A. Emadi, S. S. Williamson, and A. Khaligh, "Power Electronics Intensive Solutions for Advanced Electric, Hybrid Electric, and Fuel Cell Vehicular Power Systems," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 567–577, May 2006.

[38] M. Ehsani, Y. Gao, and J. M. Miller, "Hybrid Electric Vehicles: Architecture and Motor Drives," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 719–728, April 2007.

[39] F. Krismer, "Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH Zürich), Power Electronic Systems (PES) Laboratory, Zürich, Switzerland, 2010.

[40] F. Renken and J. Wolf, "Power Electronics for Hybrid-Drive Systems," in *12th European Conference on Power Electronics and Applications (EPE 2007)*, Sept. 2007, pp. 1–10.

[41] A. R. Gale and M. W. Degner, "Voltage Trade-Off Evaluation for Electric and Hybrid Electric Vehicle Applications," in *Power Electronics in Transportation*, Oct. 2002, pp. 11–15.

[42] J. Laeuffer, "Automotive Requirements for Power Electronic Converters in Traction Advanced Control Systems," in *43rd International Power Electronics Conference (PCIM 2001)*, June 2001, pp. 207–215.

[43] IEC 61851-1, "Electric Vehicle Conductive Charging System – Part 1: General Requirements." IEC, International Electrotechnical Commission, Geneva, Switzerland, 2001.

[44] S. Luyten, N. Leemput, F. Geth, J. Van Roy, J. Büscher, and J. Driesen, "Standardization of Conductive AC Charging Infrastructure for Electric Vehicles," in *22nd International Conference on Electricity Distribution (CIRED 2013)*, June 2013, Paper 0476.

[45] A. Mathoy (BRUSA Elektronic). (2008) Definition and Implementation of a Global EV Charging Infrastructure (Last accessed: 23/07/2013). [Online]. Available: http://www.park-charge.ch/documents/EV-infrastructure%20project.pdf

[46] M. G. Egan, D. L. O'Sullivan, J. G. Hayes, M. J. Willers, and C. P. Henze, "Power-Factor-Corrected Single-Stage Inductive Charger for Electric Vehicle Batteries," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 1217–1226, April 2007.

[47] M. Hartmann, T. Friedli, and J. W. Kolar, "Three-Phase Unity Power Factor Mains Interfaces of High Power EV Battery Charging Systems," in *ECPE Workshop "Power Electronics for Charging Electric Vehicles", Valencia, Spain*, March 2011.

[48] A. F. Burke, "Batteries and Ultracapacitors for Electric, Hybrid, and Fuel Cell Vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 806–820, April 2007.

[49] A. Affanni, A. Bellini, G. Franceschini, P. Guglielmi, and C. Tassoni, "Battery Choice and Management for New-Generation Electric Vehicles," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 5, pp. 1343–1349, Oct. 2005.

[50] I. Aharon and A. Kuperman, "Topological Overview of Powertrains for Battery-Powered Vehicles With Range Extenders," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 868–876, March 2011.

[51] K. Okura, "Development and Future Issues of High Voltage Systems for FCV," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 790–795, April 2007.

[52] U. Gottwick, A. Schäfert, A. Wach, and I. Faye, "Future Power Trains and Fuel Cell," in *16th International Conference on Automotive Technologies (ICAT 2006)*, Nov. 2006, pp. 1–10.

[53] J.-i. Itoh and F. Hayashi, "Ripple Current Reduction of a Fuel Cell for a Single-Phase Isolated Converter Using a DC Active Filter With a Center Tap," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 550–556, March 2010.

[54] SMA. (2013). [Online]. Available: www.sma.de

[55] SMA, Germany. Next Innovations 2013: New Product Releases (Last accessed: 23/07/2013). [Online]. Available: http://files.sma.de/dl/17333/NEXTINNO-KEN132211W.pdf

[56] C.I.S.P.R., "Limits and Methods of Measurement of Radio Disturbance Characteristics of Information Technology Equipment–Publication 22." IEC, International Special Committee on Radio Interference, Geneva, Switzerland, 1993.

[57] IEC 61000-3-2, "Electromagnetic Compatibility (EMC) – Part 3-2: Limits for Harmonic Current Emissions (Equipment Input Current $\leqslant$ 16 A per Phase)." IEC, International Electrotechnical Commission, Geneva, Switzerland, 1995.

[58] U.S. Department of Energy: Energy Efficiency & Renewable Energy, Vehicle Technologies Office. (2010) Electrical and Electronics Technical Team Roadmap (Last accessed: 23/07/2013). [Online]. Available: http://www1.eere.energy.gov/vehiclesandfuels/pdfs/program/eett_roadmap_12-7-10.pdf

[59] H.-P. Schöner and P. Hille, "Automotive Power Electronics – New Challenges for Power Electronics," in *IEEE 31st Annual Power Electronics Specialists Conference (PESC 2000)*, vol. 1, June 2000, pp. 6–11.

[60] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2% Efficiency vs. 7kW/dm^3 Power Density," in *IEEE 6th International Power Electronics and Motion Control Conference (IPEMC 2009)*, May 2009, pp. 1–21.

[61] W.-J. Gu and R. Liu, "A Study of Volume and Weight vs. Frequency for High-Frequency Transformers," in *IEEE 24th Annual Power Electronics Specialists Conference (PESC 1990)*, June 1993, pp. 1123–1129.

[62] Homepage of Triphase NV, 3001 B-Heverlee. (2013). [Online]. Available: www.triphase.com

[63] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and Efficiency Comparison of Front End AC–DC Plug-in Hybrid Charger Topologies," *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 413–421, March 2012.

[64] C. B. Marxgut, "Ultra-Flat Isolated Single-Phase AC–DC Converter Systems," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH Zürich), Power Electronic Systems (PES) Laboratory, Zürich, Switzerland, 2013.

[65] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A Review of Single-Phase Improved Power Quality AC-DC Converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[66] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A Review of Single-Phase PFC Topologies Based on the Boost Converter," in *IEEE/IAS 9th International Conference on Industry Applications (INDUSCON 2010)*, Nov. 2010, pp. 1–6.

[67] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifier with High Efficiency and High Power Density," in *International Power Electronics Conference (IPEC 2010)*, June 2010, pp. 1725–1732.

[68] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[69] R. L. Steigerwald, "A Comparison of Half-Bridge Resonant Converter Topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, April 1988.

[70] R. L. Steigerwald, R. W. De Doncker, and M. H. Kheraluwala, "A Comparison of High-Power DC–DC Soft-Switched Converter Topologies," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1139–1145, Sept.-Oct. 1996.

[71] F. Krismer, J. Biela, and J. W. Kolar, "A Comparative Evaluation of Isolated Bi-directional DC/DC Converters with Wide Input and Output Voltage Range," in *40th Industry Applications Conference Annual Meeting (IAS 2005)*.

[72] A. Mehdipour and S. Farhangi, "Comparison of Three Isolated Bi-Directional DC/DC Converter Topologies for a Backup Photovoltaic Application," in *2nd International Conference on Electric Power and Energy Conversion Systems (EPECS 2011)*, Nov. 2011, pp. 1–5.

[73] N. M. L. Tan, T. Abe, and H. Akagi, "Topology and Application of Bidirectional Isolated DC–DC Converters," in *IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE 2011 - ECCE Asia)*, May 2011, pp. 1039–1046.

[74] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Comparative Evaluation of Soft-Switching, Bidirectional, Isolated AC/DC Converter Topologies," in *IEEE 27th Annual Applied Power Electronics Conference and Exposition (APEC 2012)*, Feb. 2012, pp. 1067–1074.

[75] A. Fernandez, J. Sebastian, M. M. Hernando, P. Villegas, and J. Garcia, "Helpful Hints to Select a Power-Factor-Correction Solution for Low- and Medium-Power Single-Phase Power Supplies," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 46–55, Feb. 2005.

[76] L. Petersen and M. Andersen, "Two-Stage Power Factor Corrected Power Supplies: the Low Component-Stress Approach," in *IEEE 17th Annual Applied Power Electronics Conference and Exposition (APEC 2002)*, vol. 2, March 2002, pp. 1195–1201.

[77] S. Cuk, "True Bridgeless PFC Converter Achieves Over 98% Efficiency, 0.999 Power Factor," *Power Electronics Technology Magazine*, Part 1: pp. 10–18, July 2010; Part 2: pp. 34–40, Aug. 2010; Part 3: pp. 22–31, Oct. 2010.

[78] D. Bortis, L. Fassler, and J. W. Kolar, "Comprehensive Analysis and Comparative Evaluation of the Isolated True Bridgeless Cuk Single-Phase PFC Rectifier System," in *IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL 2013)*, June 2013, pp. 1–9.

[79] S. Norrga, "A Soft-Switched Bi-Directional Isolated AC/DC Converter for AC-Fed Railway Propulsion Applications," in *International Conference on Power Electronics, Machines and Drives (PEMD 2002)*, June 2002, pp. 433–438.

[80] ——, "Experimental Study of a Soft-Switched Isolated Bidirectional AC-DC Converter Without Auxiliary Circuit," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1580–1587, Nov. 2006.

[81] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient High-Frequency Soft-Switched Power Converter with Signal Processor Control," in *IEEE 13th International Telecommunications Energy Conference (INTELEC 1991)*, Nov. 1991, pp. 631–639.

[82] M. H. Kheraluwala and R. W. De Doncker, "Single Phase Unity Power Factor Control for Dual Active Bridge Converter," in *IEEE Industry Applications Society Annual Meeting*, vol. 2, Oct. 1993, pp. 909–916.

[83] J. Everts, J. Van den Keybus, and J. Driesen, "Switching Control Strategy to Extend the ZVS Operating Range of a Dual Active Bridge AC/DC Converter," in *IEEE Energy Conversion Congress and Exposition (ECCE 2011)*, Sept. 2011, pp. 4107–4114.

[84] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching Control Strategy for Full ZVS Soft-Switching Operation of a Dual Active Bridge AC/DC Converter," in *IEEE 27th Annual Applied Power Electronics Conference and Exposition (APEC 2012)*, Feb. 2012, pp. 1048–1055.

[85] F. Jauch and J. Biela, "Single-Phase Single-Stage Bidirectional Isolated ZVS AC-DC Converter with PFC," in *15th International Power Electronics and Motion Control Conference (EPE/PEMC 2012)*, Sept. 2012, pp. LS5d.1–1–LS5d.1–8.

[86] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC-DC Converters," *IEEE Transactions on Power Electronics*, DIO: 10.1109/TPEL.2013.2292026, available as early access article in IEEE Xplore, 2013.

[87] ——, "Charge-Based ZVS Soft Switching Analysis of a Single-Stage Dual Active Bridge AC-DC Converter," in *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Sept. 2013, pp. 4820–4829.

[88] N. D. Weise, K. Basu, G. Castelino, and N. Mohan, "A Single-Stage Dual Active Bridge Based Soft Switched AC–DC Converter with Open-Loop Power Factor Correction and Other Advanced Features," *IEEE Transactions on Power Electronics*, DIO: 10.1109/TPEL.2013.2293112, available as early access article in IEEE Xplore, 2013.

[89] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A Three-Phase Soft-Switched High Power Density DC/DC Converter for High Power Applications," in *IEEE Industry Applications Society Annual Meeting*, vol. 1, Oct. 1988, pp. 796–805.

[90] R. W. DeDoncker, D. M. Divan, and M. H. Kheraluwala, "Power Conversion Apparatus for DC/DC Conversion using Dual Active Bridges," Patent US5 027 264 A, June 25, 1991.

[91] Y. Wang, S. W. H. de Haan, and J. A. Ferreira, "Optimal Operating Ranges of Three Modulation Methods in Dual Active Bridge Converters," in *IEEE 6th International Power Electronics and Motion Control Conference (IPEMC 2009)*, May 2009, pp. 1397–1401.

[92] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[93] A. K. Jain and R. Ayyanar, "PWM Control of Dual Active Bridge: Comprehensive Analysis and Experimental Verification," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1215–1227, April 2011.

[94] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-Coupled Multiport ZVS Bidirectional DC–DC Converter With Wide Input Range," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 771–781, March 2008.

[95] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation Strategy to Operate the Dual Active Bridge DC-DC Converter Under Soft Switching in the Whole Operating Range," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1228–1236, April 2011.

[96] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance Characterization of a High-Power Dual Active Bridge dc-to-dc Converter," *IEEE Transactions on Industry Applications*, vol. 28, no. 6, pp. 1294–1301, Nov.-Dec. 1992.

[97] K. Vangen, T. Melaa, and A. K. Adnanes, "Soft-Switched High-Frequency, High Power DC/AC Converter with IGBT," in *IEEE 23rd Annual Power Electronics Specialists Conference (PESC 1992)*, 1992, pp. 26–33 vol.1.

[98] G. Guidi, A. Kawamura, Y. Sasaki, and T. Imakubo, "Dual Active Bridge Modulation with Complete Zero Voltage Switching Taking Resonant Transitions Into Account," in *14th European Conference on Power Electronics and Applications (EPE 2011)*, Sept. 2011, pp. 1–10.

[99] Z. Shen, R. Burgos, D. Boroyevich, and F. Wang, "Soft-Switching Capability Analysis of a Dual Active Bridge DC-DC Converter," in *IEEE Electric Ship Technologies Symposium (ESTS 2009)*, April 2009, pp. 334–339.

[100] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo, and Y. Sasaki, "Improvement of Light Load Efficiency of Dual Active Bridge DC-DC Converter by Using Dual Leakage Transformer and Variable Frequency," in *IEEE Energy Conversion Congress and Exposition (ECCE 2010)*, Sept. 2010, pp. 830–837.

[101] U. Drofenik, A. Musing, and J. W. Kolar, "Voltage-Dependent Capacitors in Power Electronic Multi-Domain Simulations," in *International Power Electronics Conference (IPEC 2010)*, June 2010, pp. 643–650.

[102] D. Fu, F. C. Lee, and S. Wang, "Investigation on Transformer Design of High Frequency High Efficiency DC–DC Converters," in *IEEE 25th Annual Applied Power Electronics Conference and Exposition (APEC 2010)*, Feb. 2010, pp. 940–947.

[103] B. Cougo and J. W. Kolar, "Integration of Leakage Inductance in Tape Wound Core Transformers for Dual Active Bridge Converters," in *7th International Conference on Integrated Power Electronics Systems (CIPS 2012)*, March 2012, pp. 1–6.

[104] M. Meinhardt, M. Duffy, T. O'Donnell, S. O'Reilly, J. Flannery, and C. O Mathuna, "New Method for Integration of Resonant Inductor and Transformer— Design, Realisation, Measurements," in *IEEE 14th Annual Applied Power Electronics Conference and Exposition (APEC 1999)*, vol. 2, March 1999, pp. 1168–1174.

[105] Gecko-Simulations AG - GeckoCIRCUITS. (2013) Free version available. [Online]. Available: www.gecko-simulations.com

[106] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential Mode Input Filter Design for a Three-Phase Buck-Type PWM Rectifier Based on Modeling of the EMC Test Receiver," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.

[107] R. W. Erickson, "Optimal Single Resistors Damping of Input Filters," in *IEEE 14th Annual Applied Power Electronics Conference and Exposition (APEC 1999)*, vol. 2, March 1999, pp. 1073–1079.

[108] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme Efficiency Power Electronics," in *7th International Conference on Integrated Power Electronics Systems (CIPS 2012)*, March 2012, pp. 1–22.

[109] FAIRCHILD Semiconductor. (2013). [Online]. Available: www.fairchildsemi.com

[110] ST Microelectronics. (2013). [Online]. Available: www.st.com

[111] Infineon Technologies AG. (2011) First 650 V Rated Super Junction MOSFET with Fast Body Diode Suitable for Resonant Topologies. [Online]. Available: www.infineon.com

[112] ——. (2013). [Online]. Available: www.infineon.com

[113] BERGQUIST. (2013). [Online]. Available: www.bergquistcompany.com

[114] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling," in *International PCIM Europe 2005 Conference (PCIM 2005)*, June 2005, pp. 608–619.

[115] U. Drofenik and J. W. Kolar, "Sub-Optimum Design of a Forced Air Cooled Heat Sink for Simple Manufacturing," in *Power Conversion Conference - Nagoya (PCC 2007)*, 2007, pp. 1189–1194.

[116] C. Buccella, C. Cecati, and F. de Monte, "A Coupled Electrothermal Model for Planar Transformer Temperature Distribution Computation," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 10, pp. 3583–3590, Oct. 2008.

[117] G. Ortiz, J. Biela, and J. W. Kolar, "Optimized Design of Medium Frequency Transformers with High Isolation Requirements," in *IEEE 36th Annual Industrial Electronics Society Conference (IECON 2010)*, Nov. 2010, pp. 631–638.

[118] FERROXCUBE. (2013). [Online]. Available: www.ferroxcube.com

[119] TDK EPCOS. (2013). [Online]. Available: www.epcos.com

[120] J. A. Ferreira, "Analytical Computation of AC Resistance of Round and Rectangular Litz Wire Windings," *IEE Proceedings B, Electric Power Applications*, vol. 139, no. 1, pp. 21–25, Jan. 1992.

[121] C. R. Sullivan, "Optimal Choice for Number of Strands in a Litz-Wire Transformer Winding," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 283–291, March 1999.

[122] J. Mühlethaler, J. W. Kolar, and A. Ecklebe, "Loss Modeling of Inductive Components Employed in Power Electronic Systems," in *IEEE 8th International Conference on Power Electronics (ICPE ECCE Asia 2011)*, June 2011, pp. 945–952.

[123] ——, "A Novel Approach for 3D Air Gap Reluctance Calculations," in *IEEE 8th International Conference on Power Electronics (ICPE ECCE Asia 2011)*, June 2011, pp. 446–452.

[124] PACK Feindrähte. (2013). [Online]. Available: www.pack-feindraehte.de

[125] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate Prediction of Ferrite Core Loss with Nonsinusoidal Waveforms Using only Steinmetz Parameters," in *IEEE Workshop on Computers in Power Electronics*, June 2002, pp. 36–41.

[126] I. Villar, U. Viscarret, I. Etxeberria-Otadui, and A. Rufer, "Global Loss Evaluation Methods for Nonsinusoidally Fed Medium-Frequency Power Transformers," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 10, pp. 4132–4140, Oct. 2009.

[127] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 964–973, Feb. 2012.

[128] D. Aggeler, J. Biela, and J. W. Kolar, "A Compact, High Voltage 25 kW, 50 kHz DC-DC Converter Based on SiC JFETs," in *IEEE 23th Annual Applied Power Electronics Conference and Exposition (APEC 2008)*, Feb. 2008, pp. 801–807.

[129] J. Biela and J. W. Kolar, "Cooling Concepts for High Power Density Magnetic Devices," in *Power Conversion Conference (PCC 2007)*, April 2007, pp. 1–8.

[130] Panasonic Industrial. (2013). [Online]. Available: www.panasonic.com/industrial/

[131] Vishay Dale. (2013). [Online]. Available: www.vishay.com

[132] A. Stupar, T. Friedli, J. Minibock, M. Schweizer, and J. W. Kolar, "Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400 V DC Distribution Systems," in *IEEE 26th Annual Applied Power Electronics Conference and Exposition (APEC 2011)*, March 2011, pp. 505–512.

[133] M. L. Heldwein, "EMC Filtering of Three-Phase PWM Converters," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH Zürich), Power Electronic Systems (PES) Laboratory, Zürich, Switzerland, 2008.

[134] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Common Mode Modelling and Filter Design for a Three-Phase Buck-Type Pulse Width Modulated Rectifier System," *IET Power Electronics*, vol. 3, no. 2, pp. 209–218, March 2010.

[135] C.I.S.P.R., "Specification for Radio Interference Measuring Apparatus and Measurement Methods–Publication 16." IEC, International Special Committee on Radio Interference, Geneva, Switzerland, 1977.

[136] Magnetics. (2013). [Online]. Available: www.mag-inc.com

[137] VAC Vacuumschmelze. (2013). [Online]. Available: www.vacuumschmelze.com

[138] J. Mühlethaler, H. Uemura, and J. W. Kolar, "Optimal Design of EMI Filters for Single-Phase Boost PFC Circuits," in *38th Annual Conference of the IEEE Industrial Electronics Society (IECON 2012)*, Oct. 2012, pp. 632–638.

[139] Triphase NV. (2013) 3PExpress^{TM}, Rapid System Development for Power Conversion Applications. [Online]. Available: www.triphase.com

[140] KEB. (2013). [Online]. Available: www.keb.de

[141] California Instruments. (2013). [Online]. Available: www.calinst.com

[142] D. Chen and J. Liu, "The Uni-Polarity Phase-Shifted Controlled Voltage Mode AC-AC Converters with High Frequency AC Link," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 899–905, July 2006.

[143] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight Optimization of a Cooling System Composed of Fan and Extruded Fin Heat Sink," in *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Sept. 2013, pp. 2193–2200.

[144] G. G. Oggier, M. Ordonez, J. M. Galvez, and F. Luchino, "Fast Transient Boundary Control and Steady-State Operation of the Dual Active Bridge Converter Using the Natural Switching Surface," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 946–957, Feb. 2014.

[145] G. G. Oggier and M. Ordonez, "Boundary Control of Full-Bridge ZVS: Natural Switching Surface for Transient and Steady-State Operation," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 969–979, Feb. 2014.

[146] F. Krismer and J. W. Kolar, "Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.

Curriculum Vitae

Jordi Everts
Born April 25, 1985 in Maaseik, Belgium.

1997–2003	Secondary school Industrial Sciences (8h of mathematics) Technisch Instituut Sint-Jansberg Maaseik, Belgium
2003–2007	Master of Science, Electromechanical Engineering Option: Electromechanical Engineering Limburg Catholic University College (LCUC – KHLim) Diepenbeek, Belgium Graduated magna cum laude
2007–2009	Project Engineer & Teacher Electrical Engineering Limburg Catholic University College (LCUC – KHLim) Diepenbeek, Belgium
2009–2014	PhD in Engineering Science University of Leuven (KU Leuven) Department of Electrical Engineering (ESAT) Division of Electrical Energy and Computer Architectures (ELECTA) Leuven, Belgium From 2009 to 2012: IWT-Flanders PhD Fellowship

Publications, Awards, and Research Stays

List of Publications

The results achieved during the course of this doctoral work have been published in international conferences and journals as listed below. This resulted in eleven scientific papers and two patents.

Publications Related to this Dissertation

This first list enumerates the technical papers and patents which directly relate to the main topic of the doctoral research.

1. J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J.W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," in *IEEE Transactions on Power Electronics*, accepted for publication, DOI: 10.1109/TPEL.2013.2292026.

2. J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J.W. Kolar, "Charge-Based ZVS Soft Switching Analysis of a Single-Stage Dual Active Bridge AC–DC Converter," in *Proceedings of the 5th IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Denver-Colorado (USA), Sept. 2013, pp. 4820–4829.

3. J. Everts and J.W. Kolar, "Elektrischer Leistungswandler zur DC/DC-Wandlung mit Dualen Aktiven Brücken", Swiss Patent Application No. 402/13, filed 4.2.2013.

4. J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J.W. Kolar, "Comparative Evaluation of Soft-Switching, Bidirectional, Isolated AC/DC Converter Topologies," in *Proceedings of the 27th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2012)*, Orlando-Florida (USA), Feb. 2012, pp. 1067–1074.

5. J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J.W. Kolar, "Switching Control Strategy for Full ZVS Soft-Switching Operation of a Dual Active Bridge AC/DC Converter," in *Proceedings of the 27th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2012)*, Orlando-Florida (USA), Feb. 2012, pp. 1048–1055.

6. J. Everts, J. Van den Keybus, and J. Driesen, "Switching Control Strategy to Extend the ZVS Operating Range of a Dual Active Bridge AC/DC Converter," in *Proceedings of the 3th IEEE Energy Conversion Congress and Exposition (ECCE 2011)*, Phoenix-Arizona (USA), Sept. 2011, pp. 4107–4114.

Further Publications

The following publications are the result of the work that has been carried out during the first eighteen months of the doctoral studies and mainly relates to the development of basic power converters and test circuits for the characterization of Gallium Nitride (GaN) semiconductor devices. However, this work is not directly linked to this dissertation since due to an unexpected shutdown of the GaN component delivery by an industry partner and due to the unavailability of commercially available high performance GaN power devices, a reorientation of the doctoral work took place.

7. R. Gelagaev, P. Jacqmaer, J. Everts, and J. Driesen, "A Novel Voltage Clamp Circuit for the Measurement of Transistor Dynamic On-Resistance," in *Proceedings of the IEEE Instrumentation and Measurement Technology Conference (I2MTC 2012)*, Graz (Austria), May 2012, pp. 111–116.

8. J. Driesen, J. Everts, R. Gelagaev, P. Jacqmaer, and J. Van den Keybus, "Voltage Clamping Circuit and Use Thereof", patent, WO/2011/135094.

9. J. Das, J. Everts, J. Van den Keybus, M. Van Hove, D. Visalli, P. Srivastava, D. Marcon, K. Cheng, M. Leys, S. Decoutere, J. Driesen, and G. Borghs, "A 96% Efficient High-Frequency DC–DC Converter Using E-Mode GaN DHFETs on Si," in *IEEE Electron Device Letters*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011.

10. J. Everts, J. Das, J. Van den Keybus, J. Genoe, M. Germain, and J. Driesen, "A High-Efficiency, High-Frequency Boost Converter using Enhancement Mode GaN DHFETs on Silicon," in *Proc. of the IEEE Energy Conversion Congress and Expo (ECCE 2010)*, Atlanta-Georgia (USA), Sept. 2010, pp. 3296–3302.

11. P. Jacqmaer, J. Everts, R. Gelagaev, P. Tant, and J. Driesen, "Fast Robust Gate-Drivers with Easy Adjustable Voltage Ranges for Driving Normally-On Wide-Bandgap Power Transistors," in *Proceedings of the IEEE International Power Electronics and Motion Control Conference (EPE-PEMC 2010)*, Ohrid (Macedonia), Sept. 2010, pp. T2-44–T2-51.

12. J. Everts, P. Jacqmaer, R. Gelagaev, J. Van den Keybus, J. Das, M. Germain, and J. Driesen, "A Hard Switching VIENNA Boost Converter for Characterization of AlGaN/GaN/AlGaN Power DHFETs," in *Proceedings of the International Exhibition and Conference for Power Electronics Intelligent Motion Power Quality (PCIM Europe 2010)*, Nuremberg (Germany), May 2010, pp. 309–314, IET Inspec database.

13. J. Everts, J. Das, J. Van dan Keybus, M. Germain, and J. Driesen, "GaN-Based Power Transistors for Future Power Electronic Converters," in *Proceedings of the IEEE Benelux Young Researchers Symposium on Smart Sustainable Power Delivery (YRS 2010)*, Leuven (Belgium), March 2010.

List of Awards

1. **Winner of the 2013 SEMIKRON Young Professional Award:**
   - *Proposal:* "Bidirectional Isolated ZVS DAB DC–DC Converter with Ultra Wide Input and/or Output Voltage Range, being Applied in a Single-Stage PFC AC–DC Electric Vehicle Battery Charger".
   - *Awarded by* the SEMIKRON Foundation and the European Center for Power Electronics (ECPE).
   - *Awarded at* the International Exhibition and Conference for Power Electronics Intelligent Motion Power Quality (PCIM Europe 2013), Nuremberg, Germany.
   - *Awarded to* young professionals less than 30 years of age.
   - *Selection criteria:* level of innovation and social benefit.
2. **Student Industry Session Poster Presentation Award** at the IEEE 5th Energy Conversion Congress and Exposition (ECCE 2013), Denver-Colorado (USA), Sept. 2013.
   - *Paper:* "Charge-Based ZVS Soft Switching Analysis of a Single-Stage Dual Active Bridge AC–DC Converter".
3. **Best Overall Student Poster Presentation Award Winner for all ECCE 2013 Posters** at the IEEE 5th Energy Conversion Congress and Exposition (ECCE 2013), Denver-Colorado (USA), Sept. 2013.
   - *Paper:* "Charge-Based ZVS Soft Switching Analysis of a Single-Stage Dual Active Bridge AC–DC Converter".
4. **Best Presentation Award** at the IEEE 27th Annual Applied Power Electronics Conference and Exposition (APEC 2012), Orlando-Florida (USA), Feb. 2012.
   - *Paper:* "Switching Control Strategy for Full ZVS Soft-Switching Operation of a Dual Active Bridge AC/DC Converter".

List of Academic Research Stays

1. Visiting Ph.D. Researcher (Flemish FWO grant) at the Power Electronic Systems Laboratory (PES-Lab) of the Swiss Federal Institute of Technology (ETH Zürich), Zürich, Switzerland, 2012, March–August (5 months).
2. Visiting Ph.D. Researcher (Flemish FWO grant) at the Power Electronic Systems Laboratory (PES-Lab) of the Swiss Federal Institute of Technology (ETH Zürich), Zürich, Switzerland, 2011, April–August (6 months).

FACULTY OF ENGINEERING SCIENCE
DEPARTMENT OF ELECTRICAL ENGINEERING (ESAT)
DIVISION OF ELECTRICAL ENERGY AND COMPUTER
ARCHITECTURES (ELECTA)
Kasteelpark Arenberg 10, box 2445
B-3001 HEVERLEE, BELGIUM
tel. + 32 16 32 10 20
www.esat.kuleuven.be/electa